LECTURE NOTES

ON

POWER ELECTRONICS

III B. Tech I Semester (JNTUA-R15)

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SYLLABUS

UNIT I: POWER SEMI CONDUCTOR DEVICES

UNIT II: PHASE CONTROLLED CONVERTERS

UNIT III: CHOPPERS AND REGULATORS
Commutation Circuits – Time Ratio Control and Current Limit Control Strategies – Step Down and Step up Choppers Derivation of Load Voltage and Currents with R, RL and RLE Loads- Step Up Chopper – Load Voltage Expression– Problems. Study of Buck, Boost and Buck-Boost regulators, buck regulator TPS54160, hysteretic buck regulator e.g.LM3475, Switching Regulator and characteristics of standard regulator ICs – TPS40200, TPS40210, TPS 7A4901, TPS7A8300

UNIT IV: INVERTERS

UNIT V: AC VOLTAGE CONTROLLERS & CYCLO CONVERTERS
Cyclo Converters – Single Phase Mid Point Cycloconverters with Resistive and Inductive Load (Principle of Operation only) – Bridge Configuration of Single Phase Cycloconverter (Principle of Operation only) – Waveforms

TEXT BOOKS:

REFERENCE BOOKS:
UNIT-I

POWER SEMICONDUCTOR DEVICES
POWER ELECTRONICS

The control of electric motor drives requires control of electric power. Power electronics have eased the concept of power control. Power electronics signifies the word power electronics and control or we can say the electronic that deal with power equipment for power control.

Power electronics based on the switching of power semiconductor devices. With the development of power semiconductor technology, the power handling capabilities and switching speed of power devices have been improved tremendously.

Power Semiconductor Devices

The first SCR was developed in late 1957. Power semiconductor devices are broadly categorized into 3 types:

1. Power diodes \((600V,4500A)\)
2. Transistors
3. Thyristors \((10KV,300A,30MW)\)

Thyristor is a four layer three junction pnpn semiconductor switching device. It has 3 terminals these are anode, cathode and gate. SCRs are solid state device, so they are compact, possess high reliability and have low loss.
SCR is made up of silicon, it acts as a rectifier; it has very low resistance in the forward direction and high resistance in the reverse direction. It is a unidirectional device.

**Static V-I characteristics of a Thyristor**

The circuit diagram for obtaining static V-I characteristics is as shown:

Anode and cathode are connected to main source voltage through the load. The gate and cathode are fed from source $E_S$.

A typical SCR V-I characteristic is as shown below:
$V_{BO}$=Forward breakover voltage

$V_{BR}$=Reverse breakover voltage

$I_g$=Gate current

$V_a$=Anode voltage across the thyristor terminal A,K.

$I_a$=Anode current

It can be inferred from the static V-I characteristic of SCR. SCR have 3 modes of operation:

1. Reverse blocking mode
2. Forward blocking mode (off state)
3. Forward conduction mode (on state)

1. **Reverse Blocking Mode**

When cathode of the thyristor is made positive with respect to anode with switch open thyristor is reverse biased. Junctions $J_1$ and $J_2$ are reverse biased where junction $J_2$ is forward biased. The device behaves as if two diodes are connected in series with reverse voltage applied across them.

- A small leakage current of the order of few mA only flows. As the thyristor is reverse biased and in blocking mode. It is called as acting in reverse blocking mode of operation.

- Now if the reverse voltage is increased, at a critical breakdown level called reverse breakdown voltage $V_{BR}$, an avalanche occurs at $J_1$ and $J_3$ and the reverse
current increases rapidly. As a large current associated with $V_{BR}$ and hence more losses to the SCR.

This results in Thyristor damage as junction temperature may exceed its maximum temperature rise.

2. **Forward Blocking Mode**

When anode is positive with respect to cathode, with gate circuit open, thyristor is said to be forward biased.

Thus junction $J_1$ and $J_3$ are forward biased and $J_2$ is reverse biased. As the forward voltage is increases junction $J_2$ will have an avalanche breakdown at a voltage called forward breakover voltage $V_{BO}$. When forward voltage is less then $V_{BO}$ thyristor offers high impedance. Thus a thyristor acts as an open switch in forward blocking mode.

3. **Forward Conduction Mode**

Here thyristor conducts current from anode to cathode with a very small voltage drop across it. So a thyristor can be brought from forward blocking mode to forward conducting mode:

1. By exceeding the forward breakover voltage.
2. By applying a gate pulse between gate and cathode.

During forward conduction mode of operation thyristor is in on state and behave like a close switch. Voltage drop is of the order of 1 to 2mV. This small voltage drop is due to ohmic drop across the four layers of the device.

**Different turn ON methods for SCR**

1. Forward voltage triggering
2. Gate triggering
3. $\frac{dv}{dt}$ triggering
4. Light triggering
5. Temperature triggering

1. **Forward voltage triggering**
A forward voltage is applied between anode and cathode with gate circuit open.

- Junction $J_1$ and $J_3$ is forward biased.
- Junction $J_2$ is reverse biased.
- As the anode to cathode voltage is increased breakdown of the reverse biased junction $J_2$ occurs. This is known as avalanche breakdown and the voltage at which this phenomena occurs is called forward breakover voltage.
- The conduction of current continues even if the anode cathode voltage reduces below $V_{BO}$ till $I_a$ will not go below $I_h$. Where $I_h$ is the holding current for the thyristor.

2. Gate triggering

This is the simplest, reliable and efficient method of firing the forward biased SCRs. First SCR is forward biased. Then a positive gate voltage is applied between gate and cathode. In practice the transition from OFF state to ON state by exceeding $V_{BO}$ is never employed as it may destroy the device. The magnitude of $V_{BO}$, so forward breakover voltage is taken as final voltage rating of the device during the design of SCR application.

First step is to choose a thyristor with forward breakover voltage (say 800V) higher than the normal working voltage. The benefit is that the thyristor will be in blocking state with normal working voltage applied across the anode and cathode with gate open. When we require the turning ON of a SCR a positive gate voltage between gate and cathode is applied. The point to be noted that cathode n- layer is heavily doped as compared to gate p-layer. So when gate supply is given between gate and cathode gate p-layer is flooded with electron from cathode n-layer. Now the thyristor is forward biased, so some of these electron reach junction $J_2$.As a result width of $J_2$ breaks down or conduction at $J_2$ occur at a voltage less than $V_{BO}$.As $I_g$ increases $V_{BO}$ reduces which decreases then turn ON time. Another important point is duration for which the gate current is applied should be more then turn ON time. This means
that if the gate current is reduced to zero before the anode current reaches a minimum value known as holding current, SCR can’t turn ON.

In this process power loss is less and also low applied voltage is required for triggering.

3. \textbf{dv/dt triggering}

This is a turning ON method but it may lead to destruction of SCR and so it must be avoided.

When SCR is forward biased, junction $J_1$ and $J_3$ are forward biased and junction $J_2$ is reversed biased so it behaves as if an insulator is place between two conducting plate. Here $J_1$ and $J_3$ acts as a conducting plate and $J_2$ acts as an insulator. $J_2$ is known as junction capacitor. So if we increase the rate of change of forward voltage instead of increasing the magnitude of voltage. Junction $J_2$ breaks and starts conducting. A high value of changing current may damage the SCR. So SCR may be protected from high $\frac{dv}{dt}$

$$q = cv$$

$$I_a = c \frac{dv}{dt}$$

$$I_a \alpha \frac{dv}{dt}$$

4. \textbf{Temperature triggering}

During forward biased, $J_2$ is reverse biased so a leakage forward current always associated with SCR. Now as we know the leakage current is temperature dependant, so if we increase the temperature the leakage current will also increase and heat dissipitation of junction $J_2$ occurs. When this heat reaches a sufficient value $J_2$ will break and conduction starts.

Disadvantages
This type of triggering causes local hot spot and may cause thermal run away of the device.

This triggering cannot be controlled easily.

It is very costly as protection is costly.

5. **Light triggering**

First a new recess niche is made in the inner p-layer. When this recess is irradiated, then free charge carriers (electron and hole) are generated. Now if the intensity is increased above a certain value then it leads to turn ON of SCR. Such SCR are known as Light activated SCR (LASCR).

**Some definitions:**

**Latching current**

The latching current may be defined as the minimum value of anode current which at must attain during turn ON process to maintain conduction even if gate signal is removed.

**Holding current**

It is the minimum value of anode current below which if it falls, the SCR will turn OFF.

**Switching characteristics of thyristors**

The time variation of voltage across the thyristor and current through it during turn on and turn off process gives the dynamic or switching characteristic of SCR.

**Switching characteristic during turn on**

**Turn on time**

It is the time during which it changes from forward blocking state to ON state. Total turn on time is divided into 3 intervals:

1. Delay time
2. Rise time
3. Spread time

**Delay time**

If $I_g$ and $I_a$ represent the final value of gate current and anode current. Then the delay time can be explained as time during which the gate current attains 0.9 $I_g$ to the instant anode current reaches 0.1 $I_g$ or the anode current rises from forward leakage current to 0.1 $I_a$.

1. Gate current 0.9 $I_g$ to 0.1 $I_a$.
2. Anode voltage falls from $V_a$ to 0.9$V_a$.
3. Anode current rises from forward leakage current to 0.1 $I_a$. 
Rise time ($t_r$)

Time during which

1. Anode current rises from $0.1 I_a$ to $0.9 I_a$
2. Forward blocking voltage falls from $0.9V_a$ to $0.1V_a$. $V_a$ is the initial forward blocking voltage.

Spread time ($t_p$)

1. Time taken by the anode current to rise from $0.9I_a$ to $I_a$.
2. Time for the forward voltage to fall from $0.1V_o$ to on state voltage drop of 1 to 1.5V.

During turn on, SCR is considered to be a charge controlled device. A certain amount of charge is injected in the gate region to begin conduction. So higher the magnitude of gate current it requires less time to inject the charges. Thus turn on time is reduced by using large magnitude of gate current.

How the distribution of charge occurs?

As the gate current begins to flow from gate to cathode with the application of gate signal. Gate current has a non uniform distribution of current density over the cathode surface. Distribution of current density is much higher near the gate. The density decrease as the distance from the gate increases. So anode current flows in a narrow region near gate where gate current densities are highest. From the beginning of rise time the anode current starts spreading itself. The anode current spread at a rate of 0.1mm/sec. The spreading anode current requires some time if the rise time is not sufficient then the anode current cannot spread over the entire region of cathode. Now a large anode current is applied and also a large anode current flowing through the SCR. As a result turn on losses is high. As these losses occur over a small conducting region so local hot spots may form and it may damage the device.

Switching Characteristics During Turn Off

Thyristor turn off means it changed from ON to OFF state. Once thyristor is ON there is no role of gate. As we know thyristor can be made turn OFF by reducing the anode current below the latching current. Here we assume the latching current to be zero ampere. If a forward voltage is applied across the SCR at the moment it reaches zero then SCR will not be able to block this forward voltage. Because the charges trapped in the 4-layer are still favourable for conduction and it may turn on the device. So to avoid such a case, SCR is reverse biased for some time even if the anode current has reached to zero.

So now the turn off time can be different as the instant anode current becomes zero to the instant when SCR regains its forward blocking capability.

$t_q = t_{rr} + t_{qr}$ Where,
$t_q$ is the turn off time, $t_{rr}$ is the reverse recovery time, $t_{qr}$ is the gate recovery time.

At $t_1$ anode current is zero. Now anode current builds up in reverse direction with same $\frac{dv}{dt}$ slope. This is due to the presence of charge carriers in the four layers. The reverse recovery current removes the excess carriers from $J_1$ and $J_3$ between the instants $t_1$ and $t_3$. At instant $t_3$ the end junction $J_1$ and $J_3$ is recovered. But $J_2$ still has trapped charges which decay due to recombination only so the reverse voltage has to be maintained for some more time. The time taken for the recombination of charges between $t_3$ and $t_4$ is called gate recovery time $t_{qr}$. Junction $J_2$ recovered and now a forward voltage can be applied across SCR.

The turn off time is affected by:

1. Junction temperature
2. Magnitude of forward current $\frac{di}{dt}$ during commutation.

Turn off time decreases with the increase of magnitude of reverse applied voltage.

**GTO (Gate turn off thyristor)**
A gate turn off thyristor is a pnpn device. In which it can be turned ON like an ordinary SCR by a positive gate current. However it can be easily turned off by a negative gate pulse of appropriate magnitude.

Conventional SCR are turned on by a positive gate signal but once the SCR is turned on gate loses control over it. So to turn it off we require external commutation circuit. These commutation circuits are bulky and costly. So due to these drawbacks GTO comes into existence.

The salient features of GTO are:

1. GTO turned on like conventional SCR and is turned off by a negative gate signal of sufficient magnitude.
2. It is a non latching device.
3. GTO reduces acoustic and electromagnetic noise.

It has high switching frequency and efficiency.

A gate turn off thyristor can turn on like an ordinary thyristor but it is turn off by negative gate pulse of appropriate magnitude.

Disadvantage

The negative gate current required to turn off a GTO is quite large that is 20% to 30 % of anode current

Advantage

It is compact and cost less

**Switching performance**
1. For turning ON a GTO first TR1 is turned on.
2. This in turn switches on TR2 so that a positive gate current pulse is applied to turn on the GTO.
3. Thyristor \( T_1 \) is used to apply a high peak negative gate current pulse.

**Gate turn-on characteristics**

1. The gate turn on characteristics is similar to a thyristor. Total turn on time consists of delay time, rise time, spread time.
2. The turn on time can be reduced by increasing its forward gate current.
GATE TURN OFF

Turn off time is different for SCR. Turn off characteristics is divided into 3 phases:

1. Storage time
2. Fall time
3. Tail time

\[ T_o = t_s + t_f + t_t \]

At normal operating condition, GTO carries a steady state current. The turn off process starts as soon as negative current is applied after \( t=0 \).

STORAGE TIME

During the storage period, the anode voltage and current remain constant. The gate current rises depending upon the gate circuit impedance and gate applied voltage. The beginning of pd is as soon as negative gate current is applied. The end of storage pd is marked by fall in anode current and rise in voltage, what we have to do is remove the excess carriers, the excess carriers are removed by negative carriers.
FALL TIME

After $t_s$, anode current begins to fall rapidly and anode voltage starts rising. After falling to a certain value, then anode current changes its rate to fall. This time is called fall time.

SPIKE IN VOLTAGE

During the time of storage and fall time there is a change in voltage due to abrupt current change. TAIL TIME

During this time, the anode current and voltage continues towards the turn off values. The transient overshoot is due to the snubber parameter and voltage stabilizes to steady state value.
THE TRIAC

As SCR is a unidirectional device, the conduction is from anode to cathode and not from cathode to anode. It conducts in both direction. It is a bidirectional SCR with three terminal.

TRIAC=TRIODE+AC

Here it is considered to be two SCRs connected in anti parallel. As it conducts in both direction so it is named as MT1, MT2 and gate G.

SALIENT FEATURES

1. Bi directional triode thyristor
2. TRIAC means triode that works on ac
3. It conduct in both direction
4. It is a controlled device
5. Its operation is similar to two devices connected in anti parallel with common gate connection.

6. It has 3 terminals MT1, MT2 and gate G

Its use is control of power in ac.

**POWER BJT**

Power BJT means a large voltage blocking in the OFF state and high current carrying capability in the ON state. In most power application, base is the input terminal. Emitter is the common terminal. Collector is the output terminal.

**SIGNAL LEVEL OF BJT**

n+ doped emitter layer, doping of base is more than collector. Depletion layer exists more towards the collector than emitter.
POWER BJT CONSTRUCTION

The maximum collector emitter voltage that can be sustained across the junction, when it is carrying substantial collector current.

\( V_{ceo} = \text{maximum collector and emitter voltage that can be sustain by the device.} \)

\( V_{cbo} = \text{collector base breakdown voltage with emitter open} \)

PRIMARY BREAKDOWN

It is due to convention avalanche breakdown of the C-B junction and its associated large flow of current. The thickness of the depletion region determines the breakdown voltage of the transistor. The base thickness is made as small as possible, in order to have good amplification capability. If the thickness is too small, the breakdown voltage is compromised. So a compromise has to be made between the two.
THE DOPING LEVELS-
1. The doping of the emitter layer is quite large.
2. The base doping is moderate.
3. n-region is lightly doped.
4. n+ region doping level is similar to emitter.

1. THICKNESS OF DRIFT REGION-
It determines the breakdown length of the transistor.

2. THE BASE THICKNESS –
Small base thickness- good amplification capability
Too small base thickness- the breakdown voltage of the transistor has to be compromised.
For a relatively thick base, the current gain will be relatively small, so it increases the gain. Monolithic designs for darlington connected BJT pair have been developed.

SECONDARY BREAKDOWN
Secondary breakdown is due to large power dissipation at localized site within the semiconductor.

PHYSICS OF BJT OPERATION-
The transistor is assumed to operate in active region. There is no doped collector drift region. It has importance only in switching operation, in active region of operation.

junction is forward biased and C-B junction is reverse biased. Electrons are injected into base from the emitter. Holes are injected from base into the emitter.

QUASI SATURATION-
Initially we assume that, the transistor is in active region. Base current is allowed to increase then lets see what happens. first collector rises in response to base current. So there is a increase voltage drop across the collector load. So C-E voltage drops.

Because of increase in collector current, there is a increase in voltage in drift region. This eventually reduces the reverse biased across the C-B junction. so n-p junction get smaller, at some point the junction become forward biased. So now injection of holes from base into collector drift region occurs. Charge neutrality requires the electron to be injected in the drift region of the holes. From where these electron came. Since a large no of electron is supplied to the C-B junction via injection from emitter and subsequent diffusion across the base. As excess carrier build up in the drift region begins to occur quasi saturation region is entered. As the injected carries increase in the drift region is
gradually shotred out and the voltage across the drift region drops. In quasi saturation the drift region is not completely shorted out by high level injection. Hard saturation obtained when excess carrier density reaches the n+ side.

During quasi saturation, the rate of the collector fall. Hard saturation occurs when excess carriers have completely swept across the drift region.

**THYRISTOR PROTECTION**

**OVER VOLTAGE PROTECTION**

Over voltage occurring during the switching operation causes the failure of SCR.

**INTERNAL OVERVOLTAGE**

It is due to the operating condition of SCR.
During the commutation of SCR, when the anode current decays to zero anode current reverses due to stored changes. First the reverse current rises to peak value, then reverse current reduces abruptly with large \( \frac{di}{dt} \). During series inductance of SCR large transient large voltage i.e \( L \frac{di}{dt} \) is generated.

**EXTERNAL OVER VOLTAGE**

This is due to external supply and load condition. This is because of

1. The interruption of current flow in an inductive circuit.
2. Lightening strokes on the lines feeding the thyristor systems.

Suppose a SCR converter is fed from a transformer, voltage transient occur when transformer primary will energise or de-energised.

This overvoltages cause random turn ON of a SCR.

The effect of overvoltage is minimized using

1. RC circuits
2. Non linear resistor called voltage clamping device.

Voltage clamping device is a non linear resistor. It is connected between cathode and anode of SCR. The resistance of voltage clamping device decreases with increasing voltages. During normal working condition Voltage clamping (V.C) device has high resistance, drawing only leakage current. When voltage surge appears voltage clamping device offers a low resistance and it create a virtual short circuit across the SCR. Hence voltage across SCR is clamped to a safe value.
When surge condition over voltage clamping device returns to high resistance state.
e.g. of voltage clamping device
1. Selenium thyrector diodes
2. Metal Oxide varistors
3. Avalanche diode suppressors

OVER CURRENT PROTECTION
Long duration operation of SCR, during over current causes the
1. junction temp. of SCR to rise above the rated value, causing permanent
damage to device.
SCR is protected from overcurrent by using
1. Circuit breakers
2. Fast acting fuses
Proper co-ordination is essential because
1. fault current has to be interrupted before SCR gets damaged.
2. only faulty branches of the network has to be replaced.
In stiff supply network, source has negligible impedance. So in such system
the magnitude and rate of rise of current is not limited. Fault current hence
junction temp rises in a few milliseconds.

POINTS TO BE NOTED-
1. Proper coordination between fast acting fuse and thyristor is essential.
2. The fuse is always rated to carry marginal overload current over
definite period.
3. The peak let through current through SCR must be less than sub cycle
ingrating of the SCR.
4. The voltage across the fuse during arcing time is called arcing or
recovery voltage and is equal to sum of the source voltage and emf
induced in the circuit inductance during arcing time.
5. On abrupt interruption of fuse current, induce emf would be high, which
results in high arcing voltage.

Circuit Breaker (C.B)

has long tripping time. So it is used for protecting the device against continuous
overload current or against the surge current for long duration. In order that fuse
protects the thyristor realiably the $I^2t$ rating of fuse current must be less than that of
SCR.

ELECTRONIC CROWBAR PROTECTION
For overcurrent protection of power converter using SCR, electronic crowbar are used. It provide rapid isolation of power converter before any damage occurs.

HEAT PROTECTION-

To protect the SCR

1. From the local spots
2. Temp rise
   SCRs are mounted over heat sinks.

GATE PROTECTION-

Gate circuit should also be protected from

1. Overvoltages
2. Overcurrents

Overvoltage across the gate circuit causes the false triggering of SCR
Overcurrent raise the junction temperature. Overvoltage protection is by zener diode across the gate circuit.

INSULATED GATE BIPOLAR TRANSISTOR (IGBT) -

BASIC CONSTRUCTION -

The n+ layer substrate at the drain in the power MOSFET is substituted by p+ layer substrate and called as collector. When gate to emitter voltage is positive, n- channel is formed in the p- region. This n- channel short circuit the n- and n+ layer and an electron movement in n channel cause hole injection from p+ substrate layer to n- layer.
**POWER MOSFET**

A power MOSFET has three terminal device. Arrow indicates the direction of current flow. MOSFET is a voltage controlled device. The operation of MOSFET depends on flow of majority carriers only.

![Circuit diagram](Image1)  
![Circuit symbol](Image2)

**(a) (Circuit diagram)**  
**(a) (circuit symbol)**

**Switching Characteristics:-**

The switching characteristic is influenced by

1. Internal capacitance of the device.
2. Internal impedance of the gate drive circuit.

Total **turn on time** is divided into

1. Turn on delay time
2. Rise time

Turn on time is affected by impedance of gate drive source. During turn on delay time gate to source voltage attends its threshold value $V_{GST}$.

After $t_{on}$ and during rise time gate to source voltage rise to $V_{Gsp}$, a voltage which is sufficient to drive the MOSFET to ON state.

The turn off process is initiated by removing the gate to source voltage. Turn off time is composed of turn off delay time to fall time.

**Turn off delay time**
To turn off the MOSFET the input capacitance has to be discharged. During $t_{df}$ the input capacitance discharge from $V_1$ to $V_{Gsp}$. During $t_f$, fall time, the input capacitance discharges from $V_{Gsp}$ to $V_{GST}$. During $t_f$ drain current falls from $I_D$ to zero.

So when $V_{Gs} \leq V_{GST}$, MOFSET turn off is complete.

![Fig. Switching waveform of power MOSFET](image)

**Insulated Gate Bipolar Transistor (IGBT)**

IGBT has high input impedance like MOFFSET and low on state power lose as in BJT.

**IGBT Characteristics**

Here the controlling parameter is gate emitter voltage As IGBT is a voltage controlled device.

When $V_{GE}$ is less than $V_{GET}$ that is gate emitter threshold voltage IGBT is in off state.
Switching characteristics: Figure below shows the turn ON and turn OFF characteristics of IGBT.
Time between the instants forward blocking state to forward on state.

Turn on time = Delay time + Rise time

Delay time = Time for collector emitter voltage fall from $V_{CE}$ to 0.9$V_{CE}$

$V_{CE}$=Initial collector emitter voltage

$t_{do}$=collector current to rise from initial leakage current to 0.1Ic

$Ic$= Final value of collector current

Rise time

Collector emitter voltage to fall from 0.9$V_{CE}$ to 0.1$V_{CE}$.

$Ic$ to $Ic$

After $t_{on}$ the device is on state the device carries a steady current of $Ic$ and the collector emitter voltage falls to a small value called conduction drop $V_{CES}$.

Turn off time

1) Delay time $t_{df}$
2) Initial fall time $t_{f1}$
3) Final fall time $t_{f2}$

$t_{off}=t_{df} + t_{f1} + t_{f2}$

$t_{df}$ = Time during which the gate emitter voltage falls to the threshold value $V_{GET}$.

Collector current falls from $Ic$ to 0.9$Ic$ at the end of the $t_{df}$ collector emitter voltage begins to rise.

Turn off time = Collector current falls from 90% to 20% of its initial value $Ic$ OR The time during which collector emitter voltage rise from $V_{CE}$ to 0.1$V_{CE}$.

$t_{f2}$ = collector current falls from20% to 10% of $Ic$.

During this collector emitter voltage rise 0.1$V_{CE}$ to final value of $V_{CE}$.

Series and parallel operation of SCR

SCR are connected in series for h.v demand and in parallel for fulfilling high current demand. Sting efficiency can be defined as measure of the degree of utilization on SCRs in a string.

String efficiency < 1.

Derating factor (DRF)
1 – string efficiency.

If DRF more then

no. of SCRs will more, so string is more reliable.

Let the rated blocking voltage of the string of a series connected SCR is \(2V_1\) as shown in the figure below, But in the string two SCRs are supplied a maximum voltage of \(V_1+V_2\).

\[
\eta = \frac{V_1 + V_2}{2V_1}
\]

**Significance of string efficiency.**

Two SCRs are have same forward blocking voltage ,When system voltage is more then the voltage rating of a single SCR. SCRs are connected in series in a string.

There is a inherent variation in characteristics. So voltage shared by each SCR may not be equal. Suppose, SCR1 leakage resistance > SCR2 leakage resistance. For same leakage current \(I_0\) in the series connected SCRs. For same leakage current SCR1 supports a voltage \(V_1\), SCR2 supports a voltage \(V_2\),

So string \(\eta\) for two SCRs \(=\frac{V_1+V_2}{2V_2} = \frac{1}{2} (1 + \frac{V_2}{V_1}) < 1\).

So, \(V_1 > V_2\).

The above operation is when SCRs are not turned ON. But in steady state of operation , A uniform voltage distribution in the state can be achieved by connect a suitable resistance across each SCRs , so that parallel combination have same resistance.

But this is a cumbersome work. During steady state operation we connect same value of shunt resistance across each SCRs. This shunt resistance is called *state equalizing circuit.*

Suppose,
Let SCR1 has lower leakage current \( l_{brmn} \). It will block a voltage comparatively larger than other SCRs.

Voltage across SCR1 is \( V_{bm} = I_1 R \).

Voltage across (n-1)SCR is (n-1) \( I_2 R \), so the voltage equation for the series circuit is

\[
V_s = I_1 R + (n-1)I_2 R = V_{brm} + (n-1)R (I - l_{brmx})
\]

As \( I_1 = l - l_{brmn} \)

\( I_2 = l - l_{brmx} \)

So, \( V_s = V_{brm} + (n-1)R [l_1 - (l_{brmx} - l_{brmn})] \) If

\( \Delta I_b = l_{brmx} - l_{brmn} \)

Then \( V_s = V_{brm} + (n-1)R (I_1 - \Delta I_b) \)

\( V_s = V_{brm} + (n-1)R I_1 - (n-1)R \Delta I_b \)

\( R I_1 = V_{brm} \)

So, \( V_s = V_{brm} + (n-1) V_{brm} - (n-1)R \Delta I_b \)

\[
= n V_{brm} - (n-1)R \Delta I_b
\]

\[
\Rightarrow R = \frac{nV_{brm} - V_s}{(n-1)\Delta I_b}
\]

SCR data sheet usually contain only maximum blocking current, \( l_{brmx} \)

so we assume \( l_{brmn} = 0 \)

So \( \Delta I_b = l_{brmx} \)

So the value of R calculated is low than actually required.

**SCRs having unequal dynamic characteristics:**
It may occur that SCRs may have unequal dynamic characteristics so the voltage
distribution across the SCR may be unequal during the transient condition.

SCR 1 and SCR 2 have different dynamic characteristics. Turn ON time of SCR 2 is more
than SCR 1 by time $\Delta t_d$.

As string voltage is $V_S$ so voltage shared by each SCRs be $V_S/2$. Now both are gated at same
time so SCR 1 will turn ON at $t_1$ its voltage fall nearly to zero so the voltage shared by SCR
2 will be the string voltage if the break over voltage of SCR 2 is less than $V_S$ then SCR 2 will
turn ON.

* In case $V_S$ is less than the breakoverer voltage, SCR 2 will turn ON at instant 2. SCR 1
assumed to have less turn off $t_{q1}$ time then SCR 2, so $t_{q1} < t_{q2}$. At $t_2$ SCR 1 has recovered
while SCR 2 is developing recovery voltage at $t_1$ both are developing different reverse
recovery voltage.

At $t_2$ SCR 1 has recovered while SCR 2 is developing reverse recovery voltage.

**Conclusion:**

* Series connected SCR develop different voltages during turn ON and turn OFF
process. Till now we connect a simple resistor across the diode for static voltage equalizing
circuit.

* During turn ON and turn OFF capacitance of reverse biased junction determine the
voltage distribution across SCRs in a series connected string. As reverse biased junction
have different capacitance called self capacitance, the voltage distribution during turn ON
and turn Off process would be different.
* Under transient condition equal voltage distribution can be achieved by employing shunt capacitance as this shunt capacitance has the effect of that the resultant of shunt and self capacitance tend to be equal. The capacitor is used to limits the $dv/dt$ across the SCR during forward blocking state. When this SCR turned ON capacitor discharges heavy current through the SCR. The discharge current spike is limited by damping resistor $R_c$. $R_c$ also damps out high frequency oscillation that may arise due to series combination of $R_c , C$ and series inductor. $R_c$ & $C$ are called dynamic equalizing circuit.

Diode D is used during forward biased condition for more effective charging of the capacitor. During capacitor discharge $R_c$ comes into action for limiting current spike and rate of change of current $di/dt$.

The $R, R_c$ & $C$ component also provide path to flow reverse recovery current. When one SCR regain its voltage blocking capability. The flow of reverse recovery current is necessary as it facilitates the turning OFF process of series connected SCR string. So C is necessary for both during turn ON and turn OFF process. But the voltage unbalance during turn OFF time is more predominant then turn ON time. So choice of C is based on reverse recovery characteristic of SCR.
SCR 1 has short recovery time as compared to SCR 2. \( \Delta Q \) is the difference in reverse recovery charges of two SCR 1 and SCR 2. Now we assume the SCR 1 recovers fast i.e it goes into blocking state so charge \( \Delta Q \) can pass through C. The voltage induced by \( c_1 \) is \( \Delta Q/C \), where is no voltage induced across \( C_2 \).

The difference in voltage to which the two shunt capacitor are charged is \( \Delta Q/C \).

Now thyristor with least recovery time will share the highest transient voltage say \( V_{bm} \),

So, \( V_{bm} - V_2 = \Delta Q/C \)

So, \( V_2 = V_{bm} - \Delta Q/C \)

As \( V_1 = V_{bm} \)

\( V_S = V_1+V_2 \)

\( = V_{bm}+(V_{bm} - \Delta Q/C) \)

\( V_S = 2V_{bm} - \Delta Q/C \)

\( \Rightarrow \frac{1}{2}(V + \Delta Q/C) = V \)

\( \Rightarrow V_2 = V_{bm} - \Delta Q/C \)

\( \Rightarrow \frac{1}{2}[V_S - \Delta Q/C] \)

Now suppose that there are \( n \) series SCRs in a string.
Let us assume that if top SCR has similar to characteristic SCR 1. Then SCR 1 would support a voltage $V_{bm}$

* If the remaining $(n-1)$ SCR has characteristic that of SCR 2. Then SCR 1 would recover first and support a voltage $V_{bm}$. The charge $(n-1) \Delta Q$ from the remaining $(n - 1)$ SCR would pass through C.

$V_1 = V_{bm}$

$V_2 = V_{bm} - \Delta Q/C$

Voltage across $(n-1)$ slow thyristors

$V = (n-1) (V_{bm} - \Delta Q/C)$

So,

$V_S = V_1 + (n-1) V_2$

$= V_{bm} + (n-1) (V_{bm} - \Delta Q/C)$

By simplifying we get,

$V_{bm} = \frac{L}{n} [V_S + (n-1) \Delta Q/C]$  

$C = \left[ (n-1) \Delta Q / (nV_{bm} - V_S) \right]$

$V_2 = (V_S - \Delta Q/C) / n$.

**Parallel operation:**

When current required by the load is more than the rated current of single thyristor, SCRs are connected in parallel in a string.
For equal sharing of current, SCRs must have same $V - I$ characteristics during forward conduction. $V_T$ across them must be same. For same $V_T$, SCR 1 share $I_1$ and SCR 2 share $I_2$.

If $I_1$ is the rated current

$$I_2 < I_1$$

The total current $I_1 + I_2$ and not rated current $2I_1$. Type equation here.

Thus string efficiency,

$$\frac{I_1 + I_2}{2I_1} = \frac{I_1}{2I_1} + \frac{I_2}{I_1}$$

Middle conductor will have more inductance as compared to other two nearby conductor. As a result less current flow through the middle conductor. Another method is by magnetic coupling.

**Thyristor gate characteristics:**

- $V_g$ = +ve gate to cathode voltage.
- $I_g$ = +ve gate to cathode current.

As the gate cathode characteristic of a thyristor is a p-n junction, gate characteristic of the device is similar to diode.

Curve 1 the lowest voltage value s that must be applied to turn on the SCR.
Curve 2 highest possible voltage values that can be safely applied to get circuit.

\[ V_{gm} = \text{Maximum limit for gate voltage} \]

\[ I_{gm} = \text{Maximum limit for gate current} \]

\[ P_{gav} = \text{Rated gate power dissipation for each SCR} \]

These limits should not be crossed in order to avoid the permanent damage of the device junction \( J_3 \).

\( OY = \text{Minimum limit of gate voltage to turn ON} \)

\( OX = \text{minimum limit of gate current to turn ON} \)

If \( V_{gm}, I_{gm}, P_{gav} \) are exceeded the thyristor will damage so the preferred gate drive area of SCR is bcdefghb.

\( \text{oa} = \text{The non triggering gate voltage} \). If firing circuit generates +ve gate signal prior to the desired instant of triggering the SCR. It should be ensured that this unwanted signal should be less than the non–triggering voltage \( \text{oa} \).

\[ E_S = V_g + I_g R_S \]

\( E_S = \text{Gate source voltage} \)

\( V_g = \text{Gate cathode voltage} \)

\( I_g = \text{Gate current} \)

\( R_S = \text{Gate source resistance} \)

\( R_S = \text{The internal resistance of the trigger source} \)

\( R_I \) is connected across the gate cathode terminal, which provides an easy path to the flow of leakage current between SCR terminal. If \( I_{gmn}, V_{gmn} \) are the minimum gate current and gate voltage to turn ON the SCR.

\[ E_S = (I_{gmn} + V_{gmn} / R_I) R_S + V_{gmn} \]
UNIT-II

PHASE CONTROLLED CONVERTERS
RECTIFIER

Rectifier are used to convert A.C to D.C supply.

Rectifiers can be classified as single phase rectifier and three phase rectifier. Single phase rectifier are classified as 1-Φ half wave and 1-Φ full wave rectifier. Three phase rectifier are classified as 3-Φ half wave rectifier and 3-Φ full wave rectifier. 1-Φ Full wave rectifier are classified as 1-Φ mid point type and 1-Φ bridge type rectifier. 1-Φ bridge type rectifier are classified as 1-Φ half controlled and 1-Φ full controlled rectifier. 3-Φ full wave rectifier are again classified as 3-Φ mid point type and 3-Φ bridge type rectifier. 3-Φ bridge type rectifier are again divided as 3-Φ half controlled rectifier and 3-Φ full controlled rectifier.

Single phase half wave circuit with R-L load

Output current $i_o$ rises gradually. After some time $i_o$ reaches a maximum value and then begins to decrease.

At $\pi$, $v_o=0$ but $i_o$ is not zero because of the load inductance $L$. After $\pi$ interval SCR is reverse biased but load current is not less then the holding current.

At $\beta>\pi$, $i_o$ reduces to zero and SCR is turned off.

At $2\pi+\beta$ SCR triggers again

$\alpha$ is the firing angle.
\( \beta \) is the extinction angle.

\[ v = \beta - \alpha = \text{conduction angle} \]

Analysis for \( V_T \).

At \( \omega t = \alpha, V_T = V_m \sin \alpha \)

During \( \alpha \) to \( \beta, V_T = 0 \);

When \( \beta, V_T = V_m \sin \beta \),

\[ V_m \sin \omega t = Ri_o \quad \frac{di_0}{dt} \]

\[ i_s = \frac{V_m}{\sqrt{R^2 + X^2}} \sin(\omega t - \phi) \]

Where,

\[ \phi = \tan^{-1}\frac{X}{R} \]

\[ X = \omega L \]

Where \( \beta \) is the angle by which \( I_s \) lags \( V_s \).

The transient component can be obtained as

\[ Ri_t + L \frac{di_t}{dt} = 0 \]

So \( i_t = Ae^{-(R\alpha \omega)} \)

\[ i_0 = i_s + i_t \]

\[ \frac{V_m}{z} \sin(\omega t - \beta) + Ae^{-(R\alpha \omega)} \]

Where \( z = \sqrt{R^2 + X^2} \)

At \( \alpha = \omega t, i_0 = 0 \);

\[ 0 = \frac{V_m}{z} \sin(\beta - \beta) + Ae^{-(R\alpha \omega)}; \]

\[ A = -\frac{V_m}{z} \sin(\alpha - \beta) e^{(R\alpha \omega)} \]

\[ i = \frac{V_m}{z} \sin(\omega t - \beta) - \frac{V_m}{z} \sin(\alpha - \beta) e^{-(R\alpha \omega)} \]

\[ \frac{1}{z} \sin(\omega t - \beta) \]
Therefore,

\[ \omega t = \beta, \; i_0 = 0; \]

So \( \sin(\beta - \alpha) = \sin(\alpha - \beta) e^{-\pi(\beta - \alpha)/(\omega L)} \)

\( \beta \) can be obtained from the above equation.

The average load voltage can be given by

\[
V_0 = \frac{1}{2\pi} \int_{\alpha}^{\beta} V_m \sin \omega t d(\omega t)
\]

\[
\frac{V_m}{2\pi} \frac{\cos(\alpha) - \cos(\beta)}{2\pi}
\]

Average load current

\[
I_0 = \frac{V_m}{2\pi R} (\cos \alpha - \cos \beta)
\]

**Single phase full converter**

\[
V_0 = \frac{1}{\pi} \int_{\alpha}^{\pi+\beta} V_m \sin(\omega t) d(\omega t)
\]

\[
= \frac{2V_m \cos \alpha}{\pi}
\]

T1, T2 triggered at \( \alpha \) and \( \pi \) radian latter T3, T4 are triggered.
The minimum value of firing angle is
\[ V_m \sin(\omega t) = E \]

So,
\[ \theta_1 = \sin^{-1} \frac{E}{V_m} \]

Maximum value of firing angle
\[ \theta_2 = \pi - \theta_2 \]

The voltage differential equation is
\[ V_m \sin(\omega t) = Ri_0 + L \frac{di_0}{dt} + E \]

Due to source volt
\[ i_s = i_{s1} + i_{s2} \]

Due to DC counter emf
\[ i_{s1} = \frac{V_m}{Z} \sin(\omega t - \phi) \]
\[ i_{s2} = -(E / R) \]

\[ i_t = Ae^{-(Rt/L)t} \]

Thus the total current is given by

\[ i_t = i_1 + i_{s2} + i_i \]

\[ i_1 = \frac{V_m}{Z} \sin(\omega t - \phi) - \frac{E}{R} + Ae^{-(Rt/L)t} \]

\[ i_{s2} = \frac{V_m}{Z} \sin(\omega t - \phi) - \frac{E}{R} + Ae^{-(Rt/L)t} \]

At \( \omega t = \alpha \), \( i_0 = 0 \)

\[ A = \left[ \frac{E}{R} - \frac{V_m}{Z} \sin(\alpha - \phi) \right] e^{-R\alpha / L\omega} \]

So

\[ i_0 = \frac{V_m}{Z} \left[ \sin(\omega t - \phi) - \sin(\alpha - \phi) \right] e^{\frac{-R(\omega t - \alpha)}{L\omega}} - \frac{E}{R} \left[ 1 - e^{\frac{-R(\omega\alpha - \alpha)}{L\omega}} \right] \]

Average voltage across the inductance is zero. Average value of load current is

\[ I = \frac{1}{2\pi R} \int_{\alpha}^{\beta} (V \sin \omega t - E) \, d(\omega t) \]

\[ = \frac{1}{2\pi R} \left[ V \left( \cos \alpha - \cos \beta \right) - E(\beta - \alpha) \right] \]

Conduction angle \( \nu = \beta - \alpha \)

\[ \Rightarrow \beta = \alpha + \nu \]

\[ I_0 = \frac{1}{2\pi R} [V_m(\cos \alpha - \cos(\alpha + \nu)) - E(\nu)] \]

\[ \cos A - \cos B = 2 \sin \frac{A + B}{2} \sin \frac{A - B}{2} \]

So

\[ I_0 = \frac{1}{2\pi R} [2V_m \sin(\alpha + \frac{\nu}{2}) \sin \frac{\nu}{2} - E\nu] \]
\[ v = E + I_0 R \]

\[ = E + \frac{1}{2\pi} [2V_m \sin(\alpha + \frac{v}{2}) \sin \frac{v}{2} - E \cdot v] \]

\[ = E(1 - \frac{v}{2\pi}) + \frac{1}{\pi} \sin(\alpha + \frac{v}{2}) \sin \frac{v}{2} \]

If load inductance \( L \) is zero then

\[ \beta = \theta_2 \]

And \( v = \beta - \alpha = \theta_2 - \alpha \)

But \( \theta_2 = \pi - \theta_1 \)

So \( \beta = \theta_2 = \pi - \theta_1 \)

And \( v = \pi - \theta_1 - \alpha \)

So average current will be

\[ I_0 = \frac{1}{2\pi R} [V_m (\cos \alpha - \cos(\pi - \theta_2)) - E(\pi - \theta_2 - \alpha)] \]

So \( V_0 = E + I_0 R \)

\[ = \frac{V_m}{2\pi} (\cos \alpha + \cos \theta_2) + \frac{E}{\pi} (1 + \frac{\theta_2 + \alpha}{2}) \]

For no inductance rms value of load current

\[ I = \frac{1}{2\pi R^2} \int_0^{\pi/2} \sqrt{V_m^2 \sin^2(\omega t) - E^2} d(\omega t) \]

Power delivered to load

\[ P = I^2 R + I E \]

Supply power factor

\[ Pf = \frac{I^2 R + I E}{V_s I} \]

**Single phase full wave converter:**
\[ V = \frac{1}{\pi} \int_{\alpha}^{\pi} V \sin(\omega t) d(\omega t) \]
\[ = \frac{2V_m}{\pi} \sin \alpha \]

**Single phase semi converter:**

---

\[ V = \frac{1}{\pi} \int_{\alpha}^{\pi} V \sin(\omega t) d(\omega t) \]
\[ = \frac{V_m}{\pi} \cos \alpha \]

**Full converter:**
steady state analysis

\[ V = Ri + L \frac{di}{dt} + E \]

\[ V_0 = RI_0 + E \]

\[ V = \frac{2V_m \cos \alpha}{\pi} \]

So in case of DC motor load

\[ V_0 = r_a I_a + \omega_m \alpha_m \]

\[ \omega_m = \frac{2V_m \cos \alpha - r I}{\pi} \]

So

\[ T = \alpha_m I_a \]

\[ I_a = \frac{T}{\alpha_m} \]

\[ I_s = \frac{T}{\alpha_m} \]

Put

\[ \omega_m = \frac{\frac{2V_m}{\pi} \cos \alpha}{\frac{r_a T}{\alpha_m^2}} \]

So
UNIT-III

CHOPPERS AND REGULATORS
**CHOPPER**

A chopper is a static device that converts fixed DC input voltage to variable output voltage directly. Chopper are mostly used in electric vehicle, mini haulers.

Chopper are used for speed control and braking. The systems employing chopper offer smooth control, high efficiency and have fast response.

![Chopper Diagram](image)

The average output voltage is

\[ V_a = \frac{1}{T} \int_{0}^{T} V_o dt = \frac{1}{T} \int_{0}^{T_1} V_s(t) = f_1 V_s = \alpha V_s \]

The average load current

\[ I = \frac{V_a}{R} = \frac{\alpha V_s}{R} \]

Where, \( T \) = chopping period

Duty cycle of chopper =

\[ \alpha = \frac{t_1}{T} \]

f = chopping frequency

The rms value of output voltage is

\[ V = \left( \frac{1}{T} \int_{0}^{T} V_o^2 dt \right)^{\frac{1}{2}} = \alpha V \]

If we consider the converter to be loss less then the input power is equal to the output power and is given by
The effective input resistance seen by the P source is

\[ P = \frac{V_s}{I_s} = \frac{V_s}{\alpha V_s} = \frac{R}{\alpha} \]

The duty cycle \( \alpha \) can be varied by varying \( t_1, T \) of frequency.

**Constant frequency operation:**

1) The chopping period \( T \) is kept constant and on time is varied. The pulse width modulation, the width of the pulse is varied.

2) Variable frequency operation, the chopping frequency \( f \) is varied. Frequency modulation, either on time or off time is kept constant.

This type of control generate harmonics at unpredictable frequency and filter design is often difficult.

**TYPES OF CHOPPER:**

**FIRST QUADRANT OR TYPE A CHOPPER:**

When switch ON

\[ V_o = V_s. \]
Current $i_0$ flows in the same direction when switch off. $V_o=0$,

$i_0=0$

So, average value of both the load and the current are positive.

**SECOND QUADRANT OR TYPE B CHOPPER:**

![Diagram of Second Quadrant or Type B Chopper]

When switch are closed the load voltage $E$ drives current through $L$ and switch. During $T_{on}$ $L$ stores energy.

When switch off $V_0$ exceeds source voltage $V_i$.  

$$V_0 = E + L \frac{di}{dt}$$

Diode $D_2$ is forward biased. Power is fed back to supply. As $V_0$ is more than source voltage. So such chopper is called step up chopper.

$$V_0 = E + L \frac{di}{dt}$$

So current is always negative and $V_0$ is always positive.

**TWO QUADRANT TYPE A CHOPPER OR, TYPE C CHOPPER:**
Both the switches never switch ON simultaneously as it lead direct short circuit of the supply.

Now when sw2 is closed or FD is on the output voltage $V_o$ is zero. When sw1 is ON or diode D conducts output voltage is $V_o$ is $+V_s$.

CURRENT ANALYSIS: When CH1 is ON current flows along $i_o$. When CH1 is off current continues to flow along $i_o$ as FD is forward biased. So $i_o$ is positive.

Now when CH2 is ON current direction will be opposite to $i_o$. When sw2 is off D2 turns ON. Load current is $-i_o$. So average load voltage is always positive. Average load current may be positive or negative.

TWO QUADRANT TYPE B CHOPPER, OR TYPE D CHOPPER:
When CH1 and CH2 both are on then $V_0 = V_s$.

When CH1 and CH2 are off and D1 and D2 are on $V_0 = -V_s$.

The direction of current is always positive because chopper and diode can only conduct in the direction of arrow shown in fig.

Average voltage is positive when $T_{on} > T_{off}$

**FOUR QUADRANT CHOPPER, OR TYPE E CHOPPER**
FIRST QUADRANT:

CH4 is kept ON
CH3 is off
CH1 is operated
V₀ = Vₛ

i₀ = positive
when CH1 is off positive current free wheel through CH4, D2 so V₀
and I₂ is in first quadrant.

SECOND QUADRANT:

CH₁, CH₃, CH₄ are off.
CH₂ is operated.

Reverse current flows and Iₙ is negative through L, CH₂ D₄ and E. When CH₂
off D₁ and D₄ is ON and current id fed back to source. So

\[ E + L \frac{di}{dt} \] is more than source voltage Vₛ.

As i₀ is negative and V₀ is positive, so second quadrant operation. THIRD

QUADRANT:

CH₁ OFF, CH₂ ON

CH₃ operated. So both V₀ and i₀ is negative.

When CH₃ turned off negative current freewheels through CH₂ and D₄.

FOURTH QUADRANT:
CH4 is operated other are off.

Positive current flows through CH4 E L D2.

Inductance L stores energy when current fed to source through D3 and D2. \( V_0 \) is negative.

**STEADY STATE ANALYSIS OF PRACTICAL BUCK CHOPPER:**

The voltage across the inductor L is \( e_i = Li/dt \).

\[
V_a - V_s = L \frac{d}{dt} (i_2 - i_1) = L \frac{\Delta i}{t_1}
\]

\[
t_1 = \frac{\Delta i L}{V_a - V_s}
\]

The inductor current falls linearly from \( i_2 \) to \( i_1 \) in time \( t_2 \) as \( V_s = 0 \).

So

\[
-V_a = \frac{L(i_1 - i_2)}{t_2}
\]

If \( i_2 - i_1 = \Delta I \) then

\[
-V_a = -\frac{L\Delta I}{t_2}
\]

\[
t_2 = \frac{L\Delta I}{V_a}
\]

\( \Delta I = i_2 - i_1 \) = peak to peak ripple current.

\[
\Delta I = \frac{(V_s - V_a) t_1}{L} = \frac{V_s t_2}{L}
\]

Now \( t_1 = \alpha T \), \( t_2 = (1 - \alpha)T \)

\[
V = V_a t_1 = \frac{\alpha V}{T}
\]

\( \alpha < 1 \) so it is a step down or buck converter. If the circuit is lossless then \( V_s I_s = V_a I_a = \alpha V_s I_s = \alpha I_a \).

Now switching period \( T \) can be expressed as
\[ T = 1/f = t_1 + t_2 = \Delta I L / (V_s - V_a) + \Delta I L / (V_a) \]

\[ = \Delta I L V_s / V_a (V_s - V_a) \]

So peak to peak ripple current

\[ \Delta I = \frac{V_a (V_s - V_a)}{f L V_i} \]

\[ \Delta I = \frac{V_s \alpha (1 - \alpha)}{f L} \]

The peak to peak voltage of the capacitor is

\[ \Delta V_c = \frac{\Delta I}{8 f c} \]

So from above equation

\[ \Delta V_c = \frac{V_a (V_s - V_a) V_s \alpha (1 - \alpha)}{8 L cf^2 V_i} \]

**Condition for continuous inductor current and capacitor voltage:**

If \( I_L \) is the average inductor current

\[ \Delta I = 2I_L \] ....as

\[ V_a = \alpha V_s \]

\[ \frac{V_s \alpha (1 - \alpha)}{f L} = \]

\[ \frac{I_2 - I_1}{2} = I_L \]

As

\[ \Delta I = 2I_L \]

\[ \frac{V_s \alpha (1 - \alpha)}{f L} = 2I_L = 2I_a = \frac{2 \alpha V_s}{R} \] ....eq(4)
As $V_a = \alpha V_s$ so $I_a = \frac{\alpha V_s}{R}$

$$2I_a = \frac{2\alpha V_s}{R}$$

So equation 4 gives

$$L_c = \frac{(1-\alpha)R}{2f}$$

Which is the critical value of inductor

$$\Delta V_c = 2V_a$$

$$2V_a = \frac{V_a \alpha (1-\alpha)}{8LCf^2} = 2\alpha V_s$$

$$C = \frac{1-\alpha}{16Lf^2}$$

**Peak to peak ripple voltage of capacitor:**

$$\Delta V_c = V_c - V_c (t = 0)$$

$$= 1 \int I_a dt = \int_{c}^{a} I_a dt$$

$$= \int_{c}^{a} \left( \int_{c}^{a} - \int_{c}^{a} \right) dt$$

$$t_i = \frac{V_a - V_s}{V_{af}}$$

So

$$t_i = \frac{V_a - V_s}{V_{af}}$$

$$1 - \alpha = \frac{V_s}{V_a}$$

$$1 - \frac{t_i}{T} = \frac{V_s}{V_a}$$

$$\Rightarrow t_i = \frac{V_a - V_s}{V_{af}}$$

$$\Delta V_c = \frac{I_a}{C} \left( \frac{V_a - V_s}{V_{af}} \right)$$

So
\[ \Delta V_c = \frac{I_a \alpha}{f c} \]

**Condition for continuous inductor current and capacitor voltage:**

If \( I_L \) = average inductor current then

\[ I_L = \Delta I \]

\[ \Delta I = \frac{V_s \alpha}{f L} \]

\[ 2I_a = \frac{2V_s}{(1-\alpha)R} \]

\[ A_s = \frac{V_s}{1-\alpha} \]

\[ 2I_a = \frac{2V_s}{(1-\alpha)R} \]

\[ \Delta I = \frac{2V_s}{f L} \]

So

\[ L_c = \frac{\alpha (1-a) R}{2 f} \]

\[ \Delta V_c = 2V_a \]

\[ \frac{I_a \alpha}{f c} = \frac{2V_a}{2I R} \]

\[ c = \frac{\alpha}{2 f R} \]
UNIT-IV
INVERTERS
INVERTERS

The device that converts dc power into ac power at desired output voltage and frequency is called an inverter.

Single phase voltage source inverters

\[
V_o(rms) = \frac{1}{T_0} \int_0^{T_0} V_s(t) \, dt = \frac{V_s}{2}
\]

\[
V_o = \frac{a_0}{2} + \sum_{n=1}^{\infty} \left( a_n \cos(n\omega t) + b_n \sin(n\omega t) \right)
\]

Due to symmetry along x-axis

\[a_0 = 0, \quad a_n = 0\]

\[b_n = \frac{4V_S}{n\pi}\]

The instantaneous output voltage

\[v_o = \sum_{n=1,3,5...}^{\infty} \frac{2V_S}{n\pi} \sin(n\omega t)\]

\[= 0, \quad n=2,4,\ldots\]

The rms value of the fundamental output voltage

\[V_{01} = \frac{2V_S}{\sqrt{2\pi}} = 0.45V_s\]
So if $V_0 = \sum_{n=1,3,5\ldots}^{\infty} \frac{2V_S}{n\pi} \sin(n\omega t) = \sum_{n=1,3,5\ldots}^{\infty} \frac{2V_S}{n\pi \sqrt{R^2+(n\omega L)^2}} \sin(n\omega t - \theta_n)$

$P_{01} = (I_0)^2 R = \left[ \frac{2V_S}{\sqrt{2\pi \sqrt{R^2+(n\omega L)^2}}} \right]^2 R$

**DC Supply Current**

Assuming a lossless inverter, the ac power absorbed by the load must be equal to the average power supplied by the dc source.

$\int_0^T i(t) dt = \frac{1}{V_0} \int_0^{T_0} \sqrt{2} V_0 \sin(\omega t) \sqrt{2} I_0 \sin(\omega t - \theta_1) dt = S$

$V_{01}$ = Fundamental rms output voltage

$I_0$ = rms load current

$\theta_1$ = the load angle at the fundamental frequency Single phase full bridge inverter

\[ F_{01} = 1, V = \frac{4V_S}{\sqrt{2}V_S} = 0.9V \quad S \quad \text{(The rms of fundamental)} \]

Instantaneous load current $i_0$ for an RL load

$i_0 = \sum_{n=1,3,5\ldots}^{\infty} \frac{4V_S}{n\pi \sqrt{R^2+(n\omega L)^2}} \sin(n\omega t - \theta_n)$

$\theta_n = \tan^{-1} \left( \frac{n\omega L}{R} \right)$

The rms output voltage is

$V = \left( \int_0^{T_0} \left[ \int_0^S \frac{2V_S}{\sqrt{2}V_S} \right] dt \right)^{\frac{1}{2}} = S$
The instantaneous output voltage in a fourier series

\[ v_0 = \sum_{n=1,3,5\ldots}^{\infty} \frac{4V_S}{n\pi} \sin(n\omega t) \]

**Single phase bridge inverter**

![Single phase bridge inverter diagram]

**INVERTER**

Inverters are of the two types

1) VSI
2) CSI
   - Pulse width model

The VSI can be further divided into general 3 categories:

1. Pulse width modulated inverters
2. Square wave inverters
3. Single phase inverter with voltage cancellation
Pulse width modulated inverters

The input dc voltage is of constant magnitude. The diode rectifier is used to rectify the line voltage. The inverter control the magnitude and frequency of the ac output voltage.

This is achieved by PWM technique of inverter switches and this is called PWM inverters.

The sinusoidal PWM technique is one of the PWM technique to shape the output voltage to as close as sinusoidal output.

Basic concepts of switch mode inverter
During interval 1 $v_0$ and $i_0$ both are positive. During interval 3 $v_0$ and $i_0$ both are negative.

Therefore during 1 and 3 the instantaneous power flow is from dc side to corresponding to inverter mode of operation.

In contrast during interval 2 and 4 $v_0$ and $i_0$ are of opposite sign i.e. power flows from ac side to dc side corresponding to rectifier mode of operation.

**Pulse width modulated switching scheme**

We require the inverter output to be sinusoidal with magnitude and frequency controllable.

In order to produce sinusoidal output voltage at desired frequency a sinusoidal control signal at desired frequency is compared with a triangular waveform as show.

The frequency of the triangular waveform established the inverter switching frequency.

The triangular waveform is called carrier waveform. The triangular waveform establishes switching frequency $f_s$, which establishes with which the inverter switches are applied.

The control signal has frequency $f_s$ and is used to modulate the switch duty ratio.

$f_i$ is the desired fundamental frequency of the output voltage.

**The amplitude modulation ratio $m_a$ is defined as**

$$m = \frac{V_{control}}{V_{tri}}$$
$V_{\text{control}}$ is the peak amplitude of control signal.

$V_{\text{Tri}}$, peak amplitude of triangular signal. The frequency modulation ratio $m_f$.

$$m_f = \frac{f_s}{f_1}$$
When \( V_{\text{control}} > V_{\text{tri}} \)  
\[ T^+ \text{is ON} \quad V_{AO} = \frac{1}{2} V_d \]

When \( V_{\text{control}} < V_{\text{tri}} \)  
\[ T^- \text{is ON} \quad V_{AO} = \frac{1}{2} V_d \]

So the following inferences can be drawn

The peak amplitude of fundamental frequency is \( m_a \text{times} \frac{1}{2} V_d \)

\[ V_{AO} = m_a \frac{V_d}{2} \]

\[ V_{AO} = \frac{V_{\text{control}}}{V_{\text{tri}}} \times \frac{V_d}{2} \quad V_{\text{control}} \leq V_{\text{tri}} \]

The foregoing arguments show why \( V_{\text{control}} \) is chosen to be sinusoidal to provide sinusoidal output voltage with fewer harmonics.

Let the \( V_{\text{control}} \) vary sinusoidal with frequency \( f_1 \), which is the desired frequency of the inverter output voltage.

Let \( V_{\text{control}} = V_{\text{control}} \sin \omega_1 t \)

\[ V_{\text{control}} \leq V_{\text{tri}} \]
\[ v_{tri} = \frac{V_i}{t_1 \frac{T_s}{4}} \]

At \( t = t_1 \), \( v_{tri} = v_{control} \)

So
\[ \frac{v_{control}}{t_1} = \frac{V_i}{t_1 \frac{T_s}{4}} \]

\[ t_1 = \frac{v_{control} T_s}{V_i} \times 4 \]

\[ T_{on} = 2t_1 + \frac{T_s}{2} \]

\[ D_1 = \frac{2t_1 + T_s}{2T_s} \]

\[ D = 1 - \frac{1}{2} \frac{v_{control}}{V_i} \]

Three phase inverter

When three single-phase inverters are connected in parallel a three phase inverter is formed.

The gating signal has to be displaced by \( 120^\circ \) with respect to each other so as achieve three phase balanced voltages.

A 3-phase output can be achieved from a configuration of six transistors and six diodes.
Two type of control signal can be applied to transistors, they are such as $180^\circ$ or $120^\circ$ conduction.

180- degree conduction

When $Q_1$ is switched on, terminal $a$ is connected to the positive terminal of dc input voltage. When $Q_4$ is switched on terminal $a$ is brought to negative terminal of the dc source.

There are 6 modes of operation is a cycle and the duration of each mode is $60^\circ$.

The conduction sequence of transistors is $123, 234, 345, 456, 561, 612$. The gating signals are shifted from each other by $60^\circ$ to get 3-$\varphi$ balanced voltages.

Switching states for the three phase voltage inverters
Step I

(a) 0—60°; 5, 6, 1 closed.

Step II

(b) 60—120°; 6, 1, 2 closed.

Step III

(c) 120—180°; 1, 2, 3 closed.

Step IV

(d) 180—240°; 2, 3, 4 closed.
### Fourier Analysis

If we go for harmonic analysis \( V_{RY} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_{ys}}{n\pi} \sin\left(\frac{n\pi\theta}{3}\right) \)

### Table

<table>
<thead>
<tr>
<th>( V_{RN} )</th>
<th>( V_{YN} )</th>
<th>( V_{BN} )</th>
<th>( V_{RY} )</th>
<th>( V_{YB} )</th>
<th>( V_{BR} )</th>
<th>( V_1 )</th>
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<tr>
<td>( \frac{V}{3} )</td>
<td>(-\frac{2V}{3})</td>
<td>( \frac{V}{3} )</td>
<td>( V_{ac} )</td>
<td>(-V_{dc})</td>
<td>0</td>
<td>( \frac{2}{\sqrt{3}} )</td>
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<td>( V_{dc} )</td>
<td>0</td>
<td>(-V_{dc})</td>
<td>( \frac{2}{\sqrt{3}} )</td>
</tr>
<tr>
<td>( \frac{V}{3} )</td>
<td>(-\frac{2V}{3})</td>
<td>0</td>
<td>( V )</td>
<td>(-V)</td>
<td>( \frac{2}{\sqrt{3}} )</td>
<td></td>
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<tr>
<td>( \frac{2V}{3} )</td>
<td>(-\frac{V}{3})</td>
<td>(-V)</td>
<td>( V )</td>
<td>0</td>
<td>( \frac{2}{\sqrt{3}} )</td>
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<td>(-V)</td>
<td>0</td>
<td>0</td>
<td>( \frac{2}{\sqrt{3}} )</td>
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<tr>
<td>( \frac{V}{3} )</td>
<td>( \frac{2V}{3})</td>
<td>0</td>
<td>(-V)</td>
<td>0</td>
<td>( \frac{2}{\sqrt{3}} )</td>
<td></td>
</tr>
</tbody>
</table>
\[ V_{YB} = \sum_{n=1,3,5...}^{\infty} \frac{4V_S \sin \frac{n\pi}{3} \sin n(\omega t - \frac{\pi}{6})}{3} \]

\[ V_{BR} = \sum_{n=1,3,5...}^{\infty} \frac{4V_S \sin \frac{n\pi}{3} \sin n(\omega t - \frac{\pi}{6})}{3} \]

All even harmonics are zero and all triple \( n \) harmonics are zero.

The rms \( n \)th component of the line voltage is

\[ \frac{4V}{\sqrt{2}n\pi} \sin \frac{n\pi}{3} = \frac{4V}{\sqrt{2}n\pi} \sin(60) \]

For \( n=1 \)

\[ = 0.7797V_S \]

**Three phase 120° mode VSI**

The circuit diagram is the same as that for 180° mode of conduction.

Here each thyristor conducts for 120°. There are 6 steps each of 60° duration, for completing one cycle of ac output voltage.
Step I: 6, 1 conducting

\[ V_{an} = \frac{V_s}{2}, \quad V_{yn} = -\frac{V_s}{2}, \quad V_{cn} = 0 \]
**Step 2:** 1,2 conducting

\[ V_{an} = \frac{V_s}{2}, \quad V_{bn} = 0, \quad V_{cn} = -\frac{V_s}{2} \]

**Step 3:** 2,3 conducting

\[ V_{an} = 0, \quad V_{bn} = \frac{V_s}{2}, \quad V_{cn} = -\frac{V_s}{2} \]

**Step 4:** 3,4 conducting

\[ V_{an} = -\frac{V_s}{2}, \quad V_{bn} = \frac{V_s}{2}, \quad V_{cn} = 0 \]

**Step 5:** 4,5 conducting

\[ V_{an} = -\frac{V_s}{2}, \quad V_{yn} = 0, \quad V_{bn} = \frac{V_s}{2} \]

**Step 6:** 5,6 conducting

\[ V_{an} = 0, \quad V_{bn} = -\frac{V_s}{2}, \quad V_{cn} = \frac{V_s}{2} \]

<table>
<thead>
<tr>
<th>Step</th>
<th>Thyristor conducting</th>
<th>( V_{Rn} )</th>
<th>( V_{yn} )</th>
<th>( V_{Bn} )</th>
<th>( \vec{V} )</th>
</tr>
</thead>
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<td>1</td>
<td>6,1</td>
<td>( \frac{V_s}{2} )</td>
<td>( -\frac{V_s}{2} )</td>
<td>0</td>
<td>( \frac{\sqrt{3}V_s}{2} ) (-30°)</td>
</tr>
<tr>
<td>2</td>
<td>1,2</td>
<td>( \frac{V_s}{2} )</td>
<td>0</td>
<td>( -\frac{V_s}{2} )</td>
<td>( \frac{\sqrt{3}V_s}{2} ) (30°)</td>
</tr>
<tr>
<td>3</td>
<td>2,3</td>
<td>0</td>
<td>( \frac{V_s}{2} )</td>
<td>( -\frac{V_s}{2} )</td>
<td>( \frac{\sqrt{3}V_s}{2} ) (90°)</td>
</tr>
<tr>
<td>4</td>
<td>3,4</td>
<td>( -\frac{V_s}{2} )</td>
<td>( \frac{V_s}{2} )</td>
<td>0</td>
<td>( \frac{\sqrt{3}V_s}{2} ) (150°)</td>
</tr>
<tr>
<td>5</td>
<td>4,5</td>
<td>( -\frac{V_s}{2} )</td>
<td>0</td>
<td>( \frac{V_s}{2} )</td>
<td>( \frac{\sqrt{3}V_s}{2} ) (210°)</td>
</tr>
<tr>
<td>6</td>
<td>5,6</td>
<td>0</td>
<td>( -\frac{V_s}{2} )</td>
<td>( \frac{V_s}{2} )</td>
<td>( \frac{\sqrt{3}V_s}{2} ) (-30°)</td>
</tr>
</tbody>
</table>
UNIT-V

AC VOLTAGE CONTROLLERS

&

CYCLO CONVERTERS
This lesson provides the reader the following:

(i) AC-AC power conversion topologies at fixed frequency
(ii) Power converter options available for the conversion
(iii) Ability to formulate equations describing the current waveform for the PAC
(iv) Ability sketch the current waveform by observation of the circuit
(v) Ability to assess the performance of the converter of the topologies

Introduction

AC to AC voltage converters operates on the AC mains essentially to regulate the output voltage. Portions of the supply sinusoid appear at the load while the semiconductor switches block the remaining portions. Several topologies have emerged along with voltage regulation methods, most of which are linked to the development of the semiconductor devices.

![Fig 26.1 Some single phase AC-AC voltage regulator topologies. (a) Back-to-back SCR; (b) One SCR in (a) replaced by a four-diode full wave diode bridge; (c) A bi-directionally conducting TRIAC; (d) The SCR in (b) replaced by a transistor.](image)

The regulators in Fig 26.1 (a), (b) and (c) perform quite similarly. They are called Phase Angle Controlled (PAC) AC-AC converters or AC-AC choppers. The TRIAC based converter may be considered as the basic topology. Being bi-directionally conducting devices, they act on both polarities of the applied voltage. However, their ratings being poor, they tend to turn-on in the opposite direction just subsequent to their turn-off with an inductive load. The 'Alternistor' was developed with improved features but was not popular. The TRIAC is common only at the low power ranges. The (a) and (b) options are improvements on (c) mostly regarding current handling and turn-off-able current rating.

A transistorised AC-AC regulator is a PWM regulator similar to the DC-DC converters. It also requires a freewheeling path across the inductive load, which has also got to be bi-directional. Consequently, only controlled freewheeling devices can be used.
Operation with resistive loads

Fig. 26.2 illustrates the operation of the PAC converter with a resistive load. The device(s) is triggered at a phase-angle \( \alpha \) in each cycle. The current follows the voltage wave shape in each half and extinguishes itself at the zero crossings of the supply voltage. In the two-SCR topology, one SCR is positively biased in each half of the supply voltage. There is no scope for conduction overlap of the devices. A single pulse is sufficient to trigger the controlled devices with a resistive load. In the diode-SCR topology, two diodes are forward biased in each half. The SCR always receives a DC voltage and does not distinguish the polarity of the supply. It is thus always forward biased. The bi-directional TRIAC is also forward biased for both polarities of the supply voltage.

![Diagram of Operation of a Phase Angle Controlled AC-AC converter with a resistive load](image)

**Fig. 26.2 Operation of a Phase Angle Controlled AC-AC converter with a resistive load**

The rms voltage \( V_{\text{rms}} \) decides the power supplied to the load. It can be computed as

\[
V_{\text{rms}} = \sqrt{\frac{1}{\pi} \int_{\alpha}^{\pi/2} 2V \sin \omega t \, d\omega t}
\]

\[
= V \sqrt{1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}}
\]
As is evident from the current waveforms, the PAC introduces significant harmonics both into the load and the supply. This is one of the main reasons why such controllers are today not acceptable. The ideal waveform as shown in Fig 26.2 is half wave symmetric. However it is to be achieved by the trigger circuits. The controller in Fig. 26.4 ensures this for the TRIAC based circuit. While the TRIAC has a differing characteristic for the two polarities of biasing with the 32V DIAC - a two terminal device- triggering is effected when the capacitor voltage reaches 32 V. This ensures elimination of DC and even components in the output voltage.

For the SCR based controllers, identical comparators for the two halves of the AC supply, which generates pulses for the two SCRs ensures DC and even harmonic free operation.

The PAC operates with a resistive load for all values of $\alpha$ ranging from $0^\circ$ to $180^\circ$. The fundamental current, $i_f$ can be represented as

$$i_f = \frac{\sqrt{2}V}{R\pi} \left( -\frac{\alpha}{2} + \frac{\pi}{2} \right) \sin \omega t - \left( \frac{\pi - \alpha}{2} - \frac{\pi}{2} \right) \cos \omega t$$

In machine drives it is only the fundamental component, which is useful. However, in resistance heating type of application all harmonics are of no consequence. The corrupted supply...
current nevertheless is undesirable.
Power Factor

The power factor of a nonlinear deserves a special discussion. Fig. 26.2 shows the supply voltage and the non-sinusoidal load current. The fundamental load/supply current lags the supply voltage by the $\phi_1$, 'Fundamental Power Factor' angle. $\cos\phi_1$ is also called the 'Displacement Factor'. However this does not account for the total reactive power drawn by the system. This power factor is inspite of the actual load being resistive! The reactive power is drawn also by the trigger-angle dependent harmonics. Now

$$\text{power factor} = \frac{\text{average power}}{\text{apparent voltamperes}} = \frac{P}{VI_L}$$  \hspace{1cm} (26.2)

$$= \frac{VI_{L1}\cos\phi_1}{VI_L}$$  \hspace{1cm} (26.3)

$$\text{distortion factor} = \frac{I_{L1}}{I_L}$$

The Average Power, $P$ drawn by the resistive load is

$$P = \frac{1}{2\pi} \int_{0}^{2\pi} vi_L \omega dt = \frac{1}{2\pi} \int_{0}^{2\pi} V^2 \sin \omega t \omega dt$$

$$= \frac{2V^2}{R} \left[ \frac{\alpha}{\pi} \sin 2\alpha \right]_{R\pi}^{2\pi}$$

$$= \frac{2V^2}{R\pi} \left[ \frac{\alpha}{\pi} \sin 2\alpha \right]_{R\pi}^{2\pi}$$

The portion within square brackets in Eq. 26.5 is identical to the first part of the expression within brackets in Eq. 26.1, which is called the Fourier coefficient $B_1$. The rms load voltage can also be similarly obtained by integrating between $\alpha$ and $\pi$ and the result can be combined with Eq. 26.5 to give

$$\text{power factor} = \frac{\text{per – unit} \text{ rms load – current}}{\text{per – unit load power}}$$
Fig. 26.5 Variation of various performance parameters with triggering angle

\[ \frac{B_1}{p.u.} = \sqrt{B_1} \]

DISPLACEMENT FACTOR

DISTORTION FACTOR

AVERAGE POWER

\( \alpha \quad \Rightarrow \)
Operation with inductive loads

With inductive loads the operation of the PAC is illustrated in Fig 26.5. The current builds up from zero in each cycle. It quenches not at the zero crossing of the applied voltage as with the resistive load but after that instant. The supply voltage thus continues to be impressed on the load till the load current returns to zero. A single-pulse trigger for the TRIAC 26.1 (c) or the anti-parallel SCR (b) has no effect on the devices if it (or the anti-parallel device) is already in conduction in the reverse direction. The devices would fail to conduct when they are intended to, as they do not have the supply voltage forward biasing them when the trigger pulse arrives. A single pulse trigger will work till the trigger angle $\alpha > \phi$, where $\phi$ is the power factor angle of the inductive load. A train of pulses is required here. The output voltage is controllable only between triggering angles $\phi$ and 180°.

The load current waveform is further explained in Fig. 26.6. The current is composed of two components. The first is the steady state component of the load current, $i_{ss}$ and the second, $i_{tr}$ is the transient component.

Fig. 26.6 Operation of a single phase PAC with an inductive load

Fig 26.7 Load current for a single phase AC-AC converter with a R_L load. $V_s$ - supply voltage, $i_{ss}$ - steady state current component, $i_{tr}$ - transient current component and $i_{load}$ - load current ($= i_{ss} + i_{tr}$).
With an inductance in the load the distinguishing feature of the load current is that it must always start from zero. However, if the switch could have permanently kept the load connected to the supply the current would have become a sinusoidal one phase shifted from the voltage by the phase angle of the load, $\phi$. This current restricted to the half periods of conduction is called the 'steady-state component' of load current $i_{ss}$. The 'transient component' of load current $i_{tr}$, again in each half cycle, must add up to zero with this $i_{ss}$ to start from zero. This condition sets the initial value of the transient component to that of the steady state at the instant that the SCR/TRIAC is triggered. Fig. 26.6 illustrates these relations.

When a device is in conduction, the load current is governed by the equation

$$L \frac{di}{dt} + Ri = v_s$$

$$i_{load} = \frac{\sqrt{2}V}{Z} \left[ \sin \alpha - \phi + \sin (\alpha - \phi) e^{-\frac{R}{L} (t - \alpha - \phi)} \right]$$

Since at $t = 0$, $i_{load} = 0$ and supply voltage $v_s = \sqrt{2}V \sin \omega t$ the solution is of the form

The instant when the load current extinguishes is called the extinction angle $\beta$. It can be inferred that there would be no transients in the load current if the devices are triggered at the power factor angle of the load. The load current $I$ that case is perfectly sinusoidal.

**AC-AC Chopper**

![AC-AC Chopper diagram](image)

**Fig. 26.8** A complete Transistorised AC-AC chopper topology of the version shown in Fig. 26.1 and the corresponding load voltage and current waveforms for an inductive load. The output voltage is shown to be about 50% for a 0.5 Duty Ratio chopping.

The AC-AC converter shown in Fig 26.1 has to be augmented with two additional controlled devices clamping the load as indicated in Fig. 26.7. A large capacitor across the supply terminals is also to be inserted. These devices which are mostly transistors of the same variety as used for the chopper are necessary to clamp the voltages generated by the switching-off of the current carrying inductors in the load while the input capacitor takes care of the line inductances. The harmonics in the line current and load voltage waveforms are significantly different from those with the PACs. Mostly switching frequency harmonics are present in both the waveforms.
PAC as a static switch

Both single phase and three phase PACs are often used as static switches for applications like switching on of highly inductive loads without transients or for regulating output AC voltages by switching in tapings of a transformer. Such sequence control PACs while controlling the output voltage also permit improvement of the power factor as seen by the source. Sequence control can be two or multiple phase depending upon the application. Typical load voltage and current waveforms are shown in Fig. 26.8. The outer TRIACs connected to the higher voltage leads of the input transformer are triggered at the desired angle $\alpha$, to realize the required load voltage. Obviously this voltage is greater than that available at the low voltage terminal of the transformer. This device continues conduction into the next half of the supply voltage till the load current falls to zero. The inner TR$_2$ starts conduction subsequently, requiring a wide pulse or a train of pulses. TR$_1$ can be however triggered by a single pulse.

![Fig. 26.9 Load voltage and current control with a two-stage sequence control](image)

Practice Questions and Problems with Answers

**Q1** A single-phase transformer, assumed to have a negligible resistance compared to its inductance is switched on via a PAC. At what trigger angle will the operation be free from transients?

**A1** For the transformer load $\phi_L \approx 90^\circ$

Therefore for transient free operation $\alpha = 90^\circ$

**Q2** For the load described in Q1, the PAC is triggered by a single pulse at $\alpha = 60^\circ$. Sketch the load current waveform.
A2 Since $\alpha < \phi_L$, the load current should have been continuous. However, the current in the SCR first triggered extinguishes at a $\beta$ the total load current, $i_L = i_{ss} + i_{tr} = 0$. For this load which can be considered to be highly inductive $\beta \approx 360^\circ$, say $\approx 360^\circ$. Thus the first SCR conducts till that angle. The anti-parallel SCR is triggered at $\alpha = 60^\circ$ corresponding to a $\beta \approx 180 + 60 = 240^\circ$ when it is still reverse biased. It fails to conduct. The load thus sees only a unipolar current. The load current and voltage waveforms are illustrated in Fig 26. A2. Note that both the load voltage and current waveforms contain DC components.

![Fig. 26. A2 The load current waveform and its steady-state and transient components when a highly inductive load is switched using single narrow trigger pulses.](image-url)
CYCLO CONVERTERS
Instructional Objectives

Study of the following:

- The cyclo-converter circuits – basic principle of operation
- The circuit for the single-phase to single-phase cyclo-converter using thyristors
- The operation of the above cyclo-converter circuit, along with the voltage waveforms

Introduction

Earlier in the last three (4.1-4.3) lessons (first half) of this module, the circuit and operation of ac to ac voltage controllers – both single-phase and three-phase, were described in detail. The devices used are either triac, or thyristors connected back to back. In this lesson (4.4) – first one in the second half of this module, the cyclo-converter is introduced as a type of power controller, where an alternating voltage at supply frequency is converted directly to an alternating voltage at load frequency (normally lower), without any intermediate dc stage. As will be shown in the last (fifth) module, an alternating voltage at any frequency (output) is obtained using an inverter as a power controller from a dc voltage fed at its input. This input, i.e. dc voltage, is again obtained using a rectifier (converter) with ac voltage (normally at supply frequency) fed at its input. This type has been described in module 2. Note that this is a two-stage process with an intermediate dc stage. Now-a-days, the power switching devices used in the inverter circuit belong to transistor family (termed as self-commutated ones), starting with power transistors, whereas thyristors are still being used in the converter (rectifier) circuits. These devices are called force-commutated ones, when used in dc chopper circuits (described in module 3), but in this case, i.e. converter circuits, line commutation takes place. As stated earlier, the output frequency of the cyclo-converter is limited to about one-third of supply (line) frequency of 50 Hz.

Initially, the basic principle of operation used in a cyclo-converter is discussed. Then, the circuit of a single-phase to single-phase cyclo-converter using thyristors is presented. This is followed by describing the operation of the above cyclo-converter circuit, along with voltage waveforms. The readers at this stage, have gone through the following lessons – single-phase fully controlled converter using thyristors, for obtaining dc output voltage from ac supply (#2.2), and ac to ac voltage controllers – both single-phase and three-phase, using either triac, or thyristors connected back to back (#4.1-4.3). In the above cases, the output voltage obtained is, in the form of phase-controlled one, as can be observed from the waveforms shown in the above lessons. In the present case, the output voltage of the cyclo-converter circuit (single-phase) using thyristors, is synthesized from the above phase-controlled voltage waveforms, so as to obtain an ac waveform (output) of low frequency, with the input being an ac voltage of higher frequency, say line. The angle, at which the thyristors are triggered, is controlled to obtain the desired waveform.

Keywords: Single-phase to single-phase cyclo-converter using thyristors, Voltage waveforms.

Cyclo-converter

Basic Principle of Operation
The basic principle of operation of a cyclo-converter is explained with reference to an equivalent circuit shown in Fig. 29.1. Each two-quadrant converter (phase-controlled) is
represented as an alternating voltage source, which corresponds to the fundamental voltage component obtained at its output terminals. The diodes connected in series with each voltage source, show the unidirectional conduction of each converter, whose output voltage can be either positive or negative, being a two-quadrant one, but the direction of current is in the direction as shown in the circuit, as only thyristors – unidirectional switching devices, are used in the two converters. Normally, the ripple content in the output voltage is neglected.

\[ P = E_m \sin \omega_o t \]

\[ e_P = E_m \sin \omega_o t \]

\[ e_N = E_m \sin \omega_o t \]

Fig. 29.1: Equivalent circuit of cycloconverter

The control principle used in an ideal cyclo-converter is to continuously modulate the firing angles of the individual converters, so that each produces the same sinusoidal (ac) voltage at its output terminals. Thus, the voltages of the two generators (Fig. 29.1) have the same amplitude, frequency and phase, and the voltage of the cyclo-converter is equal to the voltage of either of these generators. It is possible for the mean power to flow either ‘to’ or ‘from’ the output terminals, and the cyclo-converter is inherently capable of operation with loads of any phase angle – inductive or capacitive. Because of the uni-directional current carrying property of the individual converters, it is inherent that the positive half-cycle of load current must always be carried by the positive converter, and the negative half-cycle by the negative converter, regardless of the phase of the current with respect to the voltage. This means that each two-quadrant converter operates both in its rectifying (converting) and in its inverting region during the period of its associated half-cycle of current.

The output voltage and current waveforms, illustrating the operation of an ideal cyclo-converter circuit with loads of various displacement angles, are shown in Fig. 29.2. The displacement angle of the load (current) is 0° (Fig. 29.2a). In this case, each converter carries the load current only, when it operates in its rectifying region, and it remains idle throughout the whole period in which its terminal voltage is in the inverting region of operation. In Fig. 29.2b, the displacement angle of the load is 60° lagging. During the first 120° period of each half-cycle of load current, the associated converter operates in its rectifying region, and delivers...
power to the load. During the latter 60° period in the half-cycle, the associated converter
operates in its inverting region, and under this condition, the load is regenerating power back into the cyclo-converter output terminals, and hence, into the ac system at the input side. These two are illustrative cases only. Any other case, say capacitive load, with the displacement angle as leading, the operation changes with inverting region in the first period of the half-cycle as per displacement angle, and the latter period operating in rectifying region. This is not shown in Fig. 29.2, which can be studied from a standard text book.
Single-phase to Single-phase Cyclo-converter

The circuit of a single-phase to single-phase cyclo-converter is shown in Fig. 29.3. Two full-wave fully controlled bridge converter circuits, using four thyristors for each bridge, are connected in opposite direction (back to back), with both bridges being fed from ac supply (50 Hz). Bridge 1 (P – positive) supplies load current in the positive half of the output cycle, while bridge 2 (N – negative) supplies load current in the negative half. The two bridges should not conduct together as this will produce short-circuit at the input. In this case, two thyristors come in series with each voltage source. When the load current is positive, the firing pulses to the thyristors of bridge 2 are inhibited, while the thyristors of bridge 1 are triggered by giving pulses at their gates at that time. Similarly, when the load current is negative, the thyristors of bridge 2 are triggered by giving pulses at their gates, while the firing pulses to the thyristors of bridge 1 are inhibited at that time. This is the circulating-current free mode of operation. Thus, the firing angle control scheme must be such that only one converter conduct at a time, and the change over of firing pulses from one converter to the other, should be periodic according to the output frequency. However, the firing angles the thyristors in both converters should be the same to produce a symmetrical output.

![Circuit Diagram](image)

**Fig. 29.3: Single-phase to single-phase cycloconverter (using thyristor bridges)**

When a cyclo-converter operates in the non-circulating current mode, the control scheme is complicated, if the load current is discontinuous. The control is somewhat simplified, if some amount of circulating current is allowed to flow between them. In this case, a circulating current limiting reactor is connected between the positive and negative converters, as is the case with dual converter, i.e. two fully controlled bridge converters connected back to back, in circulating-current mode. The readers are requested to refer to any standard text book. This circulating current by itself keeps both converters in virtually continuous conduction over the whole control range. This type of operation is termed as the circulating-current mode of operation. The operation of the cyclo-converter circuit with both purely resistive (R), and inductive (R-L) loads is explained.
Resistive (R) Load: For this load, the load current (instantaneous) goes to zero, as the input voltage at the end of each half cycle (both positive and negative) reaches zero (0). Thus, the
conducting thyristor pair in one of the bridges turns off at that time, i.e. the thyristors undergo natural commutation. So, operation with discontinuous current (Fig. 29.4) takes place, as current flows in the load, only when the next thyristor pair in that bridge is triggered, or pulses are fed at respective gates. Taking first bridge 1 (positive), and assuming the top point of the ac supply as positive with the bottom point as negative in the positive half cycle of ac input, the odd-numbered thyristor pair, P₁ & P₃ is triggered after phase delay (α₁), such that current starts flowing through the load in this half cycle. In the next (negative) half cycle, the other thyristor pair (even-numbered), P₂ & P₄ in that bridge conducts, by triggering them after suitable phase delay from the start of zero-crossing. The current flows through the load in the same direction, with the output voltage also remaining positive. This process continues for one more half cycle (making a total of three) of input voltage (f₁ = 50 Hz). From three waveforms, one combined positive half cycle of output voltage is produced across the load resistance, with its frequency being one-third of input frequency (f₂ = f₁ / 3 = 16 2/3 Hz). The following points may be noted.

The firing angle (α) of the converter is first decreased, in this case for second cycle only, and then again increased in the next (third) cycle, as shown in Fig. 29.4b. This is, because only three cycles for each half cycle is used. If the output frequency needed is lower, the number of cycles is to be increased, with the firing angle decreasing for some cycles, and then again increasing in the subsequent cycles, as described earlier.

![Diagram of input and output voltage waveforms](image)

**Fig. 29.4:** Input (a) and output (b) voltage waveforms of a cycloconverter with an output frequency of 16 2/3 Hz for resistive (R) load

To obtain negative output voltage, in the next three half cycles of input voltage, bridge 2 is used. Following same logic, if the bottom point of the ac supply is taken as positive with the top point as negative in the negative half of ac input, the odd-numbered thyristor pair, N₁ & N₃ conducts, by triggering them after suitable phase delay from the zero-crossing. Similarly, the even-numbered thyristor pair, N₂ & N₄ conducts in the next half cycle. Both the output voltage and current are now negative. As in the previous case, the above process also continues for three consecutive half cycles of input voltage. From three waveforms, one combined negative half cycle of output voltage is produced, having same frequency as given earlier. The pattern of firing

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angle – first decreasing and the increasing, is also followed in the negative half cycle. One positive half cycle, along with one negative half cycle, constitute one complete cycle of output.
(load) voltage waveform, its frequency being $16\frac{2}{3}$ Hz as stated earlier. The ripple frequency of
the output voltage/ current for single–phase full-wave converter is 100 Hz, i.e., double of the
input frequency. It may be noted that the load (output) current is discontinuous (Fig. 29.4c), as
also load (output) voltage (Fig. 29.4b). The supply (input) voltage is shown in Fig. 29.4a. Only
one of two thyristor bridges (positive or negative) conducts at a time, giving non-circulating
current mode of operation in this circuit.

**Inductive (R-L) Load:** For this load, the load current may be continuous or discontinuous
depending on the firing angle and load power factor. The load voltage and current waveforms are
shown for continuous and discontinuous load current in Fig. 29.5 and 29.6 respectively.

![Fig. 29.5: Input (a) and output (b) voltage, and current
(c) waveforms for a cyclo-converter with discontinuous](image)

Fig. 29.6: Input (a) and output (b) voltage, and current (c, d) waveforms for a cyclo-converter with continuous load current.

(a) Discontinuous load current

The load current in this case is discontinuous, as the inductance, L, in series with the resistance, R, is low. This is somewhat similar to the previous case, but difference also exists as described. Here, also non-circulating mode of operation takes place, with only one of the bridges − #1 (positive), or #2 (negative), conducting at a time, but two bridges do not conduct at the same time, as this will result in a short circuit. In this case, the output frequency is assumed as \( f_2 = 12.5 \text{ Hz} \), the input frequency being same as \( f_1 = 50 \text{ Hz} \), i.e., \( f_1 = 4 \cdot f_2 \), or \( f_2 = f_1 / 4 \). So, four positive half cycles, or two full cycles of the input to the full-wave bridge converter (#1), are required to produce one positive half cycle of the output waveform, as the output frequency is one-fourth of the input frequency as given earlier. As in the previous case with resistive load, taking bridge 1, and assuming the top point of the ac supply as positive, in the positive half cycle of ac input, the odd-numbered thyristor pair, P₁ & P₃, is triggered after phase
delay ($\theta = \omega t = \alpha_1$), such that current starts flowing the inductive load in this half cycle. But
here, the current flows even after the input voltage has reversed (after \( \theta = \pi \)), till it reaches zero at \((\theta = \beta_1)\) with \((\pi + \alpha_2) > \beta_1 > \pi\), due to inductance being present in series with resistance, its value being low. It may be noted that the thyristor pair is, thus, naturally commutated. In the next (negative) half cycle, the other thyristor pair (even-numbered), \(P_2\) & \(P_4\), is triggered at \((\pi + \alpha_2)\).

The current flows through the load in the same direction, with the output voltage also remaining positive. The current goes to zero at \((\pi + \beta_2)\), with \((\pi + \alpha_3) > \beta_2 > \pi\). This procedure continues for the next two half cycles, making a total of four positive half cycles. From these four waveforms, one combined positive half cycle of output voltage is produced across the inductive load. The firing angle \((\alpha)\) of the converter is first decreased, in this case for second half cycle only, kept nearly same in the third one, and finally increased in the last (fourth) one, as shown in Fig. 29.5b.

To obtain negative output voltage, in the next four half cycles of output voltage, bridge 2 is used. Following same logic, if the bottom point of the ac supply is taken as positive in the negative half of ac input, the odd-numbered thyristor pair, \(N_1\) & \(N_3\) conducts, by triggering them after phase delay \((\theta = 4 \cdot \pi + \alpha_1)\). The current flows now in the opposite (negative) direction through the inductive load, with the output voltage being also negative. The current goes to zero at \((4 \cdot \pi + \beta_1)\), due to load being inductive as given earlier. Similarly, the even-numbered thyristor pair, \(N_2\) & \(N_4\) conducts in the next half cycle, after they are triggered at \((5 \cdot \pi + \alpha_2)\). The current goes to zero at \((5 \cdot \pi + \beta_2)\). Both the output voltage and current are now negative. As in the previous case, the above process also continues for two more half cycles of input voltage, making a total of four. From these four waveforms, one combined negative half cycle of output voltage is produced with same output frequency. The pattern of firing angle – first decreasing and then increasing, is also followed in the negative half cycle. It may be noted that the load (output) current is discontinuous (Fig. 29.5c), as also load (output) voltage (Fig. 29.5b). The supply (input) voltage is shown in Fig. 29.5a. One positive half cycle, along with one negative half cycle, constitute one complete cycle of output (load) voltage waveform, its frequency being 12.5 Hz as stated earlier. The ripple frequency remains also same at 100 Hz, with the ripple in load current being filtered by the inductance present in the load.

(b) Continuous load current

As given above, the load current is discontinuous, as the inductance of the load is low. If the inductance is increased, the current will be continuous. Most of the points given earlier are applicable to this case, as described. To repeat, non-circulating mode of operation is used, i.e., only one of the bridges – #1 (positive), or #2 (negative), conducts at a time, but two bridges do not conduct at the same time, as this will result in a short circuit. Also, the ripple frequency in the voltage and current waveforms remains same at 100 Hz. The output frequency is one-fourth of input frequency (50 Hz), i.e., 12.5 Hz. So, for each half-cycle of output voltage waveform, four half cycles of input supply are required. Taking bridge 1, and assuming the top point of the ac supply as positive, in the positive half cycle of ac input, the odd-numbered thyristor pair, \(P_1\) & \(P_3\), is triggered after phase delay \((\theta = \omega t = \alpha_1)\), such that current starts flowing the inductive load in this half cycle. But here, the current flows for about one complete half cycle, i.e., up to the angle, \((\pi + \alpha_1)\) or \((\pi + \alpha_2)\), whichever is higher, even after the input voltage has reversed, due to the high value of load inductance. In the next (negative) half cycle, the other thyristor pair (even-numbered), \(P_2\) & \(P_4\), is triggered at \((\pi + \alpha_2)\). At that time, reverse voltage is applied across
each of the conducting thyristors, \( P_1/P_3 \), and the thyristors turn off. The current flows through the load in the same direction, with the output voltage also remaining positive. Also, the current
flows for about one complete half cycle, i.e., up to the angle, $(\pi + \alpha_2)$ or $(\pi + \alpha_3)$, whichever is higher. This procedure continues for the next two half cycles, making a total of four positive half cycles. From these four waveforms, one combined positive half cycle of output voltage is produced across the inductive load. The firing angle ($\alpha$) of the converter is first decreased, in this case for second half cycle only, kept nearly same in the third one, and finally increased in the last (fourth) one, as shown in Fig. 29.6b.

To obtain negative output voltage, in the next four half cycles of output voltage, bridge 2 is used. Following same logic, if the bottom point of the ac supply is taken as positive in the negative half of ac input, the odd-numbered thyristor pair, $N_1$ & $N_3$ conducts, by triggering them after phase delay ($\theta = 4 \cdot \pi + \alpha_i$). The current flows now in the opposite (negative) direction through the inductive load, with the output voltage being also negative. The current flows for about one complete half cycle, i.e., up to the angle, $(5 \cdot \pi + \alpha_1)$ or $(5 \cdot \pi + \alpha_2)$, whichever is higher, as the load is inductive. Similarly, the even-numbered thyristor pair, $N_2$ & $N_4$ conducts in the next half cycle, after they are triggered at $(5 \cdot \pi + \alpha_2)$. As described earlier, both the conducting thyristors turn off, as reverse voltage is applied across each of them. Both the output voltage and current are now negative. Also, the current flows for about one complete half cycle, i.e. up to the angle, $(5 \cdot \pi + \alpha_2)$ or $(5 \cdot \pi + \alpha_3)$, whichever is higher. As in the previous case, the above process also continues for two more half cycles of input voltage, making a total of four. From these four waveforms, one combined negative half cycle of output voltage is produced with same output frequency of 12.5 Hz. The pattern of firing angle – first decreasing and then increasing, is also followed in the negative half cycle. It may be observed that the load (output) current is continuous (Fig. 29.6c), as also load (output) voltage (Fig. 29.6b). The load (output) current is redrawn in Fig. 29.6d, under steady state condition, while the supply (input) voltage is shown in Fig. 29.6a. One positive half cycle, along with one negative half cycle, constitute one complete cycle of output (load) voltage waveform.

**Advantages and Disadvantages of Cyclo-converter**

**Advantages**

1. In a cyclo-converter, ac power at one frequency is converted directly to a lower frequency in a single conversion stage.

2. Cyclo-converter functions by means of phase commutation, without auxiliary forced commutation circuits. The power circuit is more compact, eliminating circuit losses associated with forced commutation.

3. Cyclo-converter is inherently capable of power transfer in either direction between source and load. It can supply power to loads at any power factor, and is also capable of regeneration over the complete speed range, down to standstill. This feature makes it preferable for large reversing drives requiring rapid acceleration and deceleration, thus suited for metal rolling application.

4. Commutation failure causes a short circuit of ac supply. But, if an individual fuse blows off, a complete shutdown is not necessary, and cyclo-converter continues to function with somewhat distorted waveforms. A balanced load is presented to the ac supply with unbalanced output conditions.
5. Cyclo-converter delivers a high quality sinusoidal waveform at low output frequencies, since it is fabricated from a large number of segments of the supply waveform. This is often preferable for very low speed applications.

6. Cyclo-converter is extremely attractive for large power, low speed drives.

### Disadvantages

1. Large number of thyristors is required in a cyclo-converter, and its control circuitry becomes more complex. It is not justified to use it for small installations, but is economical for units above 20 kVA.

2. For reasonable power output and efficiency, the output frequency is limited to one-third of the input frequency.

3. The power factor is low particularly at reduced output voltages, as phase control is used with high firing delay angle.

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**Fig. 29.7: DC link converter**

The cyclo-converter is normally compared with dc link converter (Fig. 29.7), where two power controllers, first one for converting from ac input at line frequency to dc output, and the second one as inverter to obtain ac output at any frequency from the above dc input fed to it. The thyristors, or switching devices of transistor family, which are termed as self-commutated ones, usually the former, which in this case is naturally commutated, are used in controlled converters (rectifiers). The diodes, whose cost is low, are used in uncontrolled ones. But now-a-days, switching devices of transistor family are used in inverters, though thyristors using forced commutation are also used. A diode, connected back to back with the switching device, may be a power transistor (BJT), is needed for each device. The number of switching devices in dc link converter depends upon the number of phases used at both input and output. The number of devices, such as thyristors, used in cyclo-converters depends on the types of connection, and also the number of phases at both input and output. It may be noted that all features of a cyclo-converter may not be available in a dc link converter. Similarly, certain features, like Pulse Width Modulation (PWM) techniques as used in inverters and also converters, to reduce the harmonics in voltage waveforms, are not applied in cyclo-converters. The various circuits used and their operational aspects are discussed in detail in the next (last) module (#5) on DC to AC Converters termed as Inverters.

### Advantages and Disadvantages of DC Link Converter

#### Advantages

1. The output frequency can be varied from zero to rated value, with the upper frequency limit,
being decided by the turn-off time of the switching devices, which is quite low due to the use of transistors in recent time.
2. The control circuit here is simpler, as compared to that used in cyclo-converter.

3. It has high input power factor, if diode rectifier is used in the first stage. If phase-controlled thyristor converter is used, power factor depends upon phase angle delay.

4. It is suitable for higher frequencies, as given earlier.

**Disadvantages**

1. The conversion is in two stages, using two power controllers – one as converter and other as inverter, as stated earlier.

2. Forced commutation is required for the inverter, if thyristors are used, even though phase control is used in converter, where natural commutation takes place.

3. The feature of regeneration is somewhat difficult, and also is involved to incorporate in a dc link converter.

4. The output waveform of the inverter is normally a stepped one, which may cause non-uniform rotation of an ac motor at very low frequencies (< 10 Hz). The distorted waveform also causes system instability at low frequencies. This can be reduced by using PWM technique as given earlier.

In this lesson, the first one in the second half of this module (#4), the cyclo-converter is first introduced, along with the basic principle of operation. The circuit and the operation of single-phase to single-phase cyclo-converter, with both resistive and inductive loads, are described in detail, with voltage and current waveforms. The current is discontinuous, with resistive and inductive (with low value of inductance) loads, but can be continuous, if the inductance is higher. In the next lesson, the circuit and operation of three-phase to single-phase cyclo-converter, followed by three-phase to three-phase one, will be described in detail.