ELECTRONIC DEVICES & CIRCUITS

(20A04101P)

LAB MANUAL

I – B.TECH

Prepared by

Dr.G.Elayaraja

Department of Electronics & Communication Engineering

VEMU INSTITUTE OF TECHNOLOGY

(Approved by AICTE, New Delhi and Affiliated to JNTUA, Ananthapuramu)
Accredited by NAAC, NBA (EEE , ECE & CSE) & ISO 9001-2015 Certified Institution
Near Pakala. P. Kothakota, Chittoor-Tirupati Highway
Chittoor, Andhra Pradesh -517112
Website: *www.vemu.org*

Course Code	Electronic Devices & Circuits	L	T	P	C
20A04101P		0	0	3	1.5

Course Objectives

- To verify the theoretical concepts practically from all the experiments
- To analyse the characteristics of Diodes, BJT, MOSFET, UJT.
- To design the amplifier circuits from the given specifications.
- To Model the electronic circuits using tools such as PSPICE/Multisim.

Course outcomes (CO) : After completion of the course, the student can able to

CO-1: Understand the basic characteristics by plotting graphs and applications of basic electronic devices

CO-2: Analyze the Characteristics of UJT, BJT, FET, and SCR

CO-3: Design FET based amplifier circuits/BJT based amplifiers for the given specifications

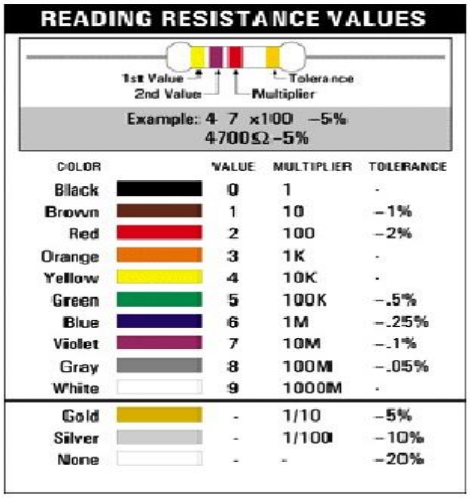
CO-4: Analyze all Electronic Circuits by Simulating in Multisim/Pspice.

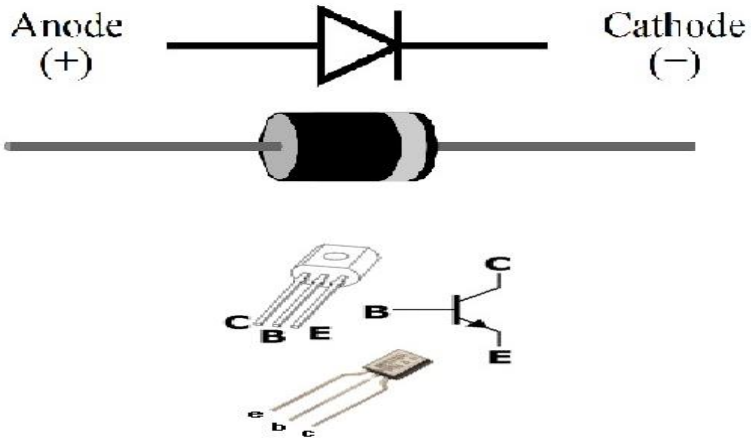
LIST OF EXPERIMENTS

1. V-I CHARACTERISTICS OF PN JUNCTION DIODE.
2. FULL WAVE RECTIFIER.
3. CLIPPING AND CLAMPER.
4. ZENER DIODE AS VOLTAGE REGULATOR.
5. COMMON SOURCE CONFIGURATION USING MOSFET.
6. COMMON SOURCE CONFIGURATION USING JFET.
7. COMMON EMITTER CONFIGURATION USING BJT.
8. COMMON BASE CONFIGURATION USING BJT.
9. VOLT -AMPERE CHARACTERISTICS OF UJT.
10. TRANSISTOR AS A SWITCH USING BJT.
11. COMMON SOURCE AMPLIFIER USING MOSFET.

12. COMMON EMITTER AMPLIFIER USING BJT
13. V-I CHARACTERISTICS OF PN JUNCTION DIODE.
14. FULL WAVE RECTIFIER.
15. CLIPPING AND CLAMPER.
16. ZENER DIODE AS VOLTAGE REGULATOR.
17. COMMON SOURCE CONFIGURATION USING MOSFET.
18. COMMON SOURCE CONFIGURATION USING JFET.
19. COMMON EMITTER CONFIGURATION USING BJT.
20. COMMON BASE CONFIGURATION USING BJT.
21. VOLT -AMPERE CHARACTERISTICS OF UJT.
22. TRANSISTOR AS A SWITCH USING BJT.
23. COMMON SOURCE AMPLIFIER USING MOSFET.
24. COMMON EMITTER AMPLIFIER USING BJT
25. UJT RELAXIATION OSCILLATOR
26. IMPLEMENTATION OF LOGIC GATES USING DIODE AND TRANSISTOR

ELECTRONIC DEVICES & CIRCUITS LAB MANUAL





Department of Electronics & Communication Engineering

VEMU INSTITUTE OF TECHNOLOGY::P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

(Approved by AICTE, New Delhi & Affiliated to JNTUA, Anantapuramu)

ELECTRONIC DEVICES & CIRCUITS LAB MANUAL

Name:_____

H.T.No:_____

Year/Semester:_____

Department of Electronics & Communication Engineering

VEMU INSTITUTE OF TECHNOLOGY::P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

(Approved by AICTE, New Delhi & Affiliated to JNTUA, Anantapuramu)

VEMU Institute of Technology
Dept. of Electronics and Communication Engineering

Vision of the institute

To be one of the premier institutes for professional education producing dynamic and vibrant force of technocrats with competent skills, innovative ideas and leadership qualities to serve the society with ethical and benevolent approach.

Mission of the institute

Mission_1: To create a learning environment with state-of-the art infrastructure, well equipped laboratories, research facilities and qualified senior faculty to impart high quality technical education.

Mission_2: To facilitate the learners to inculcate competent research skills and innovative ideas by Industry-Institute Interaction.

Mission_3: To develop hard work, honesty, leadership qualities and sense of direction in learners by providing value based education.

Vision of the department

To develop as a center of excellence in the Electronics and Communication Engineering field and produce graduates with Technical Skills, Competency, Quality, and Professional Ethics to meet the challenges of the Industry and evolving Society.

Mission of the department

Mission_1: To enrich Technical Skills of students through Effective Teaching and Learning practices to exchange ideas and dissemination of knowledge.

Mission_2: To enable students to develop skill sets through adequate facilities, training on core and multidisciplinary technologies and Competency Enhancement Programs.

Mission_3: To provide training, instill creative thinking and research attitude to the students through Industry-Institute Interaction along with Professional Ethics and values.

Programme Educational Objectives (PEOs)

PEO 1: To prepare the graduates to be able to plan, analyze and provide innovative ideas to investigate complex engineering problems of industry in the field of Electronics and Communication Engineering using contemporary design and simulation tools.

PEO-2: To provide students with solid fundamentals in core and multidisciplinary domain for successful implementation of engineering products and also to pursue higher studies.

PEO-3: To inculcate learners with professional and ethical attitude, effective communication skills, teamwork skills, and an ability to relate engineering issues to broader social context at work place

Programme Outcomes(Pos)

PO_1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO_2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO_3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO_4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO_5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO_6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO_7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO_8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO_9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO_10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO_11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO_12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Programme Specific Outcome(PSOs)

PSO_1	**Higher Education :** Qualify in competitive examination for pursuing higher education by applying the fundamental concepts of Electronics and Communication Engineering domains such as Analog & Digital Electronics, Signal Processing, Communication & Networking, Embeded Systems, VLSI Design and Control systems etc.,
PSO_2	**Employment**: Get employed in allied industries through their proficiency in program specific domain knowledge, Specalized software packages and Computer programming or became an entrepreneur.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

I B.Tech.II-Sem (ECE)

(20A04101P) ELECTRONIC DEVICES AND CIRCUITS LAB

COURSE OUTCOMES(CO_{S})

CO1	Understand the basic characteristics by plotting graphs and applications of basic electronic devices
CO2	Analyze the Characteristics of UJT, BJT, FET, and SCR
CO3	Design FET based amplifier circuits/BJT based amplifiers for the given specifications
CO4	Analyze all Electronic Circuits by Simulating in Multisim/Pspice.

LIST OF EXPERIMENTS:

1. Verification of Volt- Ampere characteristics of a PN junction diode and find static, dynamic and reverse resistances of the diode from the graphs obtained.
2. Design a full wave rectifier for the given specifications with and without filters, and verify the given specifications experimentally. Vary the load and find ripple factor. Draw suitable graphs.
3. Verify various clipping and clamper circuits using PN junction diode and draw the suitable graphs.
4. Design a Zener diode based voltage regulator against variations of supply and load. Verify the same from the experiment.
5. Study and draw the output and transfer characteristics of MOSFET (Enhance mode) in Common Source Configuration experimentally. Find Threshold voltage (VT), gm, & K from the graphs.
6. Study and draw the output and transfer characteristics of MOSFET (Depletion mode) or JFET in Common Source Configuration experimentally. Find IDSS, gm, & VP from the graphs.
7. Verification of the input and output characteristics of BJT in Common Emitter configuration experimentally and find required h – parameters from the graphs.
8. Study and draw the input and output characteristics of BJT in Common Base configuration experimentally, and determine required h – parameters from the graphs.
9. Study and draw the Volt Ampere characteristics of UJT and determine η, IP, Iv,V_P, &Vv from the experiment
10. Design and analysis of voltage- divider bias/self bias circuit using BJT.
11. Design and analysis of voltage- divider bias/self bias circuit using JFET.

12. Design and analysis of self bias circuit using MOSFET.
13. Design a suitable circuit for switch using CMOSFET/JFET/BJT.
14. Design a small signal amplifier using MOSFET (common source)for the given specifications. Draw the frequency response and find the bandwidth.
15. Design a small signal amplifier using BJT (common emitter)for the given specifications. Draw the frequency response and find the bandwidth.

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(20A04101P) ELECTRONIC DEVICES AND CIRCUITS LAB I B.Tech– II SEM

LIST OF EXPERIMENTS TO BE CONDUCTED

SOFTWARE EXPERIMENTS

PART-A:

1. V-I Characteristics of PN Junction Diode.
2. Full wave Rectifier with and without Filter.
3. Wave shaping Circuits (Clippers & Clampers)
4. Zener Diode as Voltage Regulator.
5. Common Source Configuration Using MOSFET
6. Common Source Configuration Using JFET
7. Input and output characteristics of Transistor in CE configuration.
8. Input and output characteristics of Transistor in CB configuration.
9. Volt Ampere Characteristics of UJT.
10. Transistor as a switch Using BJT.
11. Common Source Amplifier Using MOSFET.
12. Common Emitter Amplifier Using BJT.

PART-B:

HARDWARE EXPERIMENTS

1. V-I Characteristics of PN Junction Diode.
2. Full wave Rectifier with and without Filter.
3. Wave shaping Circuits (Clippers & Clampers)
4. Zener Diode as Voltage Regulator.
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ADVANCED EXPERIMENTS (BEYOND CURRICULUM)

1. UJT Relaxation Oscillator.
2. Implementation of Logic Gates Using Diode and Transistor.

CONTENTS

ADVANCED EXPERIMENTS (BEYOND CURRICULUM)			
1	UJT RELAXIATION OSCILLATOR		
2	IMPLEMENTATION OF LOGIC GATES USING DIODE AND TRANSISTOR		

DOs & DON'Ts IN LABORATORY

DO's

1. Students should be punctual and regular to the laboratory.
2. Students should come to the lab in-time with proper dress code.
3. Students should maintain discipline all the time and obey the instructions.
4. Students should carry observation and record completed in all aspects.
5. Students should be at their concerned experiment table, unnecessary moment is restricted.
6. Student should follow the indent procedure to receive and deposit the components from the Lab technician.
7. While doing the experiments any failure / malfunction must be reported to the faculty.
8. Students should check the connections of circuit properly before Switch ON the power supply.
9. Students should verify the reading with the help of the lab instructor after completion of experiment.
10. Students must endure that all switches are in the Lab OFF position, all the connections are removed.
11. At the end of practical class the apparatus should be returned to the lab technician and take back the indent slip.
12. After completing your lab session SHUTDOWN the Systems, TURNOFF the power switches and arrange the chairs properly.
13. Each experiment should be written in the record note book only after getting signature from the lab in charge in the observation note book.

DON'Ts

1. Don't eat and drink in the laboratory.
2. Don't touch electric wires.
3. Don't turn ON the circuit unless it is completed.
4. Avoid making loose connections.
5. Don't leave the lab without permission.
6. Don't bring mobiles into laboratory.
7. Do not open any irrelevant sites on computer.

8. Do not use a flash drive on computers.

SCHEME OF EVALUATION

HARDWARE AND SOFTWARE EXPERIMENT

S.No	Program	Date	Marks Awarded				Total 30(M)
			Record (10M)	Obs. (10M)	Viva (5M)	Attd. (5M)	
1	V-I CHARACTERISTICS OF PN JUNCTION DIODE.						
2	FULL WAVE RECTIFIER.						
3	CLIPPING AND CLAMPER.						
4	ZENER DIODE AS VOLTAGE REGULATOR.						
5	COMMON SOURCE CONFIGURATION USING MOSFET.						
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12	COMMON EMITTER AMPLIFIER USING BJT						
ADVANCED EXPERIMENTS (BEYOND CURRICULUM)							
1	UJT RELAXIATION OSCILLATOR						

2	IMPLEMENTATION OF LOGIC GATES USING DIODE AND TRANSISTOR						

1. Verification of Volt- Ampere characteristics of a PN junction diode and find static, dynamic and reverse resistances of the diode from the graphs obtained.

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PART -A

SIMULATION LAB EXPERIMENTS

Circuit Diagram:

Forward Bias:

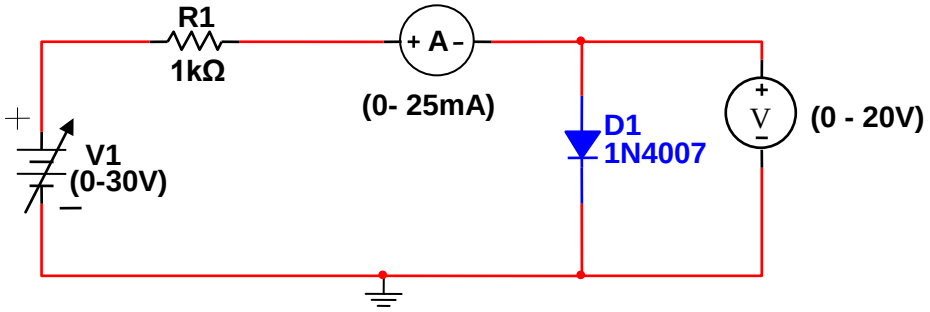


Fig. (1) Forward biased PN Junction Diode

Reverse bias:

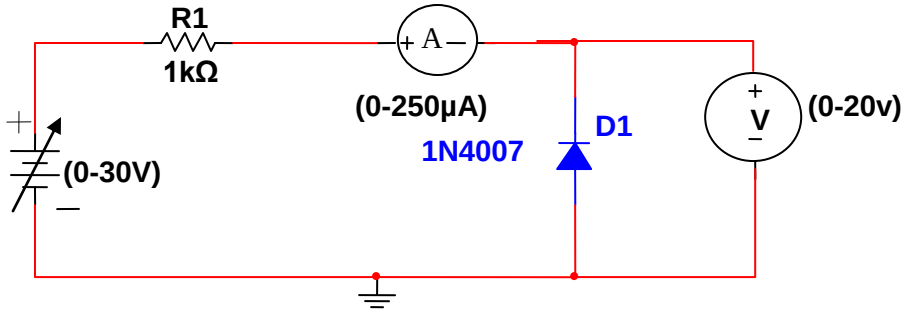
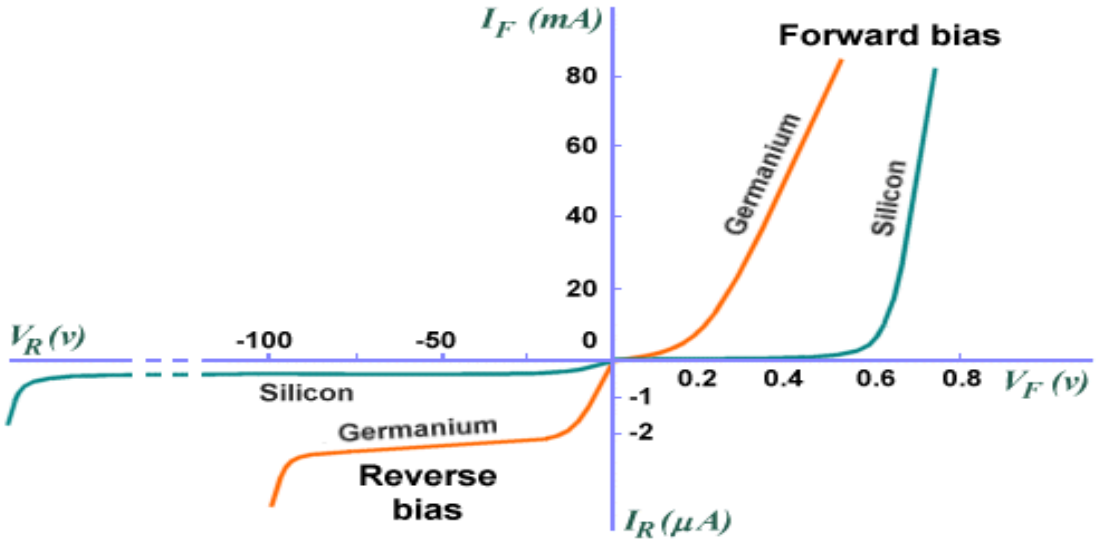


Fig. (2) Reverse biased PN Junction Diode

Model Graph:



Volt Ampere Characteristics of PN Junction Diode

Exp: 1 **Date:**

PN JUNCTION DIODE CHARACTERISTICS

Aim: To simulate the circuit of forward and reverse biased PN Junction diode using Multisim software and to determine diode static, dynamic, reverse resistance values from its Volt-Ampere characteristics.

Software Required: Multisim software 14.1 version.

Hardware Required: Personal Computer

Theory:

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode is the plot between voltage drop across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. In forward bias the potential barrier is reduced and at cut in voltage, the potential barrier altogether eliminated and current starts to flow through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage.

In Reverse bias the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current is due to the minority charge carriers. The application of diodes includes – Rectifiers, Switch, Clippers, Clampers, Demodulator, etc.

Tabular column

Forward bias:

S. No.	Silicon Diode	
	V_F(V)	I_F (mA)

Reverse bias:

S. No.	Silicon Diode	
	V_r(V)	I_r(µA)

Procedure:

Forward bias:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar.
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications.
4. Simulate the circuit.
5. Observe the voltage drop across diode and circuit current values.
6. Plot the graph between Forward voltage and current (V_f and I_f).
7. Find the Static Forward Resistance $R_f = V/I$ Ω.
8. Find the Dynamic Forward Resistance.

Reverse bias:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar.
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications
4. Simulate the circuit.
5. Observe the voltage drop across diode and circuit current values.
6. Plot the graph between V_r and I_r.
7. Find the Static Reverse Resistance.
8. Find the Dynamic Reverse Resistance.

Result:

Determine the static and dynamic diode resistances.

1. Static Forward Resistance R_F =
2. Static Reverse Resistance R_r =
3. Dynamic Forward Resistance =
4. Dynamic Reverse Resistance =

Conclusion:

1.

2

.

Viva questions:

1. Write the Diode current equation?

2. What is Reverse Saturation Current?

3. What is relation between Temperature and reverse saturation current?

4. What is transition and diffusion capacitance?

5. What is Cut-in Voltage for P-N Junction Diode?

CIRCUIT DIAGRAM:-

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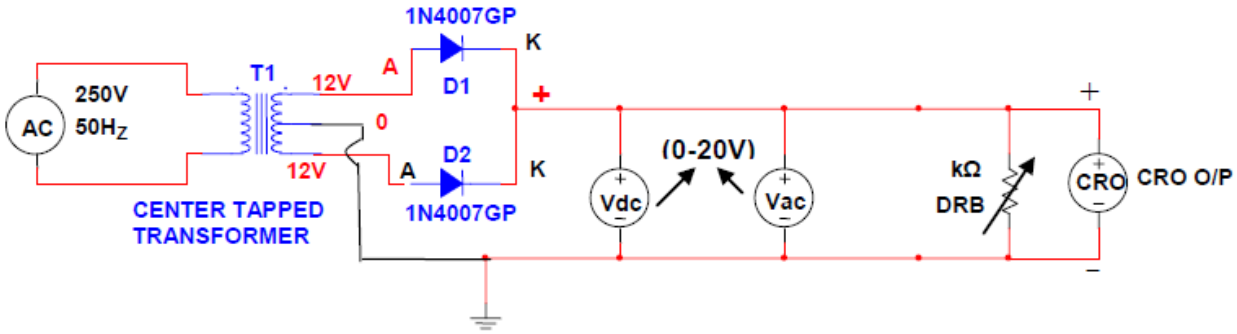

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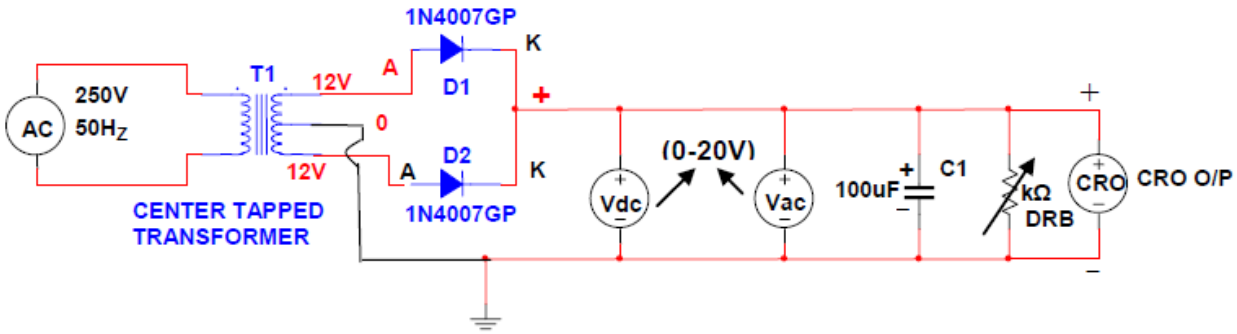
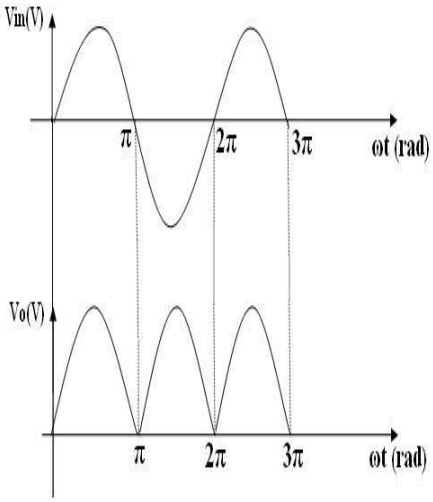


Model Waveforms:

WITHOUT FILTER:

input

Output



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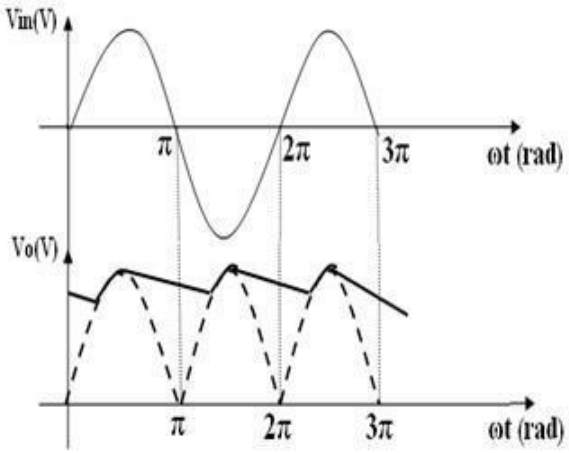

Model Graphs:

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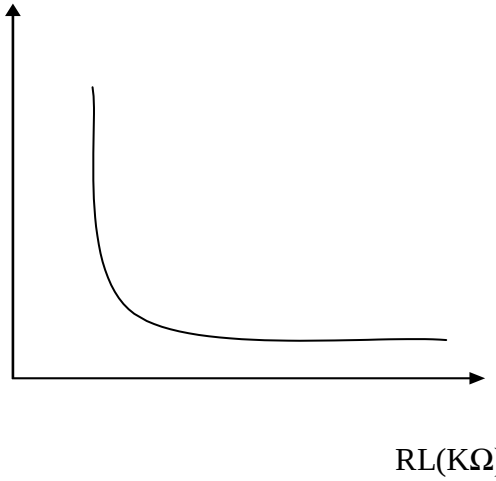

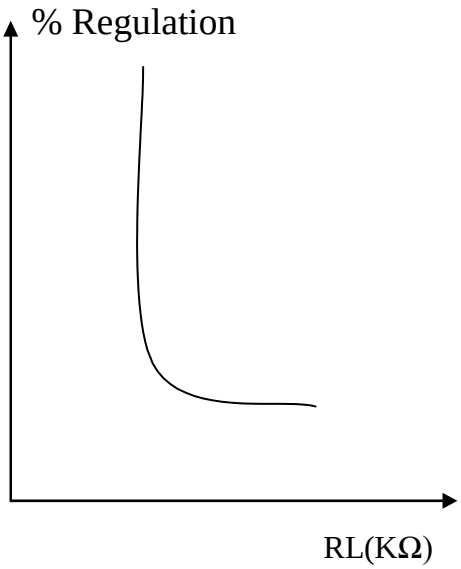

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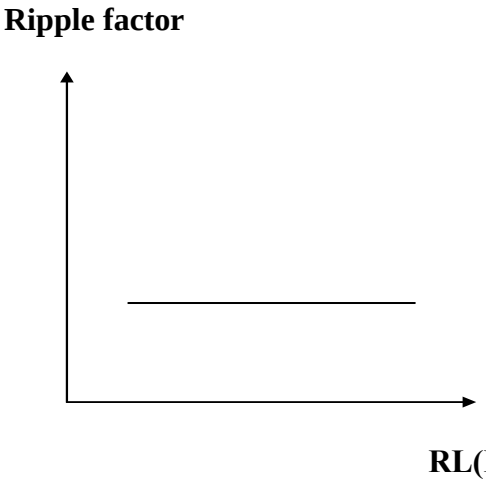
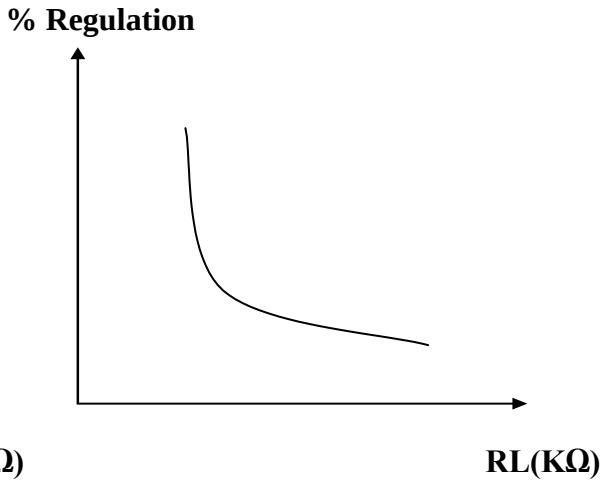




Calculations :

Calculate the ripple factor (r) $= \frac{R.M.S\ VALUES\ OF\ A.C\ COMPONENT}{AVERAGE\ VALUE} = \frac{Vac}{Vdc}$

Calculate the Percentage of Regulation = $[(V_{dc0} - V_{dc})/V_{dc}]$ x 100
(or) $(V_{NL} - V_{FL})/V_{FL}$ X100

Exp: 02 **Date:**

FULL WAVE RECTIFIER

Aim: To simulate the Full Wave Rectifier circuit using Multisim software and to determine its ripple factor and Percentage of Regulation.

Software Required: Multisim software 14.1 version.

Hardware Required: Personal Computer

Theory:

The FWR converts an AC voltage into a pulsating DC voltage using both half cycles of the applied ac voltage. It uses two diodes of which one conducts during one half cycle while the other diode conducts during the other half cycle of the applied ac voltage. There are two types of full wave rectifiers.

(i). Center taped transformer FWR
(ii). Bridge rectifier

Procedure:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar
2. Using component tool bar place all the components on the circuit window and wire the Circuit.
3. Connect the circuit diagram as per the given Specifications.
4. Simulate the circuit.
5. Note down the No Load DC Voltage V_{dc0} when $I_{dc} = 0$
6. Observe the values I_{dc} and V_{dc}, V_{ac} by varying the load resistance $R_{L.}$
7. Calculate the ripple factor (r) $= \frac{R.M.S\ VALUES\ OF\ A.C\ COMPONENT}{AVERAGE\ VALUE} = \frac{Vac}{Vdc}$
8. Calculate the Percentage of Regulation = $[(V_{dc0} - V_{dc})/V_{dc}]$ x 100

   (or) $(V_{NL} - V_{FL})/V_{FL}$ X100
9. lot the following graphs: Percentage of Regulation versus I_{dc} taking I_{dc} on x – axis.

   I_{dc} versus Ripple factor

Tabular column: (Without Filter) **No Load D.C Voltage (V_{NL}) =**

S. No.	R_L (Ω)	V_{dc} (V)	V_{ac} (V)	r = V_{ac}/V_{dc}	% Regulation $[(V_{NL}- V_{FL})/V_{FL}]$ X100
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					

With filter: **No Load D.C Voltage (V_{dc0}) =**

S. No.	R_L (Ω)	V_{dc} (V)	V_{ac} (V)	r = V_{ac}/V_{dc}	% Regulation $[(V_{NL}- V_{FL})/V_{FL}]$ X100
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					

Result:

Ripple Factor =

Percentage of Regulation =

Conclusions:

1.

2.

Viva Questions:

1. Define ripple factor.

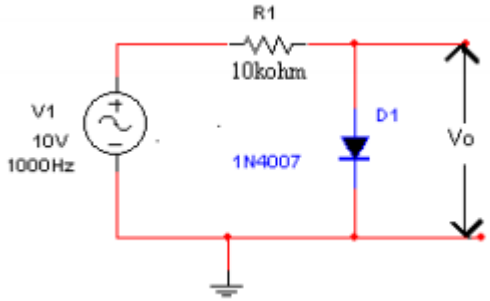
2. Define efficiency.

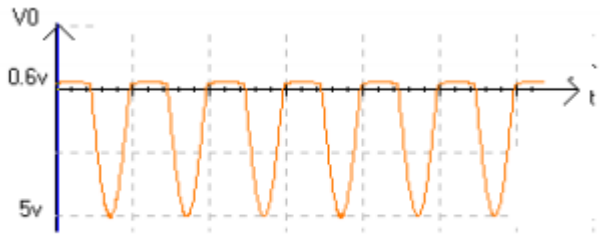
3. Define %Regulation.

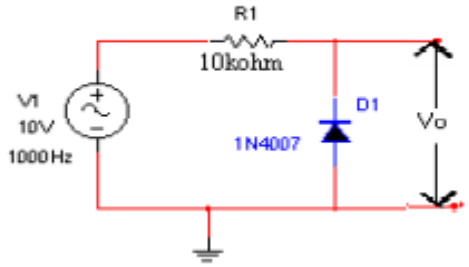
4. Define TUF.

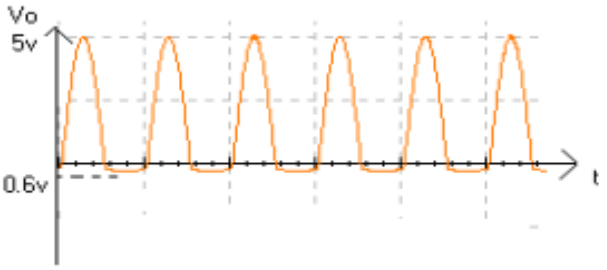
5. Define Peak Inverse Voltage (PIV).

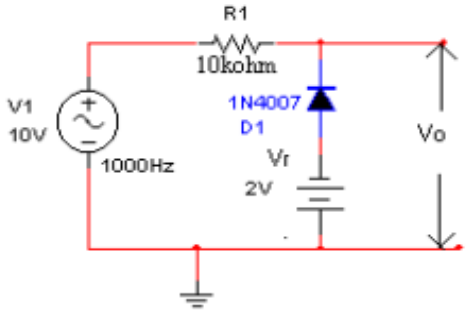
Clipper Circuits with their corresponding output waveforms:

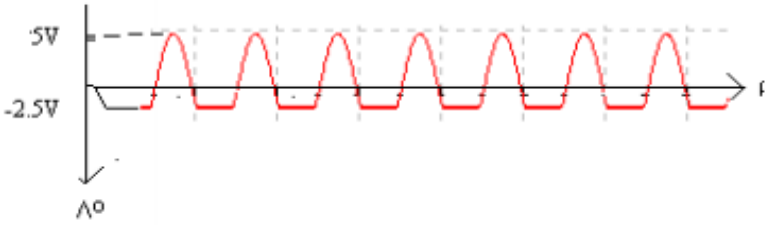


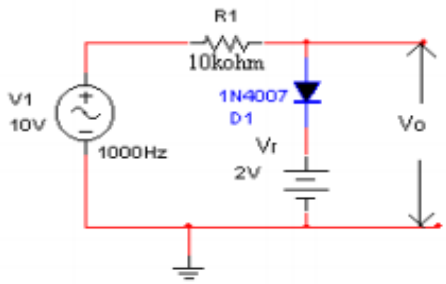


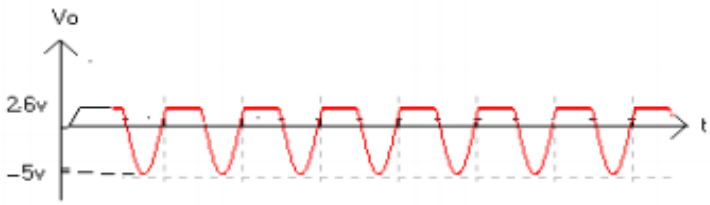












Exp:03 **Date:**

DIODE APPLICATIONS-CLIPPERS & CLAMPERS

CLIPPERS

Aim: To simulate the positive, negative and two level clipping circuits using Multisim Software.

Software Required: Multisim software 14.1 version.

Hardware Required: Personal Computer

Theory:

A clipper is a device designed to prevent the output of a circuit from exceeding a predetermined voltage level without distorting the remaining part of the applied waveform. A clipping circuit consists of linear elements like resistors and non-linear elements like junction diodes or transistors, but it does not contain energy-storage elements like capacitors. Clipping circuits are used to select for purposes of transmission, that part of a signal wave form which lies above or below a certain reference voltage level. Thus a clipper circuit can remove certain portions of an arbitrary waveform near the positive or negative peaks. Clipping may be achieved either at one level or two levels.

Procedure:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications
4. Simulate the circuit.
5. In each case apply 10 VP-P, 1 KHz Sine wave I/P using a signal generator.
6. Observe the O/P waveform across the load R_L using the CRO and compare with I/P waveform.
7. Repeat the above steps for all the clipping circuits.

Result:

The practical values

V= $\gamma + V_R$

V= $\gamma - V_R$

Conclusion:

1.

2.

Viva questions:

1. Define clipping? Describe (i) Positive clipper (ii) Biased Clipper (iii) Combination clipper.

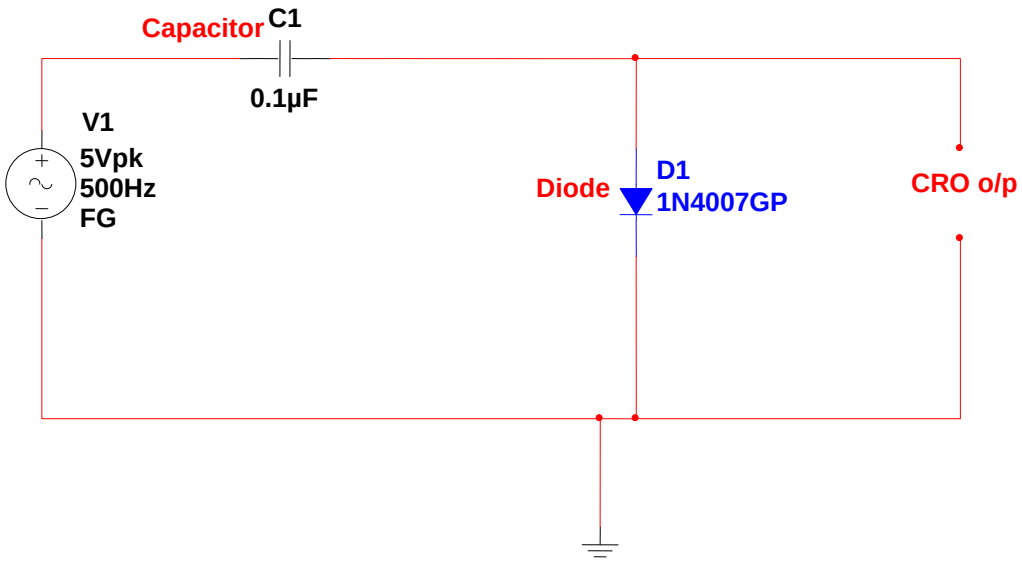
2. Define clamping?

3. Define peak inverse voltage of diode?

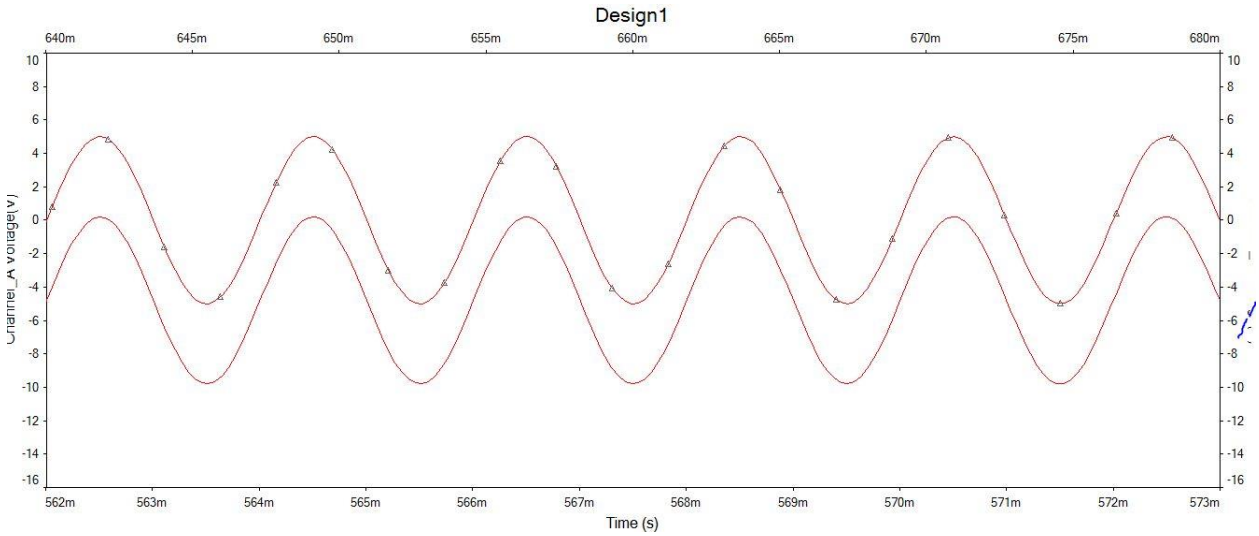
4. What are the other names for the clamper?

5. What are the applications of clampers?

Circuit Diagram: Clamper Circuit :



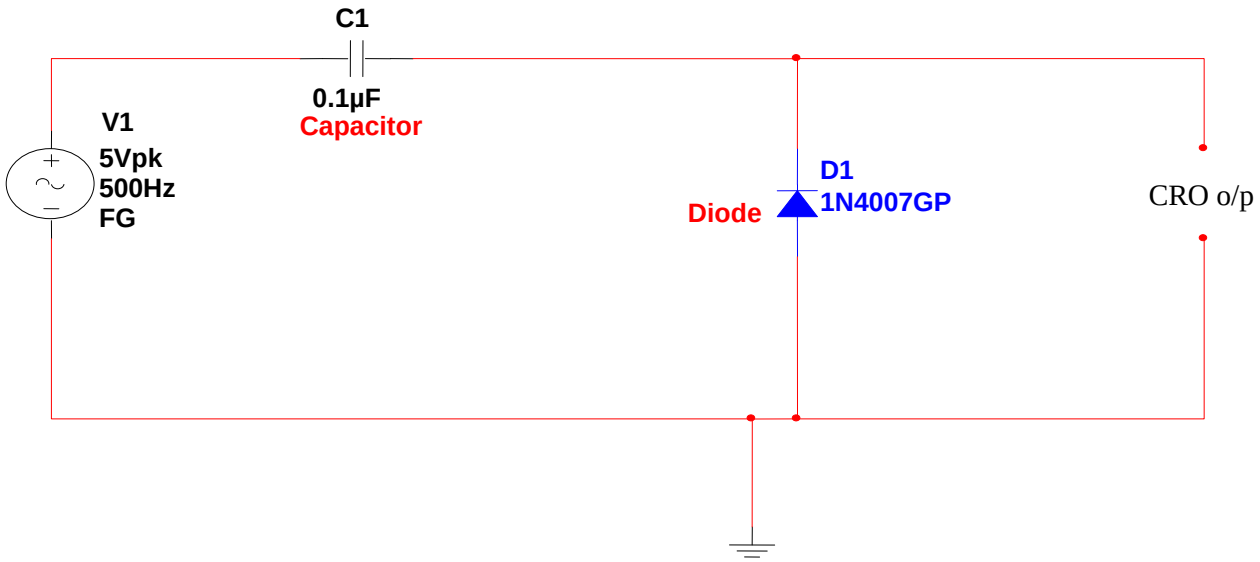
Input and Output waveform:



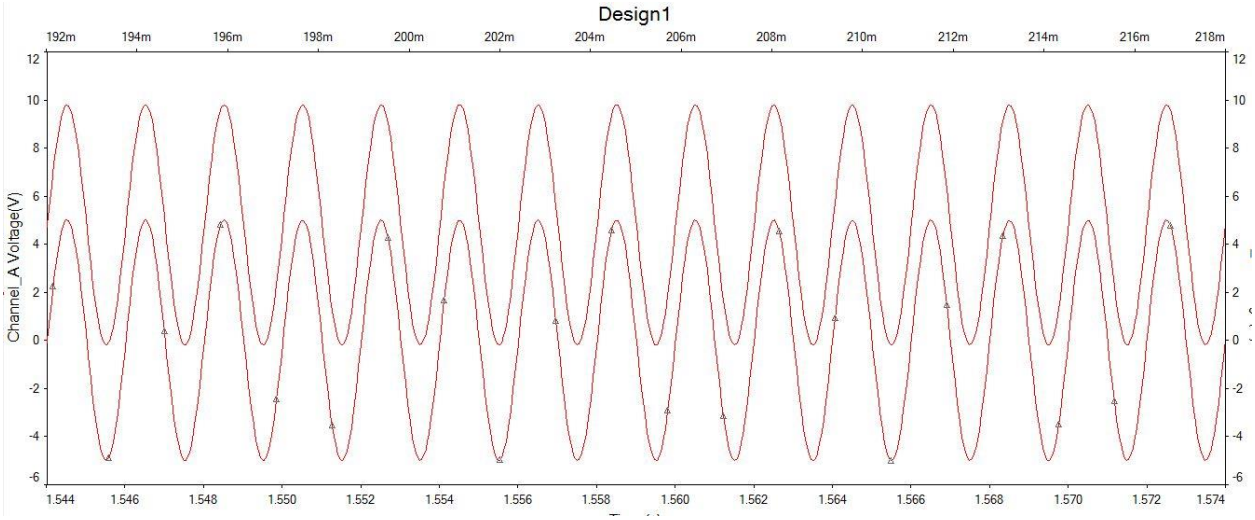
Tabular column:

S. No	Waveform	Amplitude	Frequency (time period)
1.			

Circuit Diagram: Clamper Circuit:



Input and Output waveform:



Tabular column:

S. No	Waveform	Amplitude	Frequency (time period)
1.			

Exp: 3(b) **Date:**

CLAMPERS

Aim: To Simulate Clamping circuits using Multisim Software.

Software Required: Multisim software 14.1 version.

Hardware Required: Personal Computer

Theory:

A clamper is an electronic circuit that prevents a signal from exceeding a certain defined magnitude by shifting its DC value. The clamper does not restrict the peak-to-peak excursion of the signal, but moves it up or down by a fixed value. A diode clamp (a simple, common type) relies on a diode, which conducts electric current in only one direction; resistors and capacitors in the circuit are used to maintain an altered dc level at the clamper output. The different types of clampers are positive negative and biased clampers. A positive clamp circuit outputs a purely positive waveform from an input signal; it offsets the input signal so that all of the waveform is greater than 0 V. A negative clamp is the opposite of this - this clamp outputs a purely negative waveform from an input signal. A clamping network must have a capacitor, a diode and a resistive element. The magnitude R and C must be chosen such that the time constant RC is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non- conducting.

Procedure:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications.
4. Simulate the circuit.
5. In each case apply 10 V_{P-P}, 1 KHz Sine wave I/P using a signal generator.
6. Observe the O/P waveform across the load R_L using the CRO and compare with I/P waveform.
7. Repeat the above steps for all the clamping circuits.

Result:

Conclusion:

1.

2.

Viva questions:

1. Differentiate the clippers and clampers.

2. Give the applications of clampers.

3. List the different types of clampers.

4. State clamping circuit theorem.

5. What is meant by non-linear wave shaping?

Circuit Diagram:

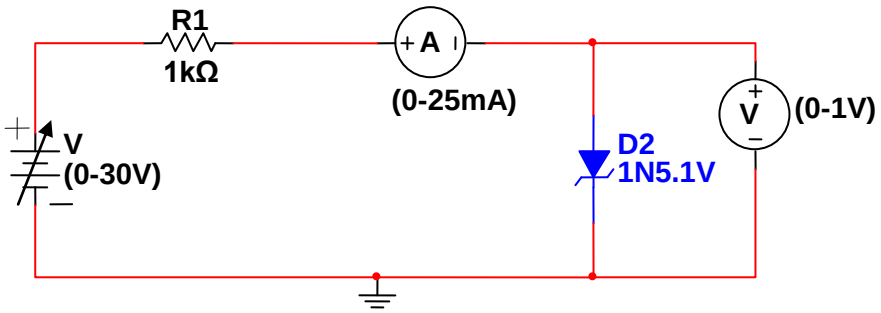


Fig. 1: V-I CHARACTERISTICS:

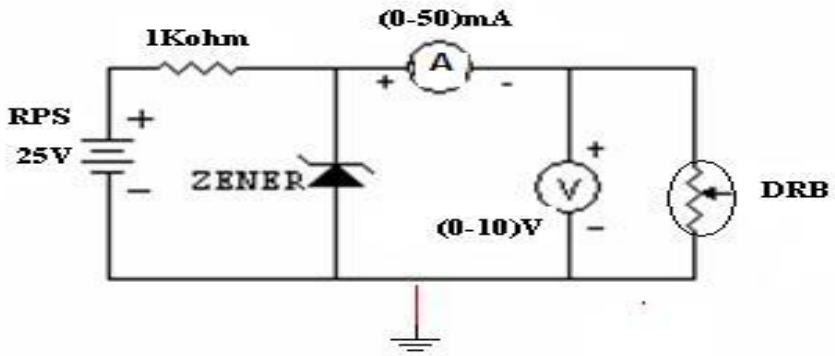
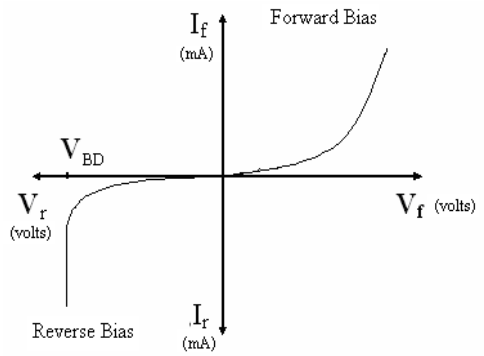


Fig. 2 Zener Diode based Voltage Regulator

Model Graph:



V-I Characteristics

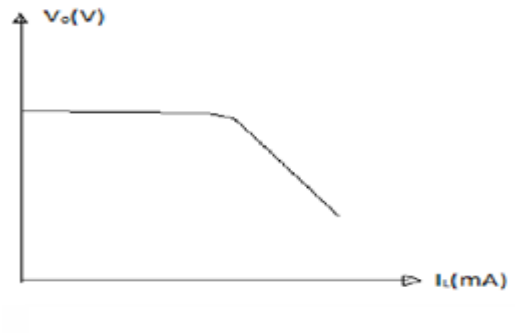


Fig. Regulation Characteristics

Exp: 4 **Date:**

ZENER DIODE BASED VOLTAGE REGULATOR

Aim: To simulate Zener diode based voltage regulator using Multisim Software.

Software Required: Multisim software 14.1 version.

Hardware Required: Personal Computer

Theory:

A Zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device. To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals whatever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

Procedure:

Load Regulation Characteristics:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications.
4. Simulate the circuit.
5. Fix the DC supply at 20V.
6. By varying the load resistances observe the load voltage V_L and load current I_L.
7. Plot the graph between load voltages V_L and load current I_L.

Result:

1. Volt – Ampere Characteristics of Zener Diode are plotted.
2. Zener Break Down Voltage =
3. Dynamic Forward Resistance =
4. Dynamic Reverse Resistance =

Tabular column:

(i). V-I CHARACTERISTICS:

S.No	Zener Voltage (V_Z) (volts)	Zener Current (I_Z) (mA)

(ii). Zener Diode based Voltage Regulator

S. No.	R_L	Voltage across Load, V_L(V)	Current through the load resistance, I_L(mA)

Conclusions:

1.

2.

Viva Questions:

1. Differentiate PN Junction diode and zener diode.

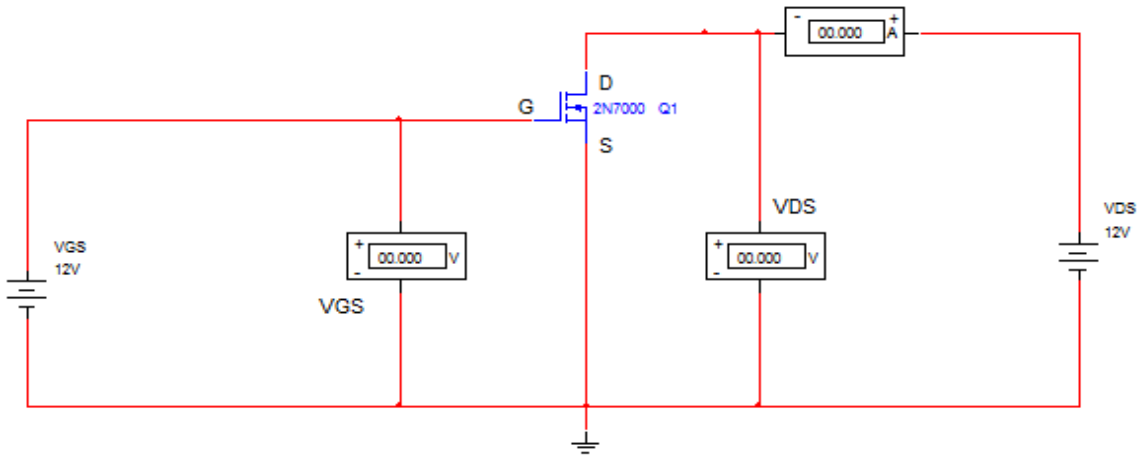
5. List the applications of zener diode.

6. Explain how zener diode acts as voltage regulator.

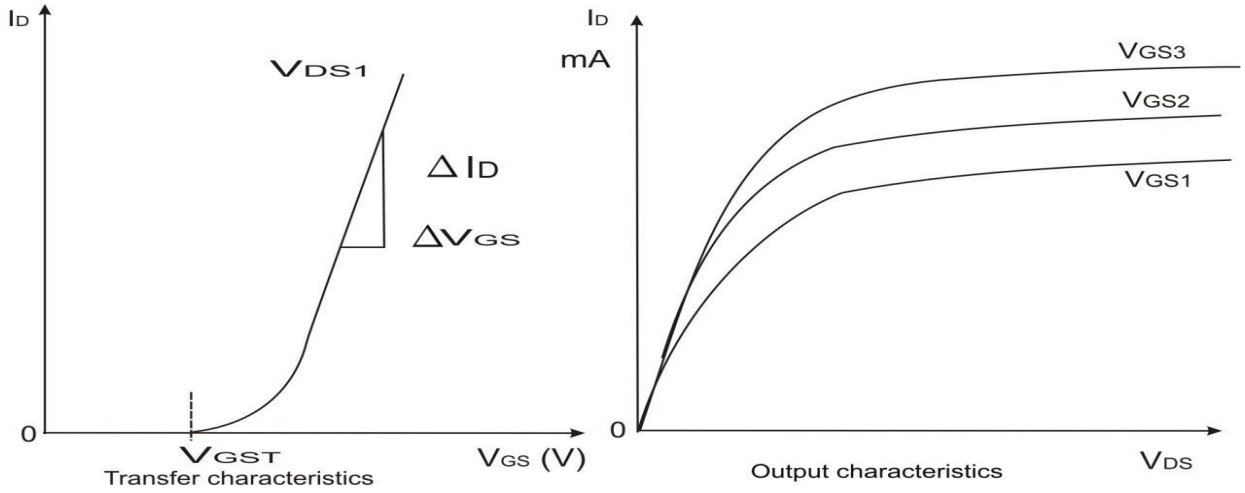
7. Define zener Breakdown.

8. Define thermal Breakdown

CIRCUIT DIAGRAM OF MOSFET CHARACTERISTICS:



Model Graph:



Exp: 5 **C**HARACTERISTICS OF MOSFET **Date:**

Aim: To plot the Transfer and Drain characteristics of MOSFET and determine Trans conductance and output Resistance in Enhancement mode using Multisim software

Software Required: Multisim software 14.1 version.

Hardware Required: Personal Computer

Theory:

A MOSFET (Metal oxide semiconductor field effect transistor) has three terminals called Drain, Source and Gate. MOSFET is a voltage controlled device. It has very high input impedance and works at high switching frequency.

MOSFET's are of two types 1) Enhancement type 2) Depletion type.

Procedure:

A).Transfer characteristics

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar.Make the connections as per the circuit diagram. .
2. Initially keep V1 and V2 at 0 V.
3. Switch ON the regulated power supplies. By varying V1,

set VDS to some constant voltage say 5V.

4. Vary V2 in steps of 0.5V, and at each step note down the corresponding values of VGS and ID.

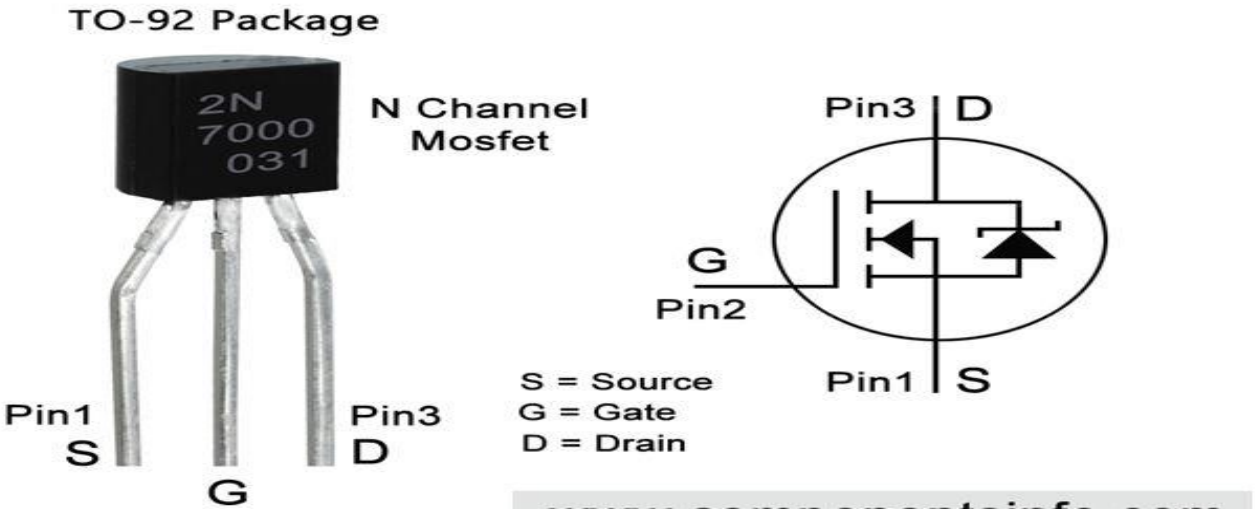
(Note: note down the value of VGS at which ID starts increasing as the threshold voltage).

5. Reduce V1 and V2 to zero.
6. By varying V1, set VDS to some other value say 10V.
7. Repeat step 4.
8. Plot a graph of VGS versus ID for different values of VDS.

B) Drain or Output Characteristics:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar.Make the connections as per the circuit diagram.
2. Initially keep V1 and V2 at zero volts.
3. By varying V2, set VGS to some constant voltage (must be more than Threshold voltage).
4. By gradually increasing V1, note down the corresponding value of VDS and ID. (Note: Till the MOSFET jumps to conducting state, the voltmeter which is connected across device as VDS reads approximately zero voltage. Further increase in voltage by V1 source cannot be read by VDS, so connect multimeter to measure the voltage and tabulate the readings in the tabular column).
5. Set VGS to some other value (more than threshold voltage) and repeat step 4.
6. Plot a graph of VDS versus ID for different values of VGS.

2N7000 MOSFET Pinout



Tabular columns:

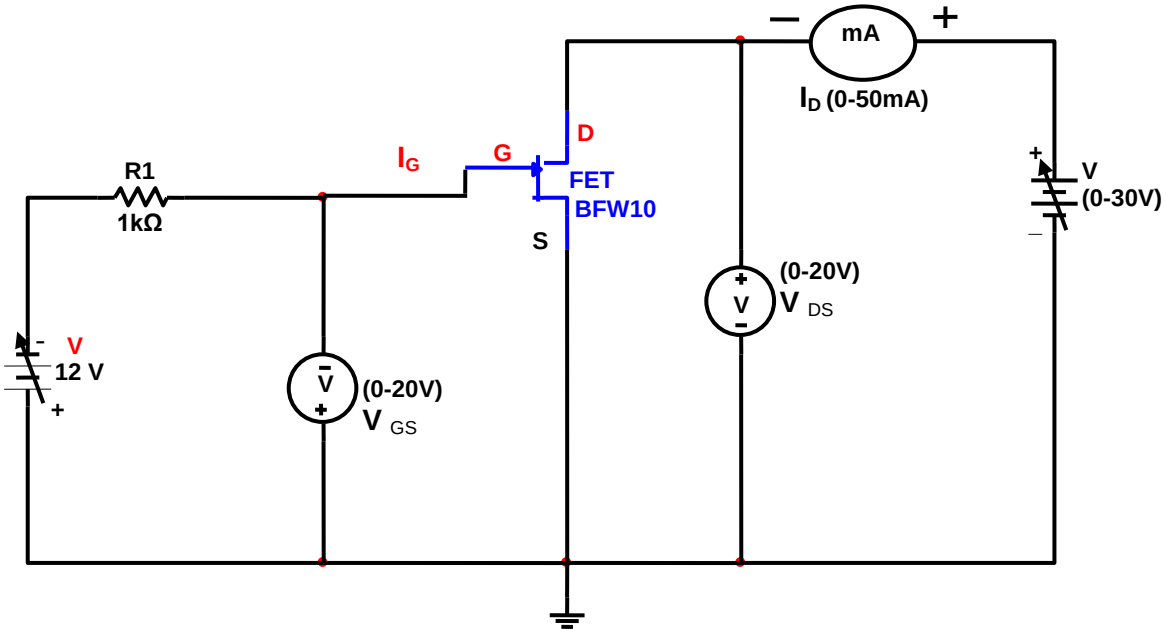
Drain characteristics:

S.No	V_{GS}= 1.1 V		V_{GS}= 1.2V	
	V_{DS}(V)	I_D (mA)	V_{DS} (V)	I_D (mA)

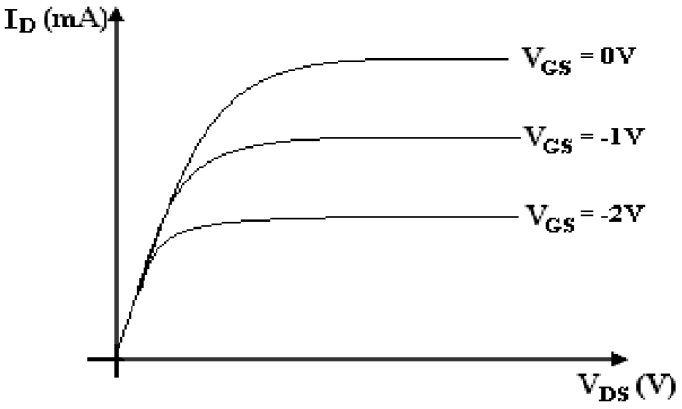
Transfer Characteristics:

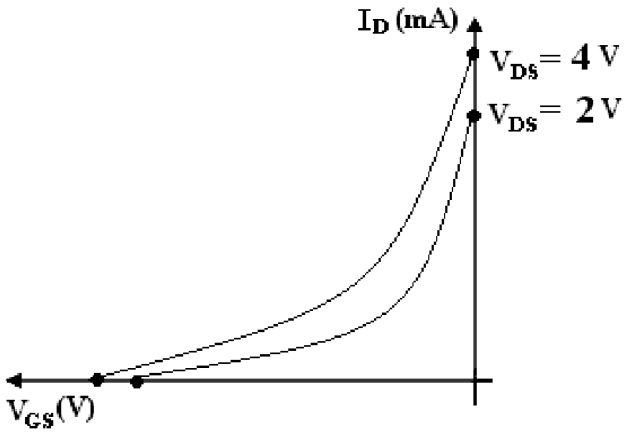
S.No	V_{DS}= 2V	
	V_{GS}(V)	I_D (mA)

Circuit diagram

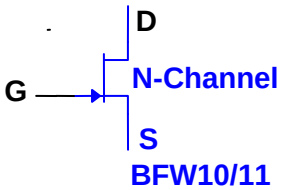


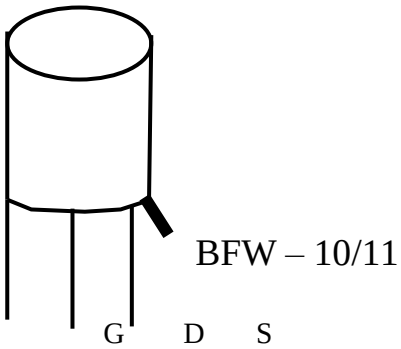
Model graphs:





PIN DETAILS OF FET :





Exp: 6 **Date:**

FET CHARACTERISTICS (IN CS CONFIGURATION)

Aim: 1. To Obtain Drain and Transfer characteristics of FET connected in Common Source configuration in Enhancement mode using Multisim software

2. To Obtain $r_{d,}$ g_m and μ of FET.

Software Required: Multisim software 14.1 version.

Hardware Required: Personal Computer

Theory:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with VDS. With increase in ID the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The VDS at this instant is called "pinch off voltage" .If the gate to source voltage (VGS) is applied in the direction to provide additional reverse bias, the pinch off voltage ill is decreased. In amplifier application, the FET is always used in the region beyond the pinch-off.

$$I_{DS} = I_{DSS} (1-V_{GS}/V_P) \text{ ^2}$$

Procedure:

Output (or) drain characteristics:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications
4. Simulate the circuit.
5. Set V_{GS} = 0V by adjusting $V_{GG.}$
6. Vary the supply voltage V_{DD} and note the readings of I_D and V_{DS}.
7. Repeat the above procedure for V_{GS} = –1V and –2V.
8. Plot the output characteristics V_{DS} Vs I_D for constant values of V_{GS} = 0 V, –1V and –2 V.
9. Find Drain Resistance $r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}}$ = Constant and Amplification Factor,

$$\mu = g_m * rd$$

Tabular columns:

Drain Characteristics:

S.No	V_{GS}= 0 V		V_{GS}= –1V	
	V_{DS}(V)	I_D (mA)	V_{DS}(V)	I_D (mA)

Transfer characteristics:

S.No	V_{DS}= 2 V		V_{DS}= 4 V	
	V_{GS}(V)	I_D (mA)	V_{GS}(V)	I_D (mA)

Procedure:

Transfer characteristics:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications
4. Simulate the circuit.
5. Set V_{DS}= 2V by adjusting $V_{DD.}$
6. Vary the input voltage V_{GG} and note the readings of I_D and V_{GS}.
7. Repeat the above procedure for V_{DS}= 4V.
8. Plot the transfer characteristics V_{GS} Vs I_D for constant values of V_{DS}= 2V and 4V.
9. Find Trans Conductance $g_{m=} \left.\frac{\Delta I_D}{\Delta V_{GS}}\right/ V_{DS}$ = Constant

Result:

1. The drain and transfer characteristics of a given FET are drawn.

2. The drain resistance (rd), amplification factor (μ) and Trans-conductance (gm) of the Given FET are calculated.

(i) The drain resistance (rd) of FET is _____

(ii) Trans-conductance (gm) of FET is_____

(iii) Amplification factor (μ) of FET is_____

Conclusion:

1.

2.

Viva Questions:

1. What is the difference between enhancement mode?

2. What is pinch off?

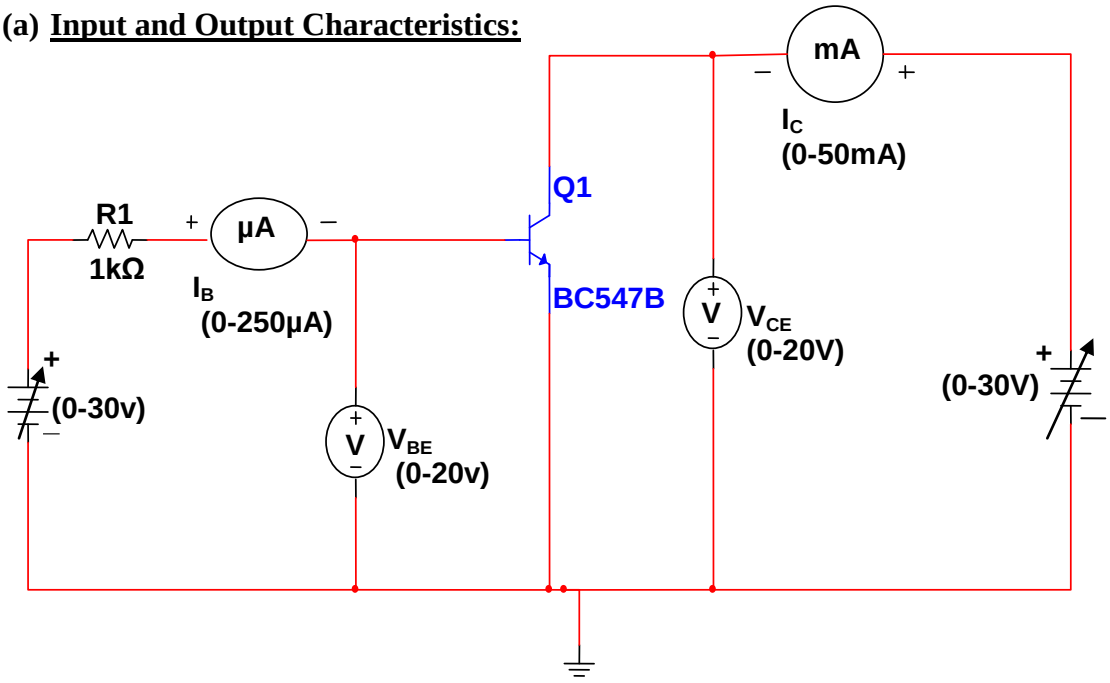
3. In which mode the continuity is exist?

4. Compare to transistor, input impedance of the FET is high(or)low?

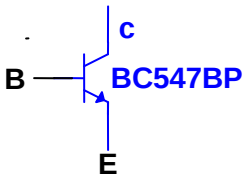
5. Differences between JFET and MOSFET?

Circuit diagram:

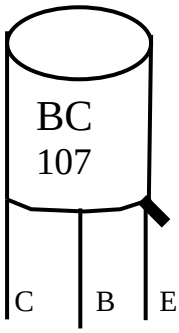
(a) Input and Output Characteristics:

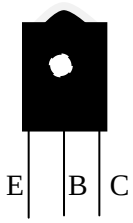


SYMBOL OF TRANSISTOR:

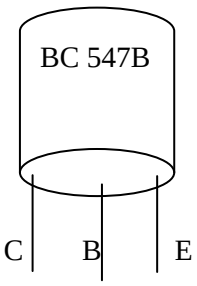


PIN DETAILS OF TRANSISTOR :



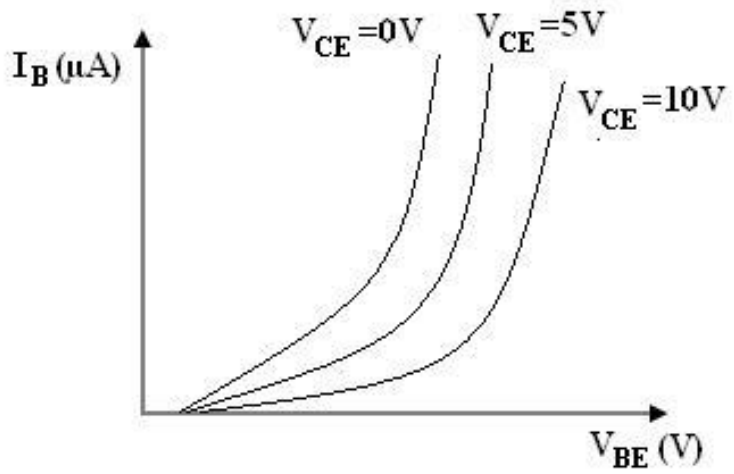


BC 547B

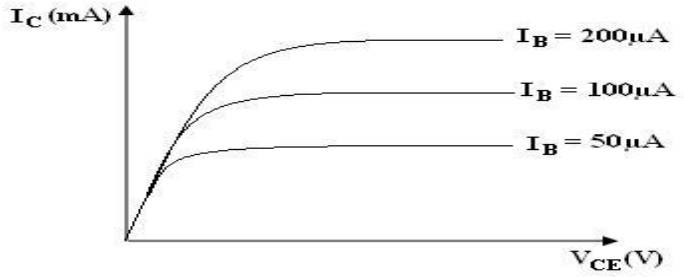


Model Graph:

Input characteristics:



Output characteristics:



Typical values:-

h_{ie}	h_{re}	h_{fe}	h_{oe}
1100Ω	2.5×10^{4}	50	25μΩ

Tabular column:
(a)Input characteristics:

S.NO	V_{CE}=		V_{CE}=	
	V_{BE}(V)	I_B (μA)	V_{BE}(V)	I_B (μA)

Tabularcolumn:

S.No	I_B=		I_B=	
	V_{CE}(V)	I_C (mA)	V_{CE}(V)	I_C (mA)

Exp: 07 **Date:**

BJT CHARACTERISTICS (CE CONFIGURATION)

Aim: 1. To Obtain Input and Output characteristics of transistor connected in Common Emitter Configuration using Multisim Software.

2. To determine the h-parameters for CE configuration.

Software Required: Multisim software 14.1 version

Hardware Required: Personal Computer

Theory:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement IB increases less rapidly with VBE. Therefore input resistance of CE circuit is higher than that of CB circuit. The output characteristics are drawn between Ic and VCE at constant IB. the collector current varies with VCE unto few volts only. After this the collector current becomes almost constant, and independent of VCE. The value of VCE up to which the collector current changes with V CE is known as Knee voltage. The transistor always operated in the region above Knee voltage, IC is always constant and is approximately equal to IB. The current amplification factor of CE configuration is given by

$$\beta = \Delta I_C / \Delta I_B$$

Procedure:

Input characteristics:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications
4. Simulate the circuit.
5. Set V_{CE} = 0 by adjusting V_{CC}.
6. Vary the input voltage V_{BB} and note the readings of I_B and V_{BE}.
7. Repeat the above procedure for V_{CE} = 2Vand 5V.
8. Plot the input characteristics V_{BE} Vs I_B for constant Values of V_{CE} = 0V, 2Vand 5V
9. Calculate h- parameters from input characteristics graph

$$\mathbf{V_{BE} = h_{ie} I_B + h_{re} V_{CE}}$$

$$\mathbf{I_C = h_{fe} I_B + h_{oe} V_{CE}}$$

a) Reverse voltage gain $h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right/ I_B$ Constant

b) Input Impedance $h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right/ \mathbf{V_{CE}}$ Constant

Output characteristics:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar. Using component tool bar place all the components on the circuit window and wire the circuit. Connect the circuit diagram as per the given specifications.
2. Simulate the circuit.
3. Set I_B = 50 μA by adjusting $V_{BB.}$
4. Vary the supply voltage V_{CC} and note the readings of I_C and V_{CE}. Take V_{CE}=V_{CC}.
5. Repeat the above procedure for I_B = 100 μA and 200 μA,
6. Plot the output characteristics V_{CE} vs I_C for constant Values of

   I_B =50 μA, 100 μA and 200 μA.
7. Calculate h- parameters from output characteristics graph

c. Output admittance $h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B}$ Constant

d. Forward current gain $h_{fe} = \left.\Delta I_C/\Delta I_B\right|_{\mathbf{V_{CE}}}$ Constant

Calculations:

1. Reverse voltage gain $h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}$ / **I**$_B$ Constant =

2. Input Impedance $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}$ / $\mathbf{V_{CE}}$ Constant =

3. Output admittance $h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}$ / **I**$_B$ Constant =

4. Forward current gain $h_{fe} = \Delta I_C / \Delta I_B$ / $\mathbf{V_{CE}}$ Constant =

Result: The input and output characteristics of a transistor in CE configuration are drawn. The Input (Ri) and Output resistances (Ro) of a given transistor are calculated.

1. The Input resistance (Ri) of a given Transistor is_____

2. The Output resistance (Ro) of a given Transistor is_____

3. The Current amplification factor is_____

Conclusion:

1.

2.

Viva questions:

1. What is meant by bipolar?

2. Define H-Parameters of a transistor.

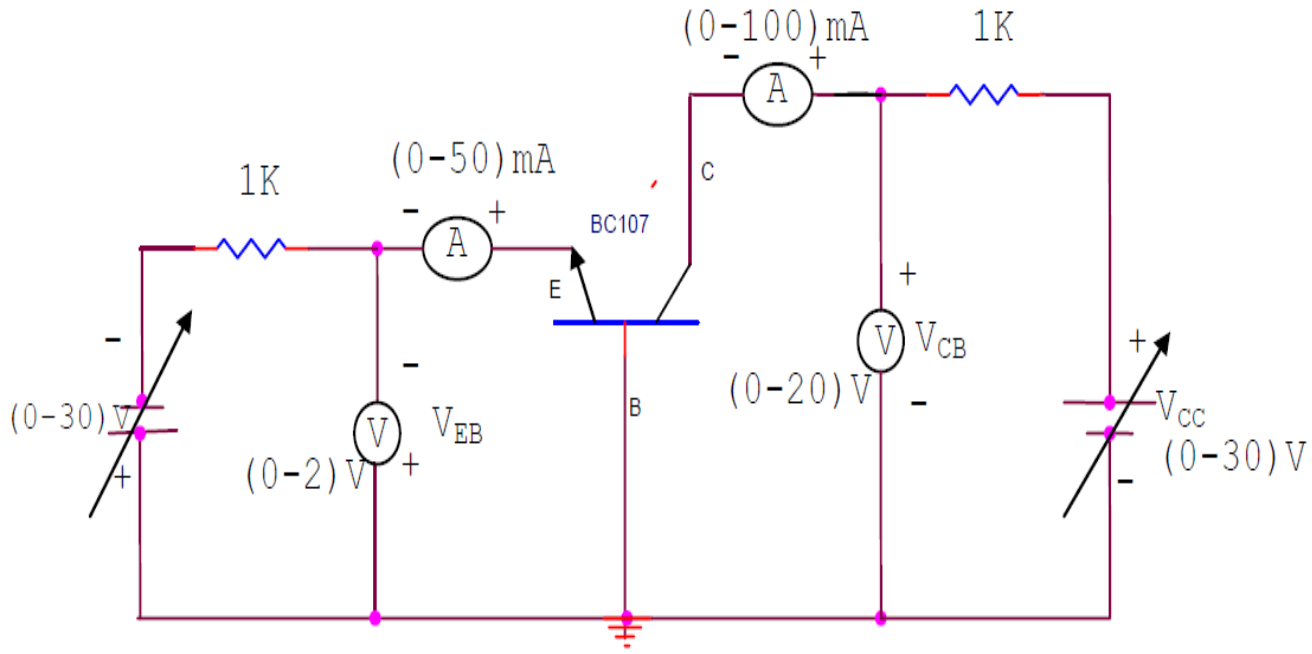
3. What is early effect?

4. Define punch through break down.

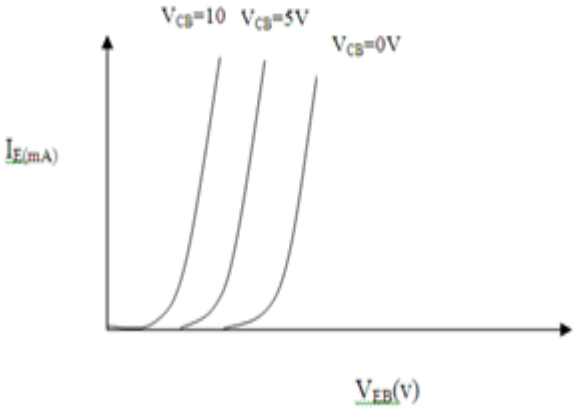
5. What are the operating modes of transistor?

Circuit diagram:

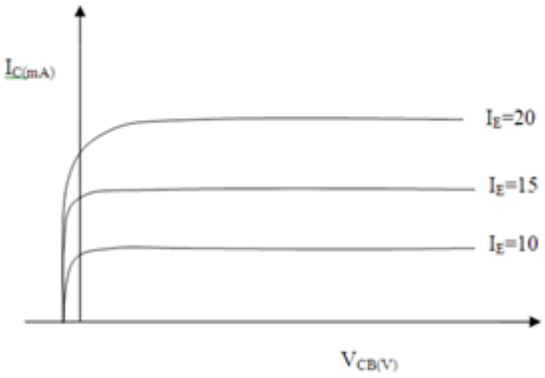
Input & Output Characteristics:



Model graph:



Input characteristics:



Output characteristics:

Exp: 08 **Date:**

BJT CHARACTERISTICS (CB CONFIGURATION)

Aim: 1. To Obtain Input and Output characteristics of transistor connected in Common Base Configuration using Multisim Software.

2. To determine the h-parameters for CB configuration.

Software Required: Multisim software 14.1 version.

Hardware Required: Personal Computer

Theory:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. In Common Base configuration the input is applied between emitter and base and the output is taken from collector and base. Here base is common to both input and output and hence the name common base configuration. Input characteristics are obtained between the input current and input voltage taking output voltage as parameter. It is plotted between VEB and IE at constant VCB in CB configuration. Output characteristics are obtained between the output voltage and output current taking input current as parameter. It is plotted between VCB and IC at constant IE in CB configuration.

The current amplification factor of CE configuration is given by

$$\alpha = \Delta I_C / \Delta I_E$$

Procedure of Input characteristics:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar. Using component tool bar place all the components on the circuit window and wire the circuit. Connect the circuit diagram as per the given specifications.
2. Simulate the circuit.
3. Set $V_{CB} = 0$ by adjusting V_{CC}.
4. Vary the input voltage V_{EE} and note the readings of I_E and V_{BE}.
5. Repeat the above procedure for V_{CB} = 2Vand 5V.
6. Plot the input characteristics V_{BE} Vs I_E for constant Values of V_{CB}= 0V, 2Vand 5V
7. Calculate h- parameters from input characteristics graph

$$\mathbf{V_{EB} = h_{ib}\, I_E + h_{rb}\, V_{CB}}$$
$$\mathbf{I_C = h_{fb}\, I_E + h_{ob}\, V_{CB}}$$

a) Reverse voltage gain $h_{rb} = \left.\frac{\Delta V_{EB}}{\Delta V_{CB}}\right/ I_E$ Constant

b) Input Impedance $h_{ib} = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right/ \mathbf{V_{CB}}$ Constant

Tabular column:
Input characteristics:

S.NO	V_{CB}=		V_{CB}=	
	V_{EB}(V)	I_E (mA)	V_{EB}(V)	I_E (mA)

Tabular column:

S.No	I_E=		I_E=	
	V_{CB}(V)	I_E (mA)	V_{CB}(V)	I_E (mA)

Output characteristics:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar. Using component tool bar place all the components on the circuit window and wire the circuit. Connect the circuit diagram as per the given specifications.
2. Simulate the circuit.
3. Set I_E = 50 mA by adjusting $V_{EE.}$
4. Vary the supply voltage V_{CC} and note the readings of I_C and V_{CB} Take V_{CB}=V_{CC}.
5. Repeat the above procedure for I_E = 100 mA and 200 mA,
6. Plot the output characteristics V_{CB} vs I_C for constant Values of I_E=50 mA, 100 mA and 200 mA.
7. Calculate h- parameters from output characteristics graph

c. Output admittance $h_{ob} = \frac{\Delta I_c}{\Delta V_{cb}} \Big/ I_E$ Constant

d. Forward current gain $h_{fb} = \frac{\Delta I_C}{\Delta I_E} \Big/ V_{CB}$ Constant

Calculations:

1. Reverse voltage gain $h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}} \Big/ I_E$ Constant =
2. Input Impedance $h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E} \Big/ V_{CB}$ Constant =
3. Output admittance $h_{ob} = \frac{\Delta I_c}{\Delta V_{cb}} \Big/ I_E$ Constant =
4. Forward current gain $h_{fb} = \frac{\Delta I_C}{\Delta I_E} \Big/ V_{CB}$ Constant =

Result:

Thus the input and output characteristics of CB configuration are plotted and h parameters are found.

a) Input impedance (hib)=
b) Forward current gain (hfb) =
c) Output admittance (hob) =
d) Reverse voltage gain(hrb)=

Conclusion;

1.

2.

Viva questions:

2. Mention about the different configurations of a transistor?

3. How a transistor performs as an electronic switch?

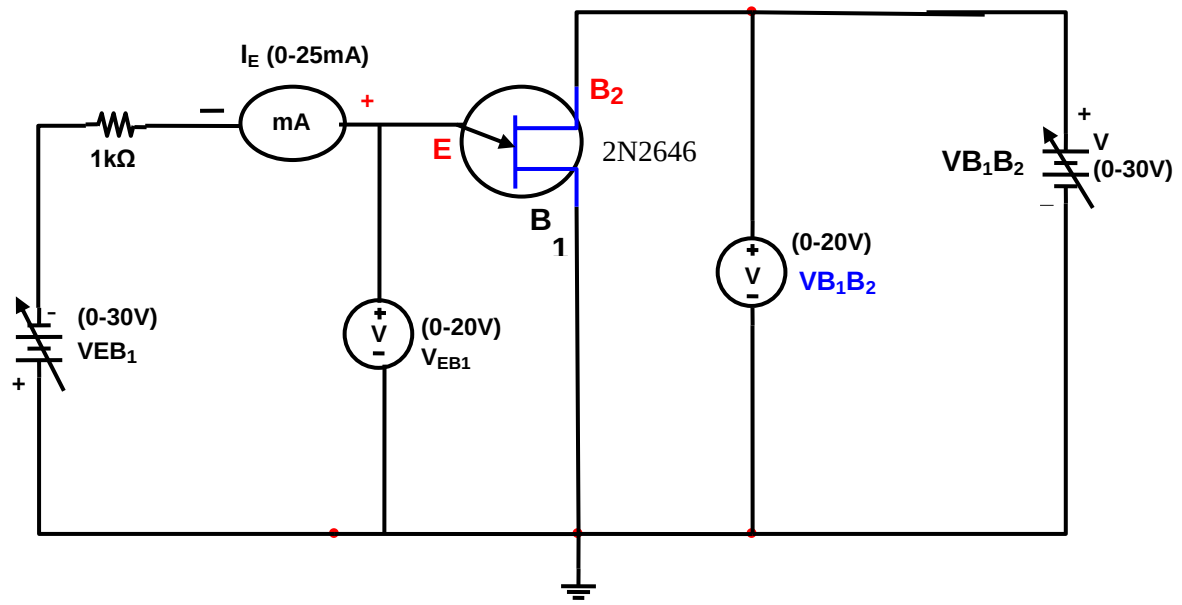
4. Explain about biasing and its need for transistors?

4 What are the applications of CB configuration?

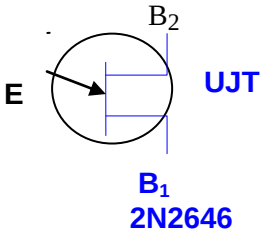
5. Why transistor is called current controlled device?

.

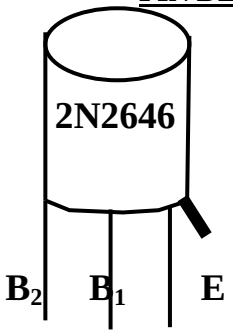
Circuit Diagram: **UJT** CHARACTERISTICS:-



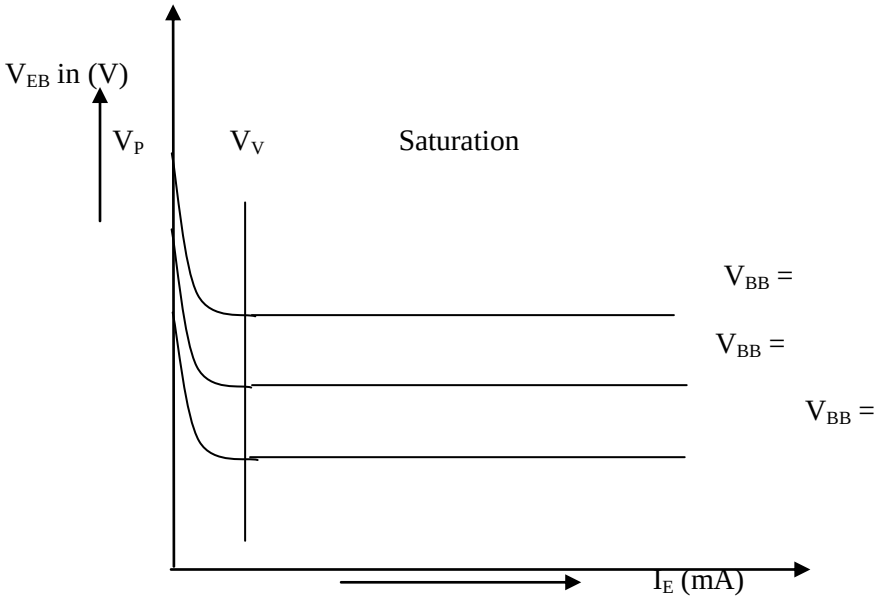
SYMBOL OF BJT:



PIN DETAILS OF UJT :



Model Graph:



Exp:09 **Date:**

V-I CHARACTERISTICS OF UJT

Aim: To obtain the characteristics of UJT and to calculate the Intrinsic Stand-Off Ratio (η) using Multisim Software

Software Required: Multisim software 14.1 version.

Hardware Required: Personal Computer

Theory: A Uni-junction Transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT Uni-junction Transistor (UJT) has three terminals, an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called inter base resistance. The original Uni-junction transistor (UJT), is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length. The 2N2646 is the most commonly used version of the UJT.

Procedure:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar. Using component tool bar place all the components on the circuit window and circuit. Connect the circuit diagram as per the given specifications.
2. Simulate the circuit.
3. Output voltage is fixed at a constant level and by varying input voltage corresponding emitter current values are noted down.
4. This procedure is repeated for different values of output voltages.
5. All the readings are tabulated and Intrinsic Stand-Off ratio is calculated using
6. $\eta = (V_p - V_D) / V_{BB}$
7. .A graph is plotted between V_{EE} and I_E for different values of $V_{BE.}$

Observations:

At V_{BB}=5V constant		At V_{BB}=10V constant	
V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)

Calculations:

$V_P = \eta V_{BB} + V_D$

$\eta = (V_P - V_D) / V_{BB}$

$\eta = (\eta_1 + \eta_2 + \eta_3) / 3$

Result: The Emitter characteristics of a UJT are studied and plotted. The peak voltage (Vp) and valley voltage (Vv) for a given UJT are found.

1. The peak voltage (VP) of a UJT is _____.
2. The valley voltage (Vv) of a UJT is _____.

Conclusion:

1.

2.

Viva questions:

1. How many junctions exits in UJT?

2. What is relaxation oscillator?

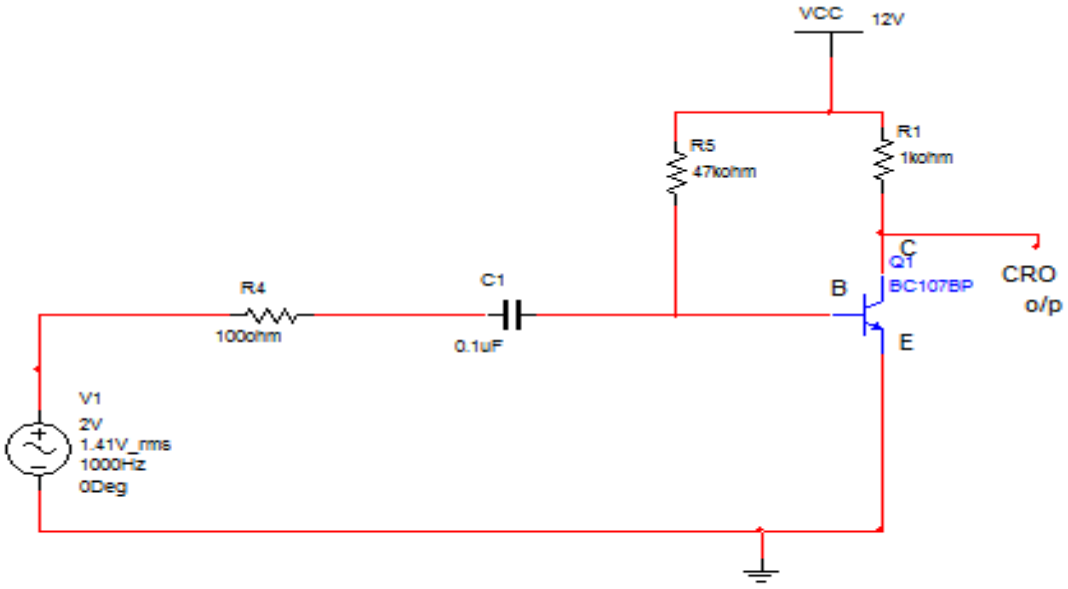
3. What are the applications of UJT?

4. What is the intrinsic stand-off ratio?

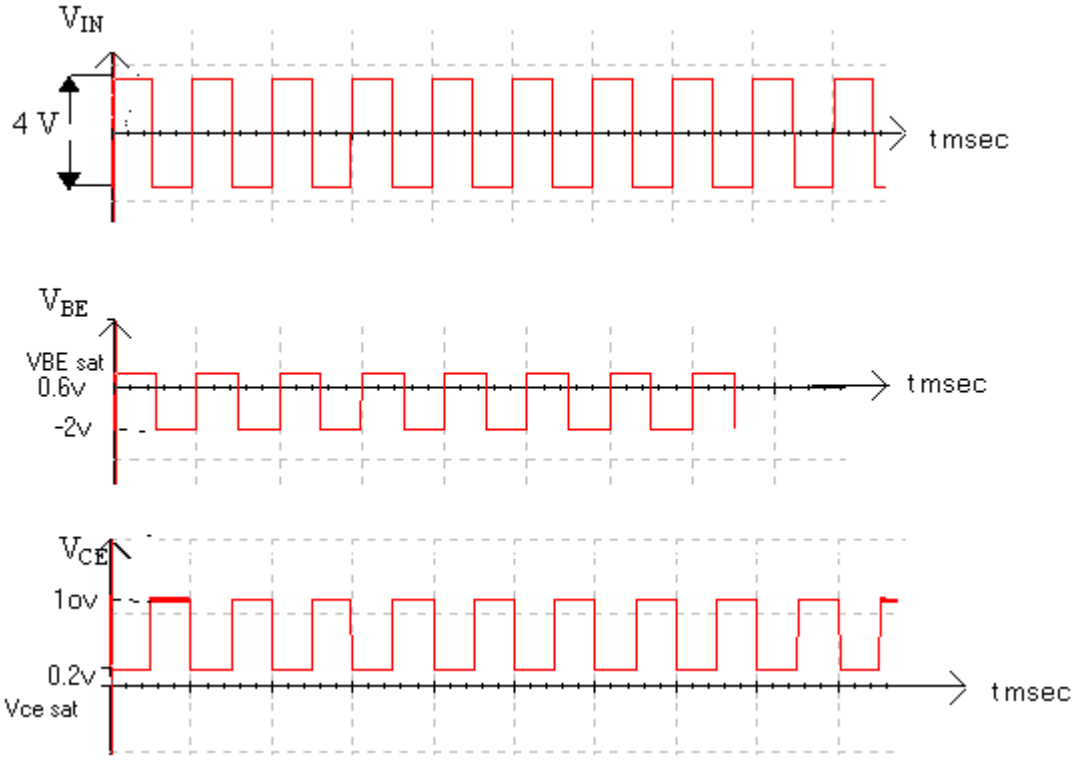
5. Why does negative resistance region appears in UJT?

Circuit Diagram

BJT as a Switch:



Model Waveforms



Exp: 10 **Date:**

TRANSISTOR AS A SWITCH

Aim: To simulate the operation of Transistor as a switch.

Software Required: Multisim software 14.1 version**.**

Hardware Required: Personal Computer

Theory:

A transistor can work in 3 regions i.e., Active region Saturation region and Cut-off region. When the transistor is connected in CE configuration the conditions for active region is base-emitter junction forward bias and collector-emitter junction reverse bias. In this region transistor can act as an amplifier.

When emitter to base junction and collector emitter junction both are forward bias the transistor is said to be in 'Saturation Region'.

When emitter to base junction and collector to emitter junction are reverse bias the transistor is said to be in 'Cut-off region'.

To operate transistor as a switch it is made to operate in saturation or cut-off region. If the switch is ON it is saturation region. If the switch is OFF it is in cut-off region.

A pulse train with sufficient amplitude is applied to the transistor base. When pulse is at high the emitter -base and collector-base junctions are forward bias.

Thus transistor enters into saturation or is ON. When pulse is at low both the junctions are reverse biased and the transistor is cut-off or open circuited.

Depending up on the base control voltage the switch may be ON or OFF.

Procedure:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar. Using component tool bar place all the components on the circuit window and wire the circuit.
2. Connect the circuit diagram as per the given specifications.
3. Applying the square wave voltage of 10V and frequency of 1000 Hz is applied to the circuit as an input.
4. Observe the response from oscilloscope.
5. Plot the graph for simulated output wave form.

Result:

Conclusion:

1.

2.

Viva questions:

1. What are the different switching times of a transistor?
2. What is the V_{BE} of a ON transistor?
3. Define OFF time of a transistor?
4. Explain how transistor acts as a switch?
5. What are the operating regions for transistor to act as a switch?

Circuit Diagram:

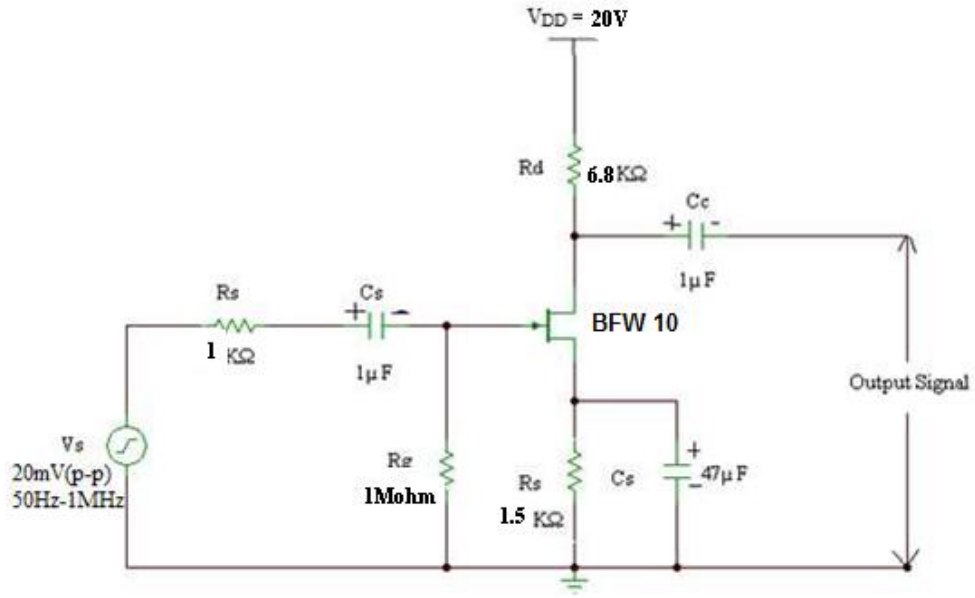


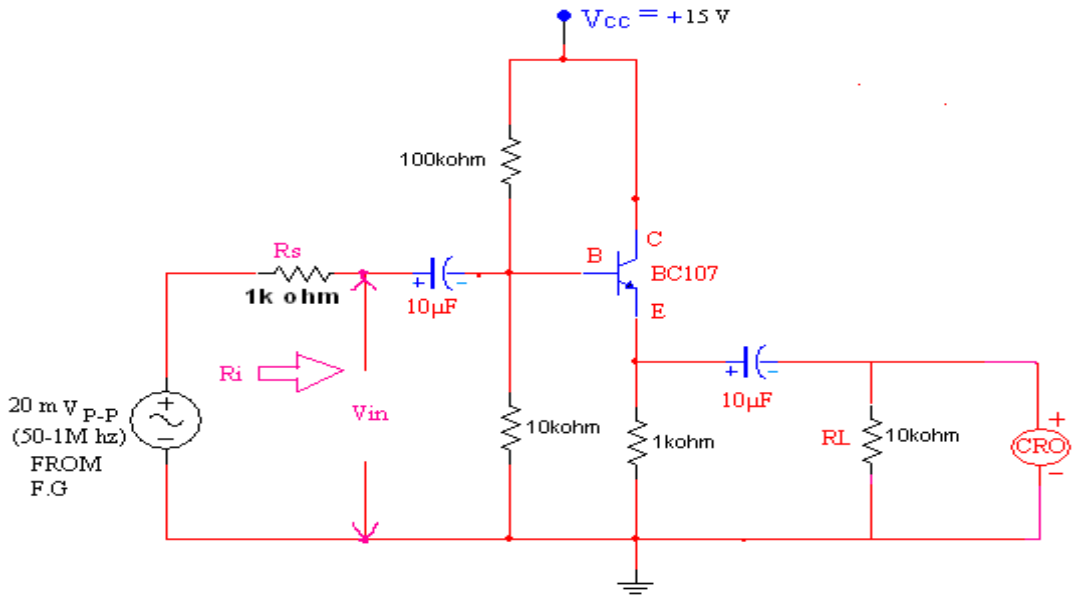
Fig (1) Common Source Amplifier

Tabular Column:

Source Voltage V_s= **Input Voltage V_i=**

S. No	Frequency (Hz)	O/P voltage (V_0)	Gain (V_0/ V_I)	Gain in dB 20*log10V_0 / V_I

Circuit Diagram:



Fig(1) Emitter Follower

Tabular Column: **Source Voltage V_S=** **Input Voltage, V_i =**

S.no.	Frequency (Hz)	Output voltage(v_0)(mV)	Voltage gain (A_v)=v_0/v_i	Gain (dB) 20 $\log_{10}\|A_v\|$

Exp: 11 **Date:**

COMMON EMITTER (Emitter Follower) AMPLIFIER

Aim: 1).To Obtain Frequency Response of Common Emitter Amplifier.

2).To Find voltage gain, current gain, input impedance, output impedance, and Bandwidth from Frequency Response curve

Software Required: Multisim software 14.1 version**.**

Hardware Required: Personal Computer

Theory:

The CE amplifier provides high gain &wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal.

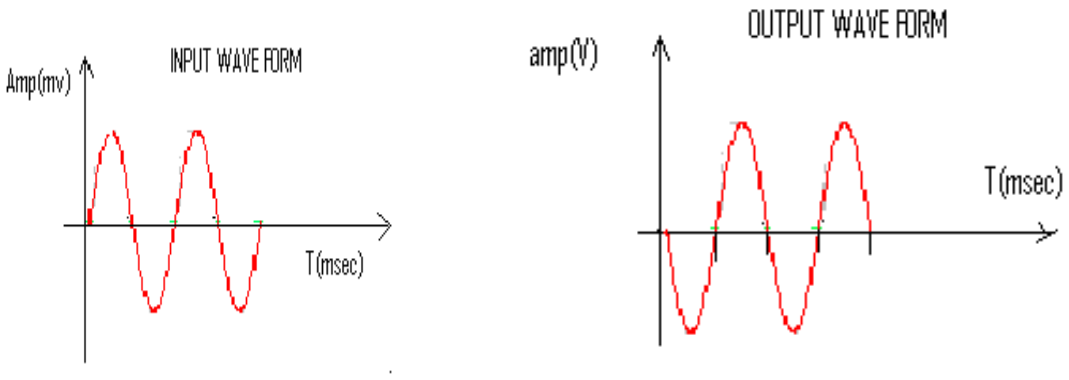
A very small change in base current produces a much larger change in collector current. When +VE half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage more –VE. Thus when input cycle varies through a -VE half-cycle, increases the forward bias of the circuit, which causes the collector current to increases thus the output signal is common emitter amplifier is in out of phase with the input signal.

Procedure:

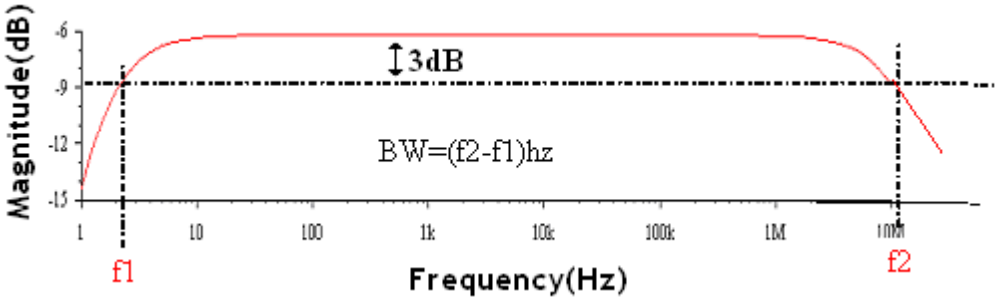
1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar. Using component tool bar place all the components on the circuit window and wire the circuit.
2. Connect the circuit diagram as per the given specifications. Simulate the circuit.
3. Observe the response from oscilloscope and obtain the magnitude plot.
4. Extract the output voltage from the magnitude plot and determine voltage gain in dB.
5. Plot the frequency response and determine bandwidth.

$$BW = f_2 - f_1.$$

Model waveforms:



Frequency response:



Calculations:

Voltage gain (A_v) =V_o/V_i =

Input resistance (R_i) =

$$Ri = \frac{Vi\ X\ Rs}{Vs - Vi}$$

Band width (BW) = $f_2 - f_1$ =

Precautions:

1. Avoid loose connections
2. Carefully note the readings from CRO without parallax error.
3. Carefully connect the transistor terminals.

Result:

Frequency Response of Common Emitter Amplifier is obtained.

Voltage gain A_V =

Input resistance R_i =

Bandwidth BW =

Conclusion:

1.

2.

Viva questions:

1. Define Amplifier.

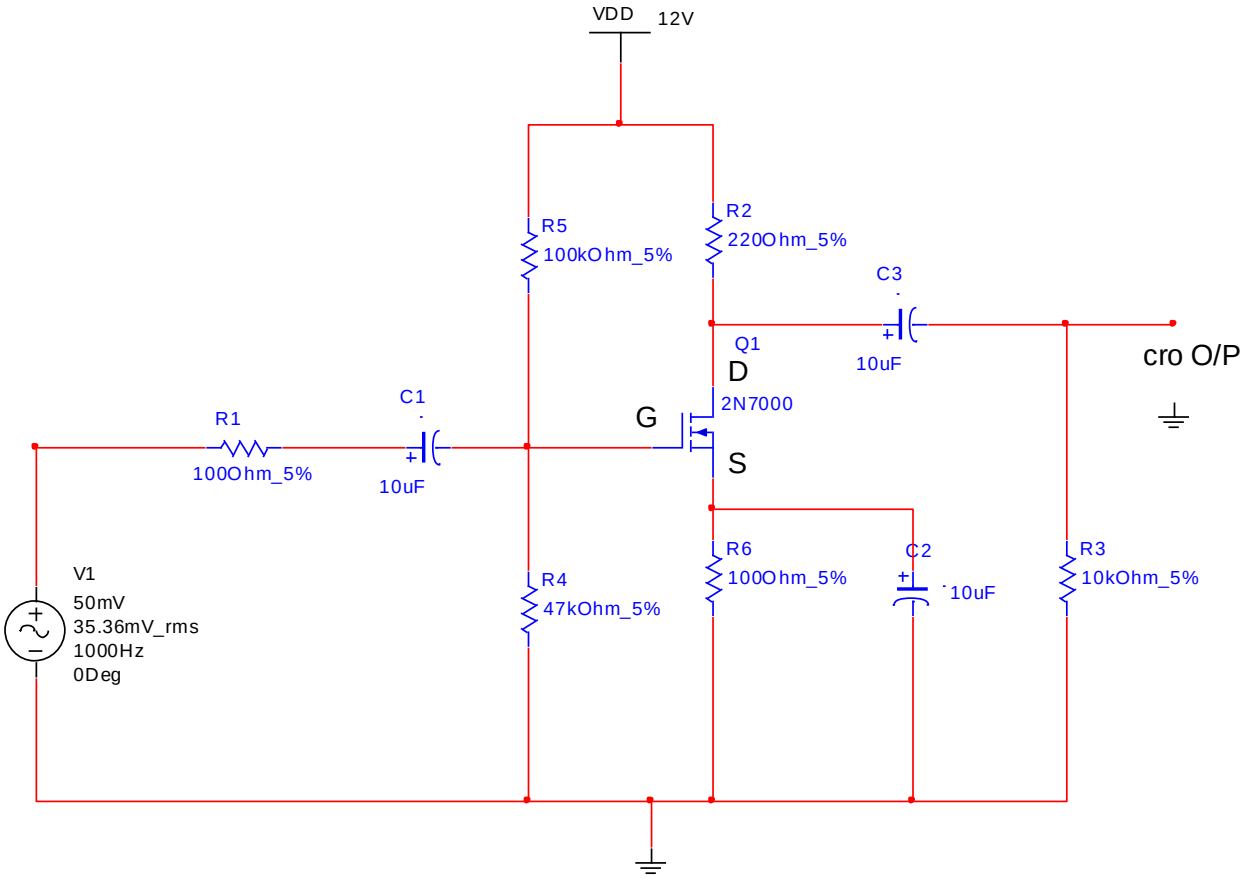
2. Define voltage gain.

3. What are the various types of biasing a Transistor?

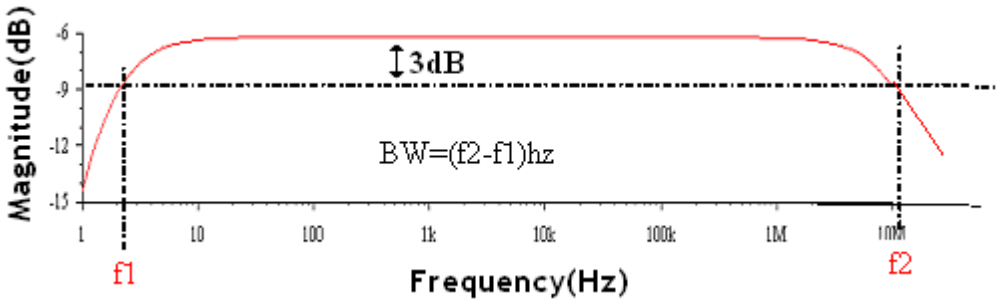
4. What are the Applications of CE amplifiers?

5. Draw the H-parameter equivalent circuit of CE amplifier.

Circuit Diagram:



Frequency response:



Exp: 12 **Date:**

MOSFET (common source) **AMPLIFIER**

Aim: 1).To Obtain Frequency Response of MOSFET (common source) Amplifier.

2).To Find voltage gain, current gain, input impedance, output impedance, and Bandwidth from Frequency Response curve

Software Required: Multisim software 14.1 version**.**

Hardware Required: Personal Computer

Theory:

Procedure:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar. Using component tool bar place all the components on the circuit window and wire the circuit.
2. Connect the circuit diagram as per the given specifications. Simulate the circuit.
3. Observe the response from oscilloscope and obtain the magnitude plot.
4. Extract the output voltage from the magnitude plot and determine voltage gain in dB.
5. Plot the frequency response and determine bandwidth.

$$BW = f_2 - f_1.$$

Tabular Column: **Input Voltage, V_i =**

S.no	Frequency (Hz)	Output voltage(v_0)(mV)	Voltage gain (A_v)=v_0/v_i	Gain(dB) 20 $\log_{10}\|A_v\|$

Result:

The Bandwidth of CS Amplifier is

BW = $f_H - f_{L=}$_____Hz.

Conclusion:

1.

2.

Viva questions:

1. What are the advantages of JFET over MOSFET?

2. What are the types of MOSFET?

3. Compare JFET and MOSFET?

4. Write equation of FET I_D in terms of V_{GS} and V_P?

5. What are the applications of MOSFET?

PART - B

HARDWARE LAB EXPERIMENTS

Circuit Diagram:

Forward Bias:

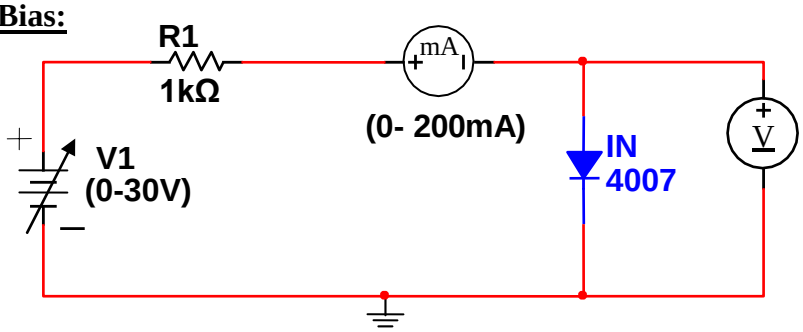


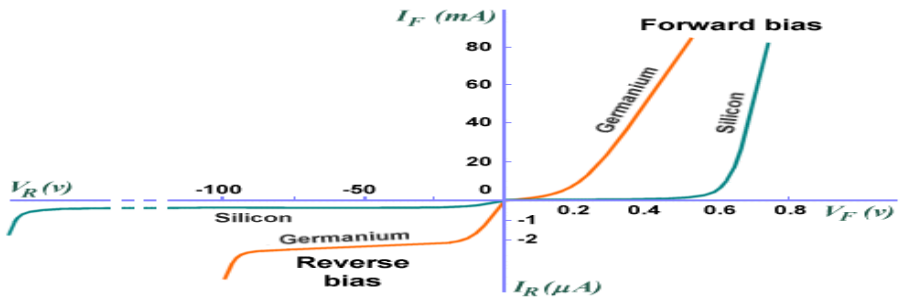
Fig. (1) Forward biased PN Junction Diode

Tabular column:

Forward bias:

S. No.	Silicon Diode	
	V_F(V)	I_F (mA)

Model Graph:



Volt Ampere Characteristics of PN Junction Diode

Exp: 01 **Date:**

PN- JUNCTION DIODE CHARACTERISTICS

Aim: 1. To plot the Volt - Ampere characteristics of given P–N junction Diode
2. To find the static, dynamic and reverse resistances.

Apparatus:

S. No.	Apparatus	Range/Rating	Quantity
1	Diode	1N4007	1
2	Resistors	1KΩ	1
3	DC Ammeter	0-200mA	1
		0-200µA	1
4	DC Voltmeter	0-30V	1
5	RPS	0-30V	1
6	Bread board	--	1
7	Connecting wires	--	Required

Procedure:

Forward Bias:

1. Connect the circuit as per the circuit diagram shown in Fig.(1).For Silicon Diode.
2. Vary the power supply in such a way that the readings are taken in steps of 0.1V, to the maximum reading of power supply of 30V.
3. Note down the corresponding Ammeter and Voltmeter readings.
4. Plot the graph between Forward voltage and current (V_F and I_F.)
5. Find the Static Forward Resistance $R_F = V/I\ \Omega$.
6. Find the Dynamic Forward Resistance $r_F = \frac{\Delta V}{\Delta I}\Omega$

Reverse Bias:

1. Connect the circuit as per the circuit diagram shown in Fig. (2).
2. Vary the power supply in such a way that the readings are taken in steps of 2V, to the maximum reading of power supply of 30V.
3. Note the corresponding Ammeter and Power Supply readings.
4. Plot the graph between V_R and I_R.
5. Find the Static Reverse Resistance.
6. Find the Dynamic Reverse Resistance.

Circuit Diagram:
Reverse bias:

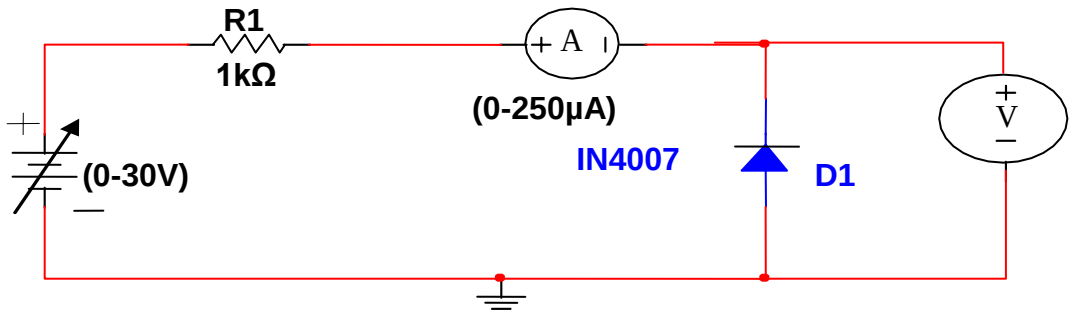


Fig. (2) Reverse biased PN Junction Diode

Tabular column
Reverse bias:

S. No.	Silicon Diode	
	V_r(V)	I_r(μA)

CALCULATIONS:
FORWARD BIAS:
Static Resistance = V/I

Dynamic Resistance = ΔV/ΔI

Cut in Voltage =

REVERSE BIAS:

Static Resistance = V/I

Dynamic Resistance = ΔV/ΔI

Breakdown Voltage =

Precautions:

1. Don't give voltage to the circuit beyond prescribed range.
2. Don't short circuit the output terminal of power supply.
3. Carefully connect meter terminals (+ and –).

Result:

Successfully verified operation of PN Junction diode under forward and reverse biased conditions and plotted Volt-Ampere Characteristics.

Determined the static and dynamic diode resistances from the plot.

1. Static Forward Resistance R_F =
2. Static Reverse Resistance R_r =
3. Dynamic Forward Resistance =
4. Dynamic Reverse Resistance =

Conclusion:

1.

2.

Viva questions:

1. What is Zener breakdown and avalanche break down?

2. Draw the symbols of special purpose diodes?

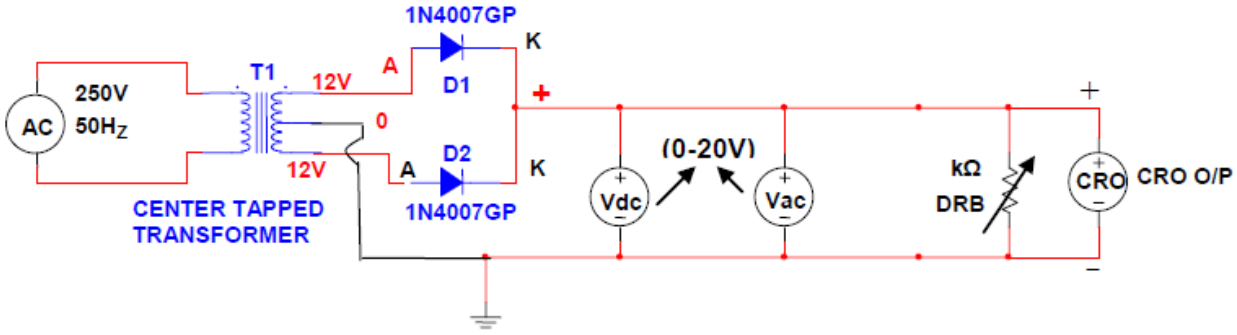
3. What is Barrier Potential?

4. How P-N Junction Formed?

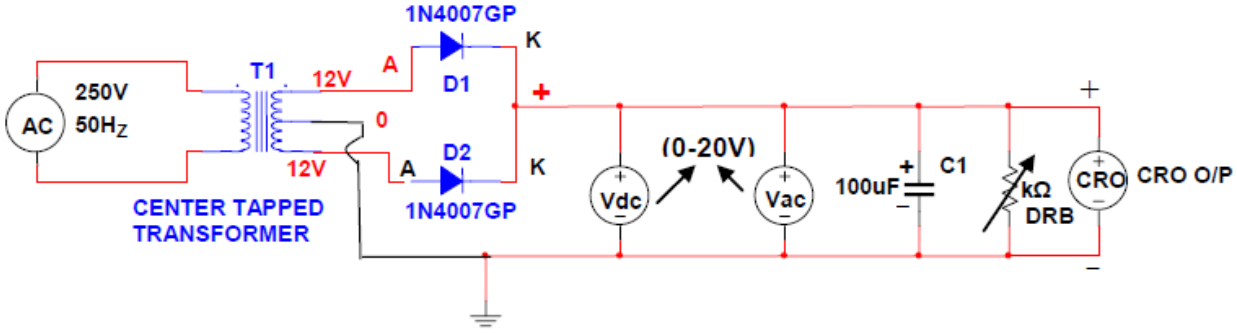
5. Why reverse saturation current is high in germanium than silicon?

CIRCUIT DIAGRAM:-

WITHOUT FILTER:-



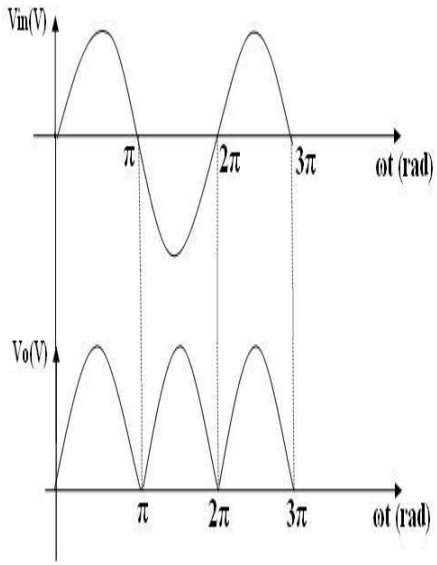
WITH FILTER:-

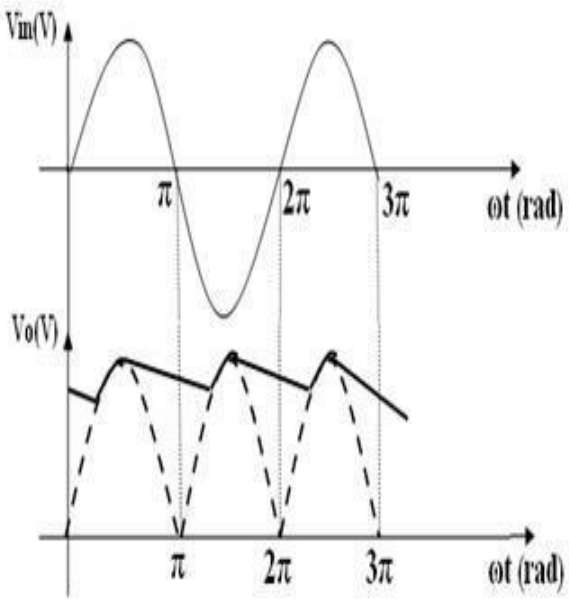


Model Waveforms:

input

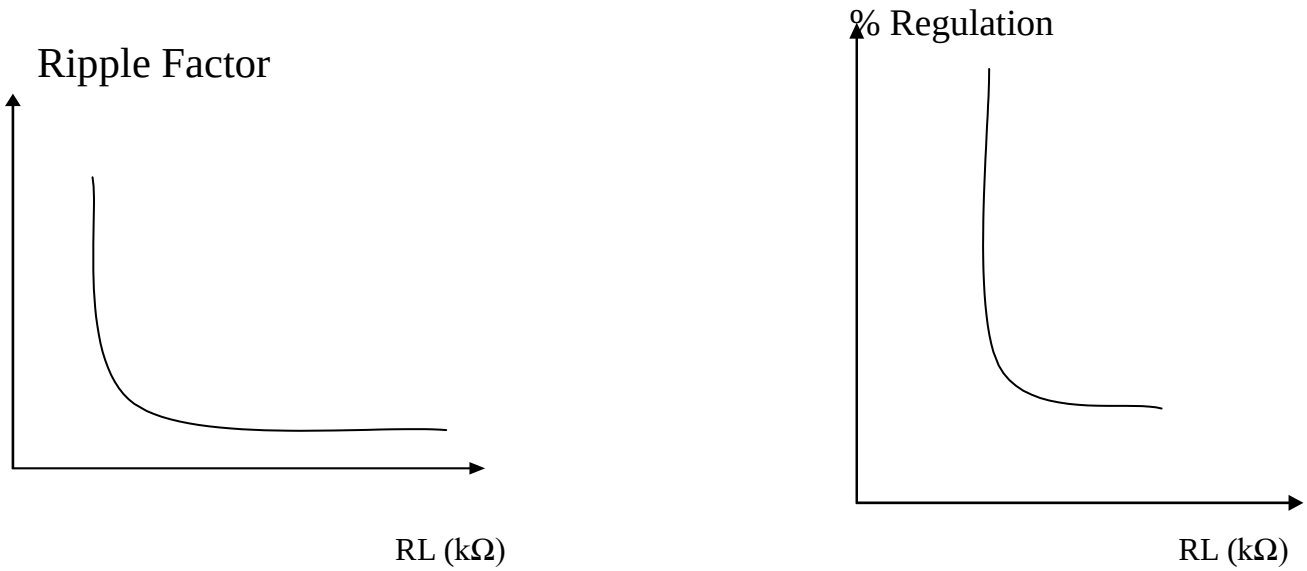
Output



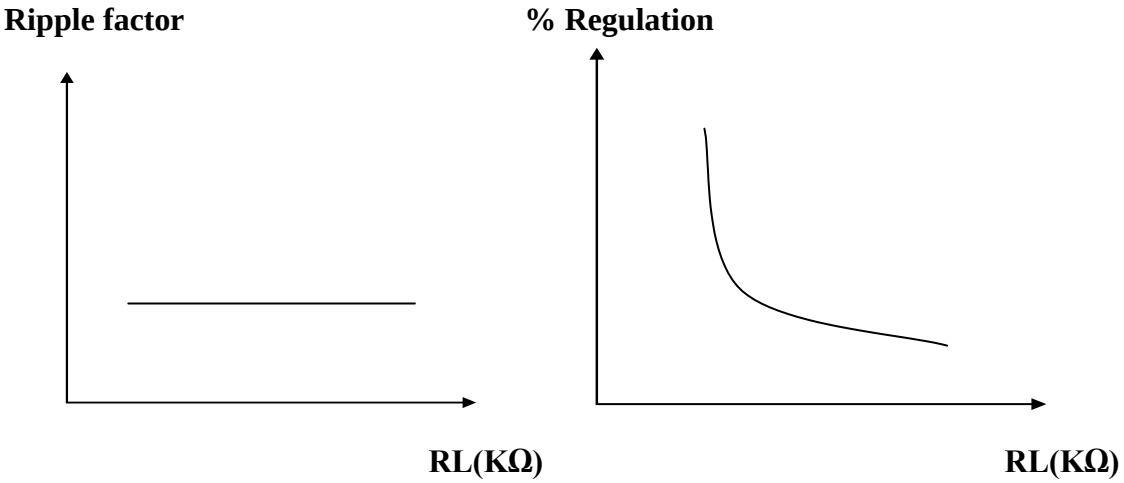


Model Graphs:

WITHOUT FILTER:-



WITH FILTER:-



Calculations:

Calculate the ripple factor (r) = $\frac{R.M.S\ VALUES\ OF\ A.C\ COMPONENT}{AVERAGE\ VALUE} = \frac{Vac}{Vdc}$

Calculate the Percentage of Regulation = $[(V_{dc0} - V_{dc})/V_{dc}]$ x 100
(or) $(V_{NL} - V_{FL})/V_{FL}$ X100

Exp:02 **Date:**

FULL WAVE RECTIFIER WITHOUT FILTER

Aim: To Find the Ripple factor and Percentage of Regulation of a Full Wave Rectifier with and without Filter.

Apparatus:

S. No.	APPARATUS	RANGE/RATING	QUANTITY
1	Step down transformer	230V/50 Hz: (12-0-12) V	1
2	Diode	1N4007	2
3	Decade Resistance Box(DRB)		1
4	Digital Multimeter (DMM)		1
5	Bread board	--	1
6.	capacitor	47µ	1
6	Connecting wires	--	Required

Procedure:

1. Connect the circuit as per the circuit diagram shown in Fig.
2. Note down the No Load DC Voltage V_{dc0} when $I_{dc} = 0$
3. Vary the load resistance R_L (DRB) and note down I_{dc} and V_{dc}, V_{ac} using Multi meter.
4. Calculate the ripple factor $r = \frac{RMS\ values\ of\ AC\ component}{Average\ value} = \frac{Vac}{Vdc}$
5. Calculate the Percentage of Regulation = $[(V_{dc0} - V_{dc})/V_{dc}]$ x 100

   (or) $(V_{NL} - V_{FL})/V_{FL}$ X100
6. Draw the following graphs:
   - Percentage of Regulation versus I_{dc} taking I_{dc} on x – axis.
   - I_{dc} versus Ripple factor

Precautions:

1. Don't short circuit the output terminal.
2. Carefully connect meter & electrolytic capacitors terminals (+ and –)
3. Carefully connect diode terminals (anodes and cathodes).

Result:

Successfully verified the operation of Full Wave Rectifier with and without filter circuit and calculated the Ripple factor and Percentage of Regulation.

Ripple Factor =

Percentage of Regulation =

Conclusions:

1.

2.

Viva Questions:

1. What is Rectification?

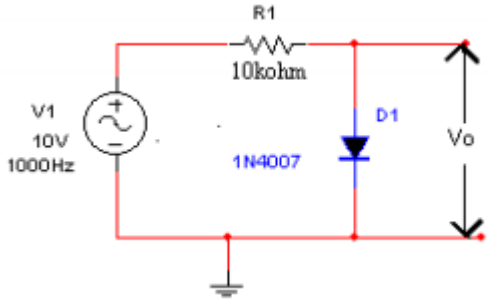
2. What is difference between HWR and FWR?

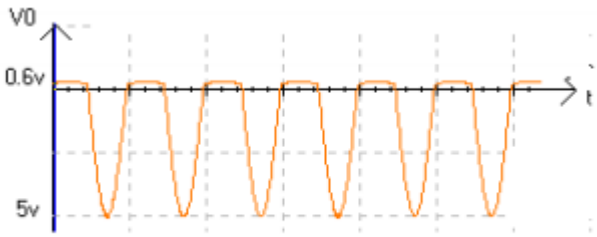
3. Define Step-up Transformer.

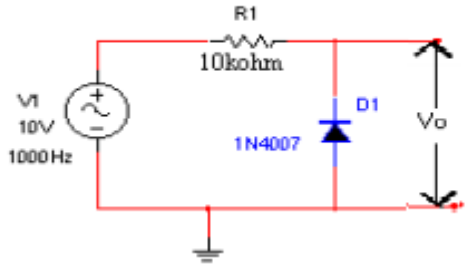
4. What are the types of Rectifier?

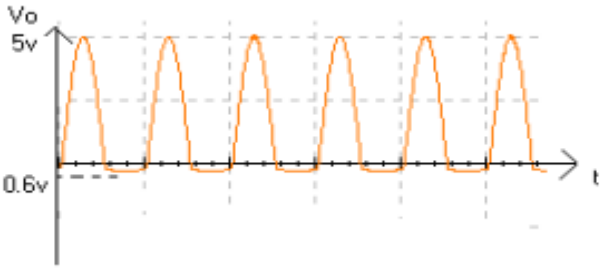
5. What is ripple?

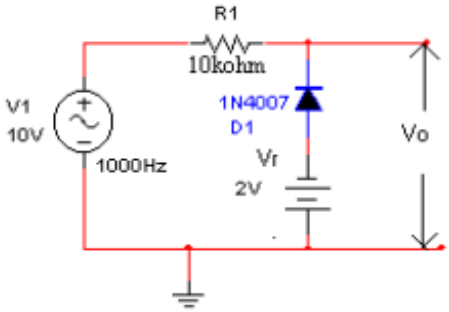
Clipper Circuits with their corresponding output waveforms:

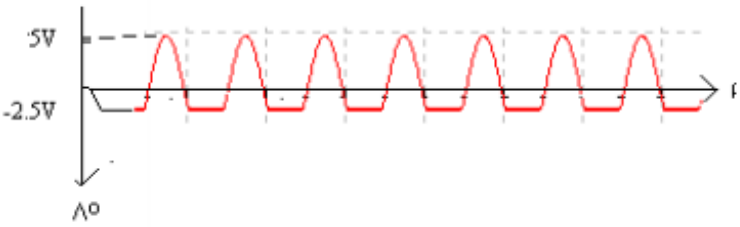


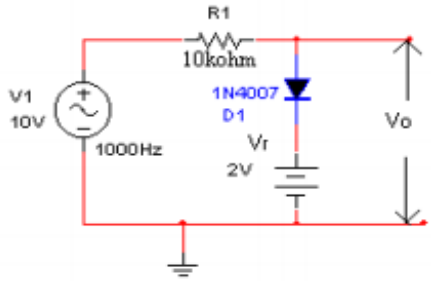


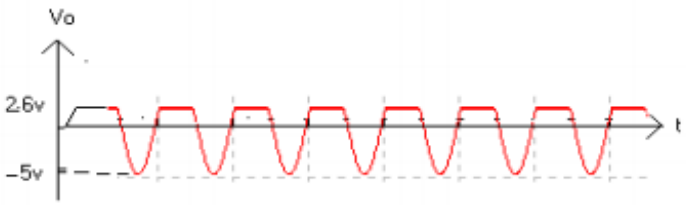












S. No	Waveform	Amplitude	Frequency
1.			
2.			
3.			
4.			

Exp: 3(A) **Date:**

DIODE APPLICATIONS-CLIPPERS & CLAMPERS

A). CLIPPERS

Aim: a) To study the clipping circuits using diodes.

b) To observe the transfer characteristics of all the clipping circuits in CRO.

Apparatus :

S. No.	APPARATUS	RANGE/RATING	QUANTITY
1	Regulated Power Supply	0 – 30 V	1
2	Diode 1N4007		2
3	Resistors	10 KΩ	1
4	Function Generator	0 – 30 V	1
5	CRO	20 MHz	1
7	Bread board	--	1
8	Connecting Wires	-	As required

Procedure:

1. Connect the circuit as per the circuit diagram in Figure 1.
2. In each case apply 10 VP-P, 1 KHz Sine wave I/P using a signal generator.
3. O/P is taken across the load R_L.
4. Observe the O/P waveform on the CRO and compare with I/P waveform.
5. Sketch the I/P as well as O/P waveforms and mark the numerical values.
6. Obtain the transfer characteristics of Fig.1, by keeping CRO in X-Y mode.
7. Repeat the above steps for all the clipping circuits.

Result:

The practical values

V= $\gamma + V_R$

V= $\gamma - V_R$

Clipping circuits for different reference voltages are studied.

Conclusion:

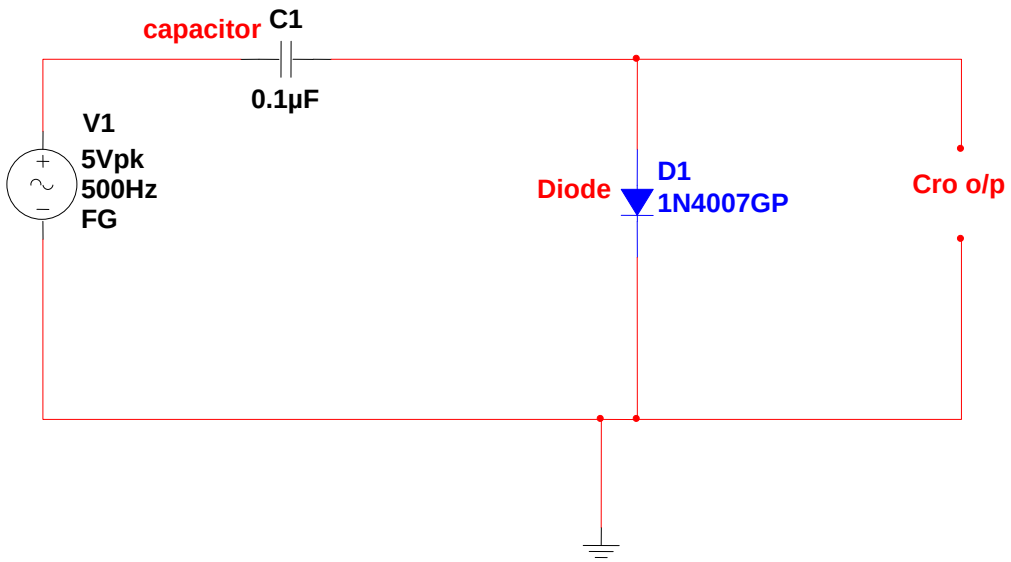
1.

2.

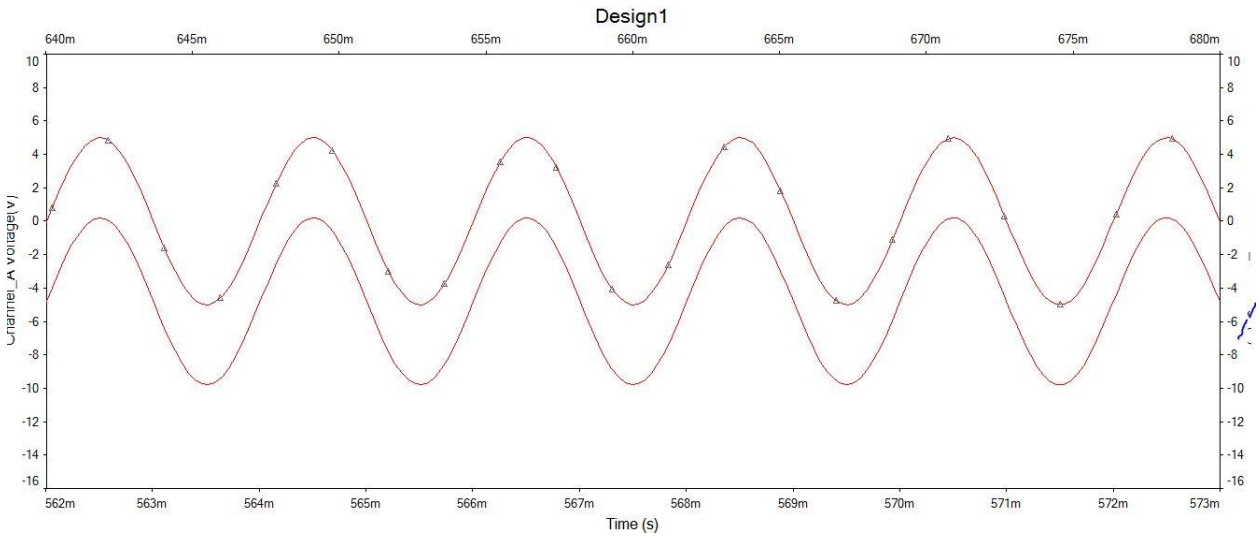
Viva questions:

1. Define clipping? Describe (i) Positive clipper (ii) Biased Clipper (iii) Combination clipper.
2. Define clamping?
3. Define peak inverse voltage of diode?
4. What are the other names for the clamper?
5. List different types of Clippers.

Circuit Diagram: Clamper Circuit :



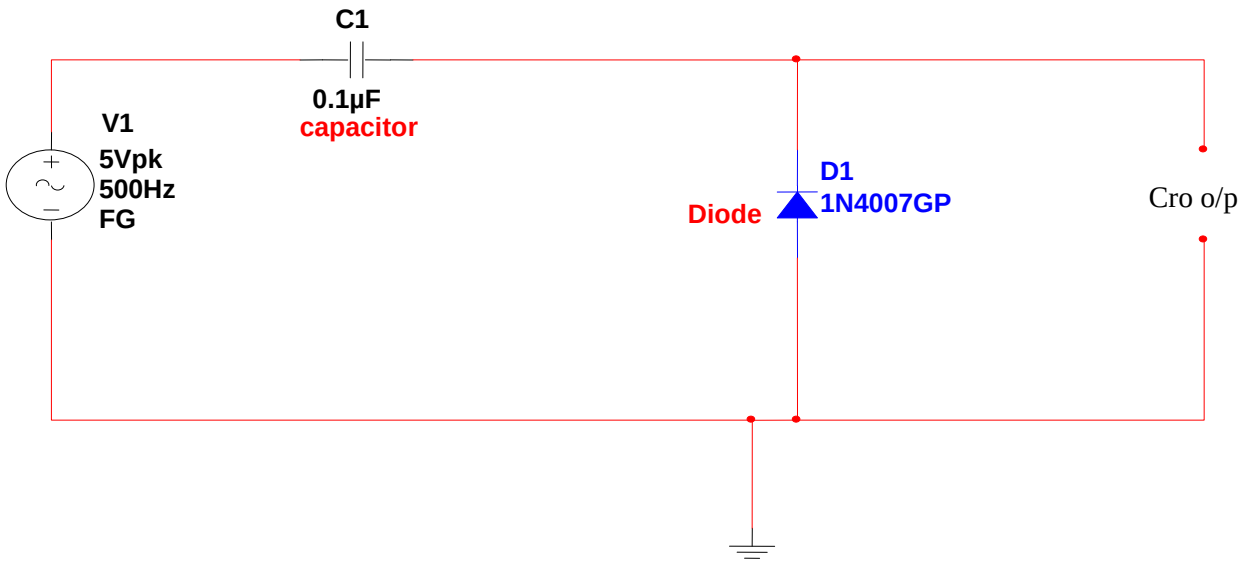
Input and Output waveform:



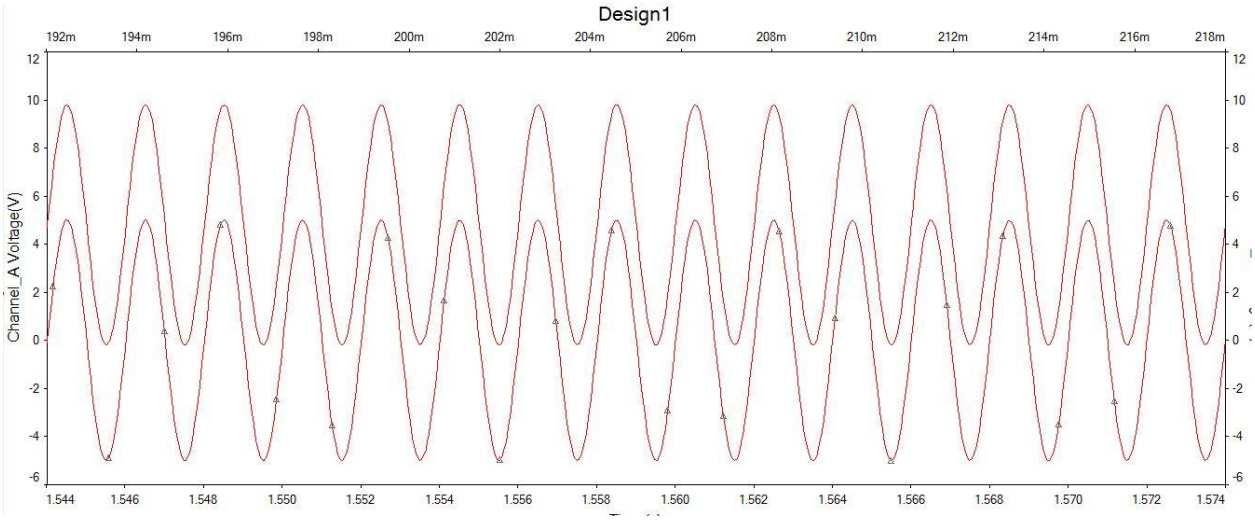
Tabular column:

S. No	Waveform	Amplitude	Frequency (time period)
1.			

Circuit Diagram: Clamper Circuit:



Input and Output waveform:



Tabular column:

S. No	Waveform	Amplitude	Frequency (time period)
1.			

Exp: 3(b) **Date:**

CLAMPERS

Aim: To study the clamping circuits.

Apparatus:

S. No.	APPARATUS	RANGE/RATING	QUANTITY
1	Regulated Power Supply	0 – 30 V	1
2	Diode	1N4007	1
3	Capacitors	0.1 µF	1
4	Function Generator	0 – 30 MHz	1
5	CRO	20 MHz	1
6	Bread board	--	1
7	Connecting Wires	-	As required

Procedure:

1. Connect the circuit as per the circuit diagram in Figure 1.
2. In each case apply 10 VP-P, 1 KHz Sine wave I/P using a signal generator.
3. O/P is taken across the load R_L.
4. Observe the O/P waveform on the CRO and compare with I/P waveform.
5. Sketch the I/P as well as O/P waveforms and mark the numerical values with V_R = 2V, 3V.
6. Repeat the above steps for all the clamping circuits.

Result:

Conclusion:

1.

2.

Viva questions:

1. List different types of clampers.

2. Define series positive clipper.

3. Define clamper.

4. Define biased clamper.

5. What are the applications of clampers?'

Circuit Diagram:

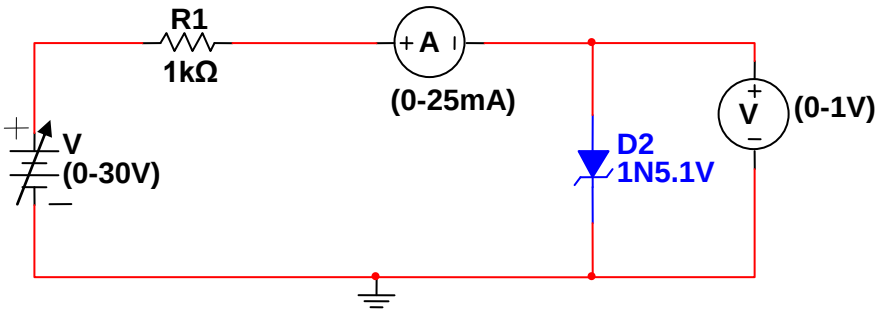


Fig. 1: V-I CHARACTERISTICS:

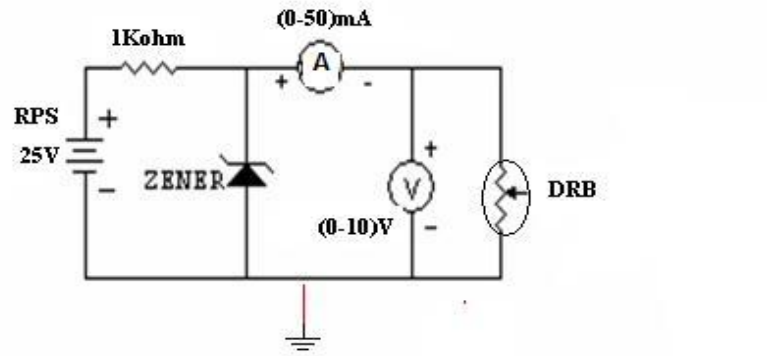
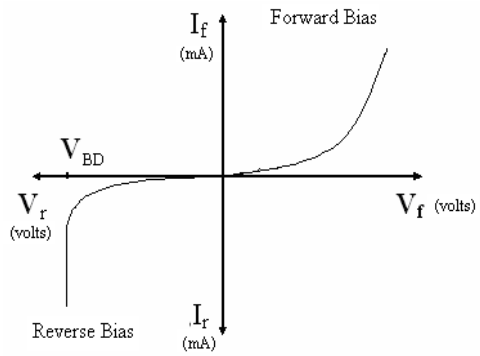
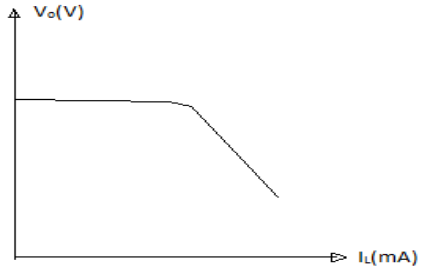


Fig. 2.Zener Diode based Voltage Regulator

Model Graph:



Regulation Characteristics



V-I Characteristics

Exp:04 **Date:**

ZENER DIODE BASED VOLTAGE REGULATOR

Aim:

To design and verify the Zener diode based voltage regulator.

Apparatus :

S.No.	APPARATUS	RANGE/RATING	QUANTITY
1	Zener Diode	5.1V	1
2	Resistors	1KΩ	1
3	DC Ammeter	0-50mA	1
4	DC Voltmeter	0-1V	1
		0-10V	1
5	RPS	0-30V	1
6	Bread board	--	1
7	DRB		1
8	Connecting wires	--	As Required

Procedure:

Load Regulation Characteristics:

1. Connect the circuit as per the circuit diagram in figure 1.
2. Fix the DC supply at 20V.
3. By varying the load resistances tabulate the load voltage V_L and load current I_L.
4. Plot the graph between load voltages V_L and load current I_L.

Precautions:

1. Carefully connect the meter terminals (+ and –).
2. Carefully connect the Zener diode terminals (Anode & Cathode)

Result:

1. Volt – Ampere Characteristics of Zener Diode are plotted.
2. Zener Break Down Voltage =
3. Dynamic Forward Resistance =
4. Dynamic Reverse Resistance =

Tabular column:

(i). V-I CHARACTERISTICS:

S.No	Zener Voltage (V_Z) (volts)	Zener Current (I_Z) (mA)

(ii).Zener Diode based Voltage Regulator:

S. No.	R_L	Voltage across Load V_L(V)	Current through the load resistance I_L (mA)

Conclusions:

1.

2.

Viva Questions:

1. Define what is Zener voltage?

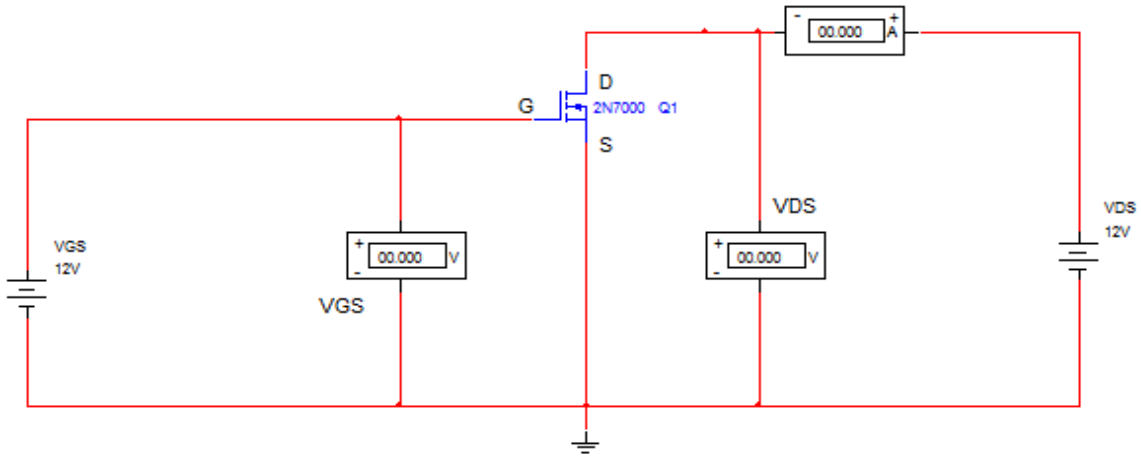
2. What is break down? What are its types?

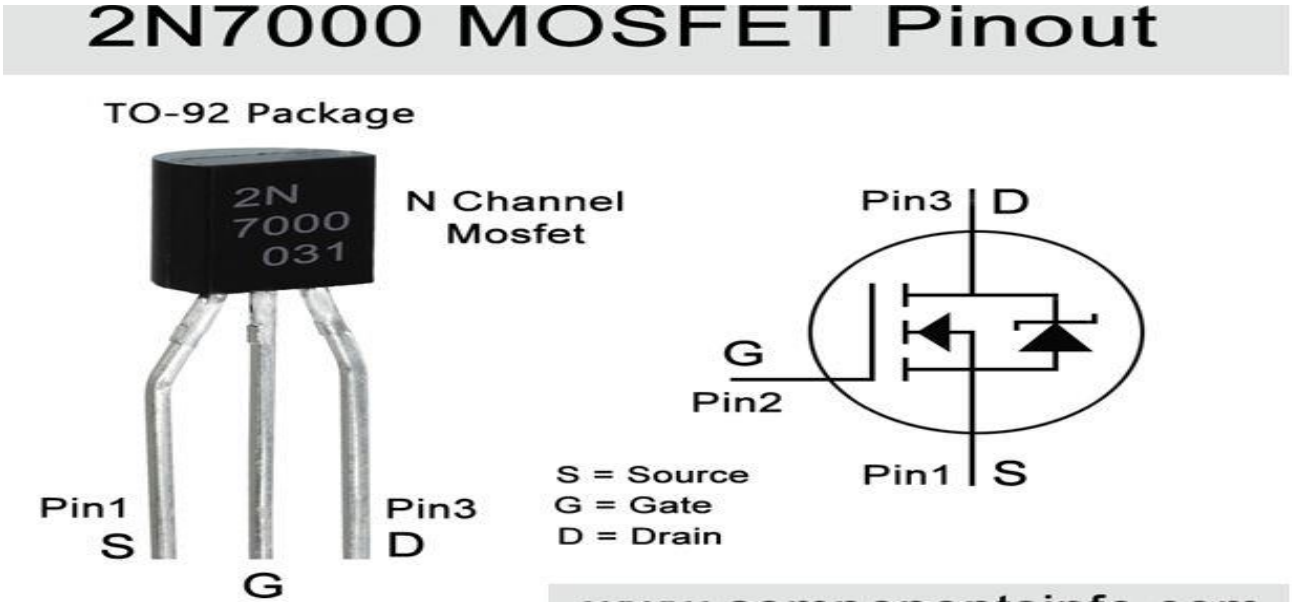
3. Why is Zener diode used as a voltage regulator?

4. What is avalanche break down?.

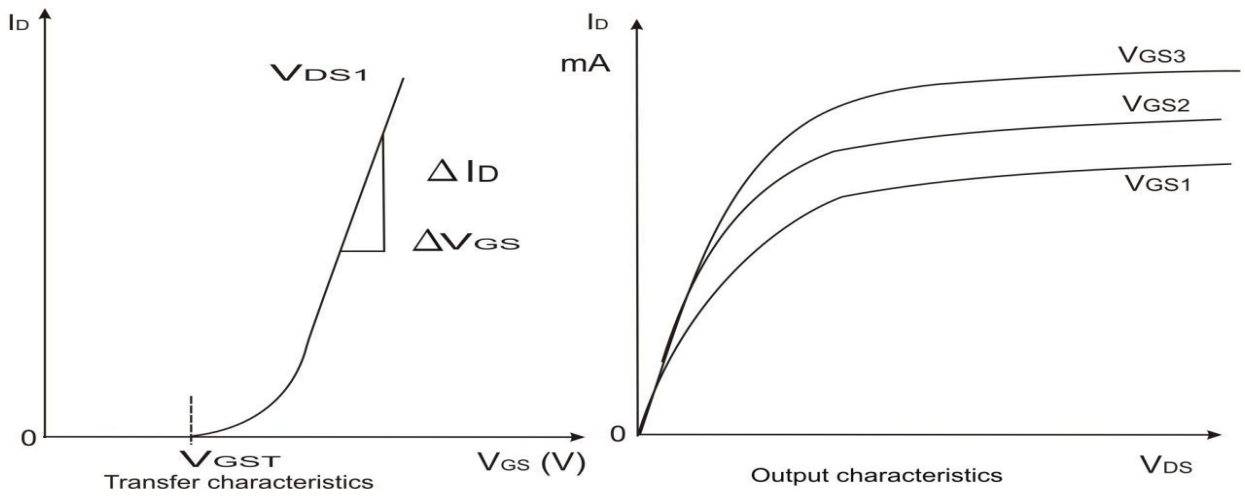
5. .How does the avalanche breakdown voltage vary with temperature.

CIRCUIT DIAGRAM OF MOSFET CHARACTERISTICS:





Model Graph:



Exp: 5 CHARACTERISTICS OF MOSFET **Date:**

Aim: To plot the Transfer and Drain characteristics of MOSFET and determine Trans conductance and output Resistance in Enhancement mode.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QTY
1.	MOSFET	2N7000	1 No
2.	Resistor	560Ω	1 No
3.	Ammeter (DC)	0-100mA	2 No
4.	Voltmeter (DC)	0-30V	2 No
5.	RPS	0-30V	1No
6.	Connecting wires		As per required

Theory:

A MOSFET (Metal oxide semiconductor field effect transistor) has three terminals called Drain, Source and Gate. MOSFET is a voltage controlled device. It has very high input impedance and works at high switching frequency.

MOSFET's are of two types 1) Enhancement type 2) Depletion type.

Procedure:

A).Transfer characteristics

1. Make the connections as per the circuit diagram.
2. Initially keep V1 and V2 at 0 V.
3. Switch ON the regulated power supplies. By varying V1, set VDS to some constant voltage say 5V.
4. Vary V2 in steps of 0.5V, and at each step note down the corresponding values of VGS and ID. (Note: note down the value of VGS at which ID starts increasing as the threshold voltage).
5. Reduce V1 and V2 to zero.
6. By varying V1, set VDS to some other value say 10V.
7. Repeat step 4.
8. Plot a graph of VGS versus ID for different values of VDS.

B) Drain or Output Characteristics:

1. Make the connections as per the circuit diagram.
2. Initially keep V1 and V2 at zero volts.
3. By varying V2, set VGS to some constant voltage (must be more than Threshold voltage).
4. By gradually increasing V1, note down the corresponding value of VDS and ID. (Note: Till the MOSFET jumps to conducting state, the voltmeter which is connected across device as VDS reads approximately zero voltage. Further increase in voltage by V1 source cannot be read by VDS, so connect multimeter to measure the voltage and tabulate the readings in the tabular column).
5. Set VGS to some other value (more than threshold voltage) and repeat step 4.
6. Plot a graph of VDS versus ID for different values of VGS.

Result:

1. The drain and transfer characteristics of a given MOSFET are drawn.
2. The drain resistance (rd), amplification factor (μ) and Trans-conductance (gm) of the Given MOSFET are calculated.

(i) The drain resistance (rd) of MOSFET is _____

(ii) Trans-conductance (gm) of MOS FET is_____

(iii) Amplification factor (μ) of MOSFET is_____

Tabular columns:

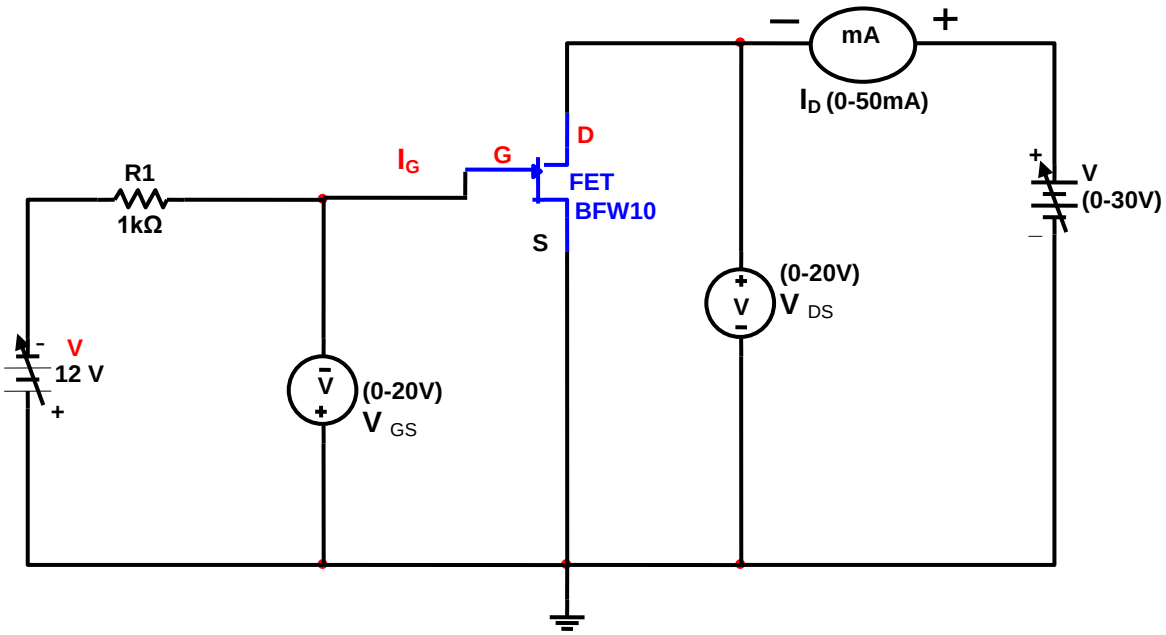
Drain Characteristics:

S.No	V_{GS}= 1.1 V		V_{GS}= 1.2V	
	V_{DS}(V)	I_D (mA)	V_{DS}(V)	I_D (mA)

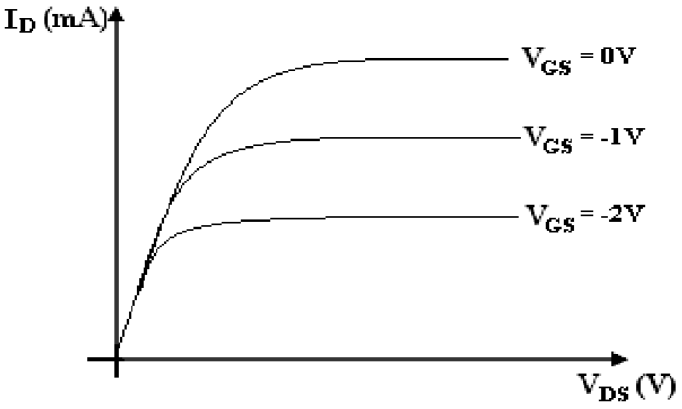
Transfer characteristics:

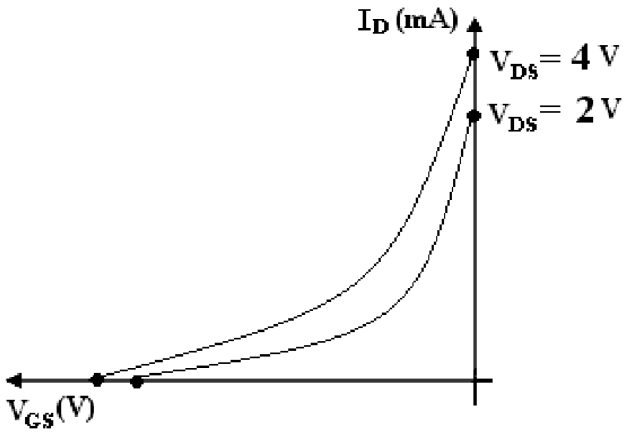
S.No	V_{DS}= 2V	
	V_{GS}(V)	I_D (mA)

Circuit diagram:

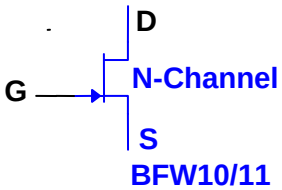


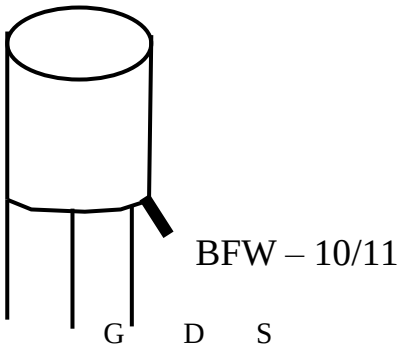
Model graphs:





PIN DETAILS OF FET :





Exp: 06 **Date:**

FET CHARACTERISTICS (IN CS CONFIGURATION)

Aim: 1.To obtain Drain and Transfer Characteristics of FET connected in Common Source configuration.

2. To Obtain $r_{d,}$ g_m and μ of FET.

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	Power Supply(RPS)	0-30V	2
2	Transistor-FET	BFW 10/11	1
3	DC Ammeter	0-50mA	1
4	DC Voltmeter	0–10V	1
5	Digital Multimeter (DMM)		1
6	Resistor	1KΩ	1
7	Bread board	--	1
8	Connecting wires	--	Required

Theory:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with VDS. With increase in ID the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The VDS at this instant is called “pinch off voltage” .If the gate to source voltage (VGS) is applied in the direction to provide additional reverse bias, the pinch off voltage ill is decreased. In amplifier application, the FET is always used in the region beyond the pinch-off.

$$I_{DS} = I_{DSS} (1-V_{GS}/V_P) \text{ ^2}$$

Result:

1. The drain and transfer characteristics of a given FET are drawn.
2. The drain resistance (rd), amplification factor (μ) and Trans-conductance (gm) of the Given FET are calculated.

(i) The drain resistance (rd) of FET is _____

(ii) Trans-conductance (gm) of FET is_____

(iii) Amplification factor (μ) of FET is_____

Procedure:-

Output (or) drain characteristics:

1. Connect the circuit as per the circuit diagram shown in Fig (1).
2. Simulate the circuit.
3. Set V_{GS} = 0V by adjusting $V_{GG.}$
4. Vary the supply voltage V_{DD} and note the readings of I_D and V_{DS}.
5. Repeat the above procedure for V_{GS} = –1V and –2V.
6. Plot the output characteristics V_{DS} Vs I_D for constant values of V_{GS} = 0 V, –1V and –2 V.
7. Find Drain Resistance $r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}}$ = Constant and Amplification Factor,

$\mu = g_m * r_d$

Procedure:

Transfer characteristics:

1. Connect the circuit as per the circuit diagram shown in Fig (1).
2. Simulate the circuit.
3. Set V_{DS}= 2V by adjusting $V_{DD.}$
4. Vary the input voltage V_{GG} and note the readings of I_D and V_{GS}.
5. Repeat the above procedure for V_{DS}= 4V.
6. Plot the transfer characteristics V_{GS} Vs I_D for constant values of V_{DS}= 2V and 4V.
7. Find Trans Conductance $g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}}$ = Constant

Tabular columns:

Transfer characteristics:

S.No	V_{GS}= 0 V		V_{GS}= –1V	
	V_{DS}(V)	I_D (mA)	V_{DS}(V)	I_D (mA)

Drain characteristics:

S.No	V_{DS}= 2 V		V_{DS}= 4 V	
	V_{GS}(V)	I_D (mA)	V_{GS}(V)	I_D (mA)

RESULT:

Conclusion:

1.

2.

Viva Questions:

1. What are the advantages of FET over BJT?

2. Is JFET is a bipolar device?

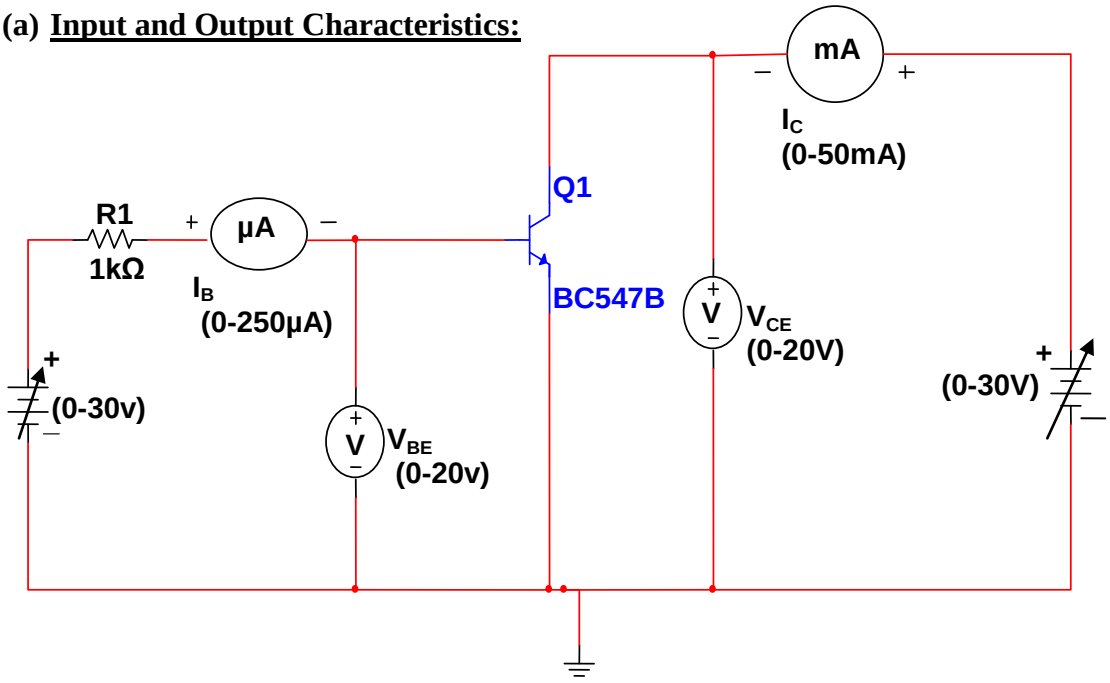
3. How many terminals exist in FET?

4. Differentiate BJT and FET.

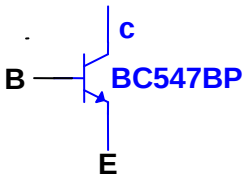
5. Why FET is called field effect transistor?

Circuit diagram:

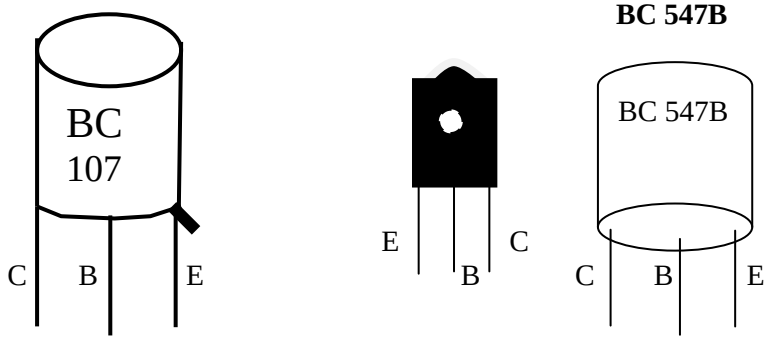
(a) Input and Output Characteristics:



SYMBOL OF TRANSISTOR:

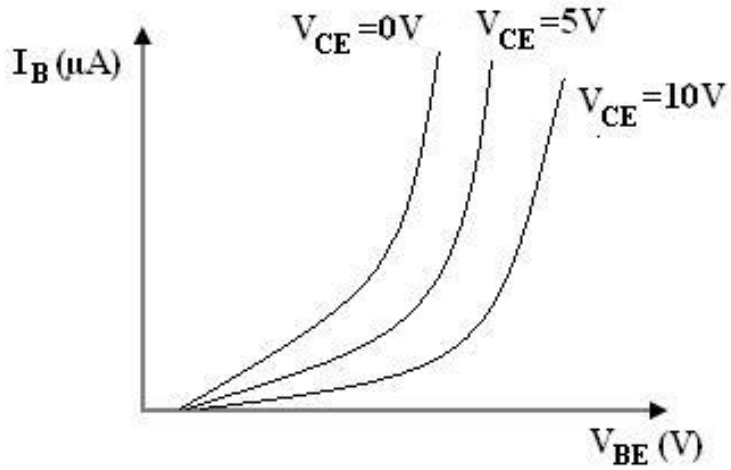


PIN DETAILS OF TRANSISTOR :

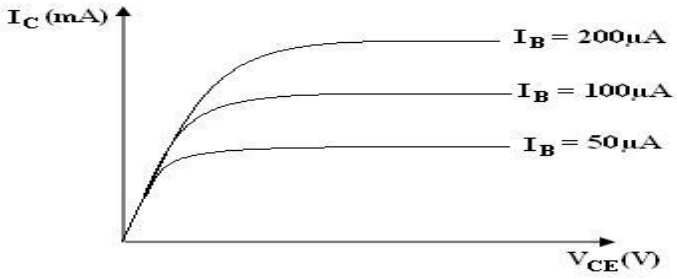


Model Graph:

Input characteristics:



Output characteristics:



Typical values:-

h_{ie}	h_{re}	h_{fe}	h_{oe}
1100Ω	2.5×10^{4}	50	25μΩ

Exp: 07 **Date:**

BJT CHARACTERISTICS (CE CONFIGURATION)

Aim: 1. To Obtain Input and Output characteristics of transistor connected in Common Emitter Configuration.

2. To determine the h-parameters for CE configuration.

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	Power Supply(RPS)	0-30V	1
2	Transistor	BC107or BC 547	1
3	DC Ammeter	0-50mA	1
		0–500mA	1
4	DC Voltmeter	0–10V	1
		0 – 1V	1
5	Digital Multimeter (DMM)		1
6	Resistor	10KΩ	1
7	Bread board	--	1
8	Connecting wires	--	Required

Theory:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal `is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement IB increases less rapidly with VBE. Therefore input resistance of CE circuit is higher than that of CB circuit. The output characteristics are drawn between Ic and VCE at constant IB. the collector current varies with VCE unto few volts only. After this the collector current becomes almost constant, and independent of VCE. The value of VCE up to which the collector current changes with V CE is known as Knee voltage. The transistor always operated in the region above Knee voltage, IC is always constant and is approximately equal to IB. The current amplification factor of CE configuration is given by

$$\beta = \Delta I_C / \Delta I_B$$

Procedure:

Input characteristics:

1. Connect the circuit as per the circuit diagram shown in Fig (1)
2. Simulate the circuit.
3. Set V_{CE} = 0 by adjusting V_{CC}.
4. Vary the input voltage V_{BB} and note the readings of I_B and V_{BE}.
5. Repeat the above procedure for V_{CE} = 2Vand 5V.
6. Plot the input characteristics V_{BE} Vs I_B for constant Values of V_{CE} = 0V, 2Vand 5V
7. Calculate h- parameters from input characteristics graph

$$\mathbf{V_{BE} = h_{ie}\, I_B + h_{re}\, V_{CE}}$$
$$\mathbf{I_C = h_{fe}\, I_B + h_{oe}\, V_{CE}}$$

a) Reverse voltage gain $h_{re} = \left.\frac{\Delta V_{EB}}{\Delta V_{CB}}\right|_{I_B \text{ Constant}}$

b) Input Impedance $h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} \text{ Constant}}$

Output characteristics:

1. Connect the circuit as per the circuit diagram shown in fig (2).
2. Simulate the circuit.
3. Set I_B = 50 μA by adjusting $V_{BB.}$
4. Vary the supply voltage V_{CC} and note the readings of I_C and V_{CE}. Take V_{CE}=V_{CC}.
5. Repeat the above procedure for I_B = 100 μA and 200 μA,
6. Plot the output characteristics V_{CE} vs I_C for constant Values of I_B =50 μA, 100 μA and 200 μA.
7. Calculate h- parameters from output characteristics graph

c. Output admittance $h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B \text{ Constant}}$

d. Forward current gain $h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} \text{ Constant}}$

Tabular column:
(a)Input characteristics:

S.NO	V_{CE}=		V_{CE}=	
	V_{BE}(V)	I_B (μA)	V_{BE}(V)	I_B (μA)

Tabular column:
b). output characteristics

S.No	I_B=		I_B=	
	V_{CE}(V)	I_C (mA)	V_{CE}(V)	I_C (mA)

Calculations:

1. Reverse voltage gain $h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \Big/ I_B$ Constant =
2. Input Impedance $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \Big/ V_{CE}$ Constant =
3. Output admittance $h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} \Big/ I_B$ Constant =
4. Forward current gain $h_{fe} = \frac{\Delta I_C}{\Delta I_B} \Big/ V_{CE}$ Constant =

Result: The input and output characteristics of a transistor in CE configuration are drawn. The Input (Ri) and Output resistances (Ro) of a given transistor are calculated.

1. The Input resistance (Ri) of a given Transistor is_____
2. The Output resistance (Ro) of a given Transistor is_____
3. The Current amplification factor is_____

Conclusion:

1.

2.

Viva questions:

1. What is a transistor?

2. What are the different types of BJT?

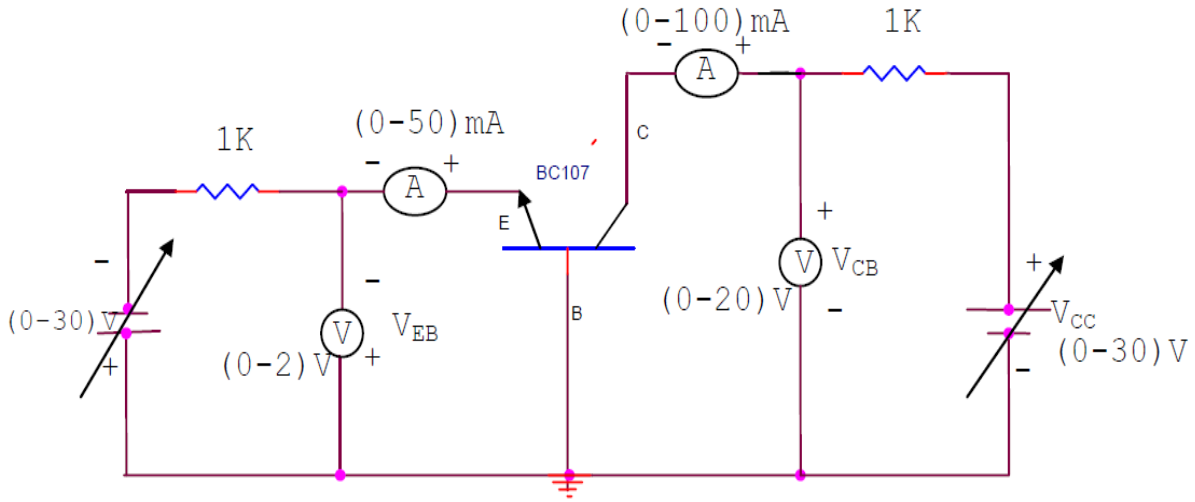
3. Define Cut-off, active and saturation regions?

4. What are the different configuration of transistor?.

5. What is meant by Q-Point?

Circuit diagram:

(a)Input Characteristics:



Tabular column:

(a)Input characteristics:

S.NO	V_{CB}=		V_{CB}=		V_{CB}=	
	V_{EB}(V)	I_E (mA)	V_{EB}(V)	I_E (mA)	V_{EB}(V)	I_E (mA)

Exp: 08 **Date:**

BJT CHARACTERISTICS (CB CONFIGURATION)

Aim: 1. To Obtain Input and Output characteristics of transistor connected in Common Base Configuration.

2. To determine the h-parameters for CB configuration.

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	Power Supply(RPS)	0-30V	1
2	Transistor	BC107or BC 547	1
3	DC Ammeter	0-50mA	1
		0–100 mA	1
4	DC Voltmeter	0–10V	1
5	Digital Multimeter (DMM)		1
6	Resistor	1KΩ	2
7	Bread board	--	1
8	Connecting wires	--	Required

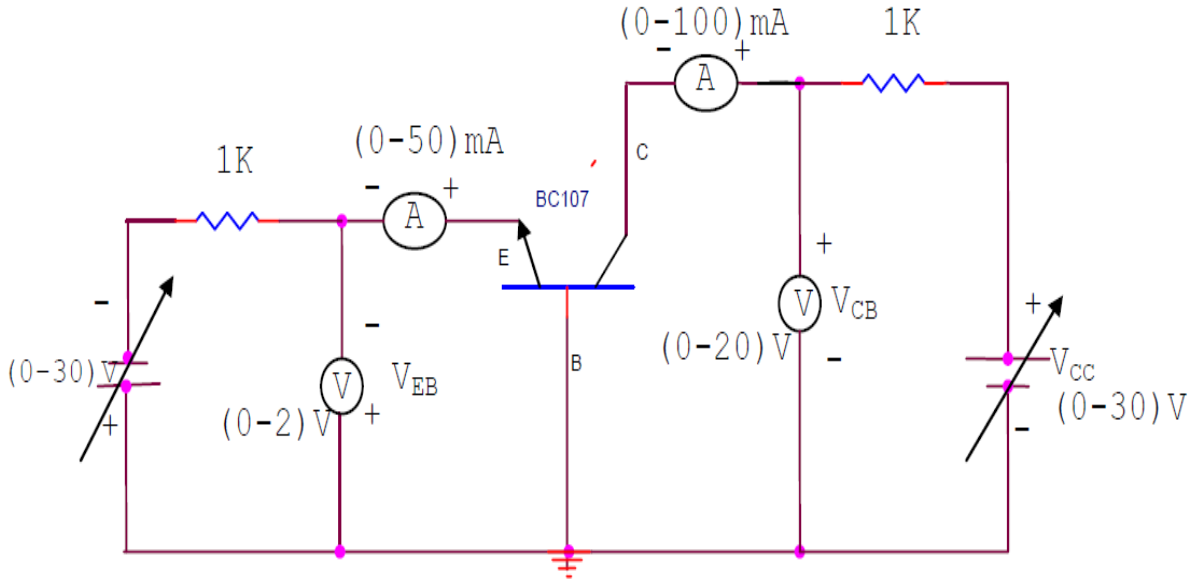
Theory:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. In Common Base configuration the input is applied between emitter and base and the output is taken from collector and base. Here base is common to both input and output and hence the name common base configuration. Input characteristics are obtained between the input current and input voltage taking output voltage as parameter. It is plotted between VEB and IE at constant VCB in CB configuration. Output characteristics are obtained between the output voltage and output current taking input current as parameter. It is plotted between VCB and IC at constant IE in CB configuration.

The current amplification factor of CE configuration is given by

$$\alpha = \Delta I_C / \Delta I_E$$

Output characteristics Circuit Diagram:



Tabular column:

S.No	I_E=		I_E=		I_E=	
	V_{CB}(V)	I_E (mA)	V_{CB}(V)	I_E (mA)	V_{CB}(V)	I_E (mA)

Procedure:

Input characteristics:

1. Connect the circuit as per the circuit diagram shown in Fig (1)
2. Simulate the circuit.
3. Set V_{CB} = 0 by adjusting V_{CC}.
4. Vary the input voltage V_{EE} and note the readings of I_E and V_{BE}.
5. Repeat the above procedure for V_{CB} = 2Vand 5V.
6. Plot the input characteristics V_{BE} Vs I_E for constant Values of V_{CB}= 0V, 2Vand 5V
7. Calculate h- parameters from input characteristics graph

$$\mathbf{V_{EB} = h_{ib}\, I_E + h_{rb}\, V_{CB}}$$
$$\mathbf{I_C = h_{fb}\, I_E + h_{ob}\, V_{CB}}$$

a) Reverse voltage gain $h_{rb} = \left.\frac{\Delta V_{EB}}{\Delta V_{CB}}\right/ \mathbf{I_E}$ Constant

b) Input Impedance $h_{ib} = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right/ \mathbf{V_{CB}}$ Constant

Output characteristics:

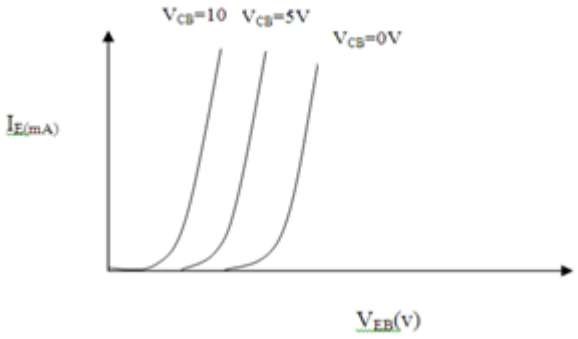
1. Connect the circuit as per the circuit diagram shown in fig (2).
2. Simulate the circuit.
3. Set I_E = 50 mA by adjusting $V_{EE.}$
4. Vary the supply voltage V_{CC} and note the readings of I_C and V_{CB} Take V_{CB}=V_{CC}.
5. Repeat the above procedure for I_E = 100 mA and 200 mA,
6. Plot the output characteristics V_{CB} vs I_C for constant Values of I_E=50 mA, 100 mA and 200 mA.
7. Calculate h- parameters from output characteristics graph

c. Output admittance $h_{ob} = \left.\frac{\Delta I_C}{\Delta V_{CB}}\right| \mathbf{I_E}$ Constant

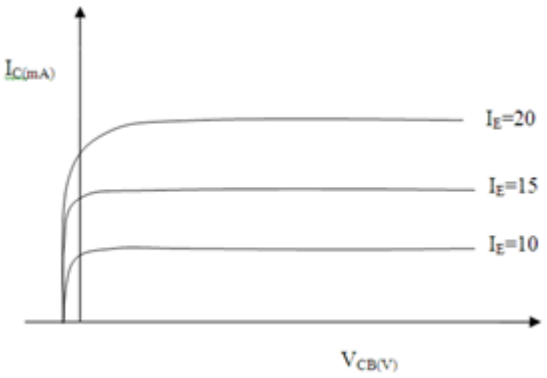
d. Forward current gain $h_{fb} = \left.\frac{\Delta I_C}{\Delta I_E}\right| \mathbf{V_{CB}}$ Constant

Model Graph:

Input characteristics:



Output characteristics:



Calculations:

1. Reverse voltage gain $h_{rb}= \left.\frac{\Delta V_{EB}}{\Delta V_{CB}}\right/ I_E$ Constant =
2. Input Impedance $h_{ib}= \left.\frac{\Delta V_{EB}}{\Delta I_E}\right/ V_{CB}$ Constant =
3. Output admittance $h_{ob} = \left.\frac{\Delta I_C}{\Delta V_{CB}}\right/ I_E$ Constant =
4. Forward current gain h_{fb} $\left.\frac{\Delta I_C}{\Delta I_E}\right/ V_{CB}$ Constant =

Result:

Thus the input and output characteristics of CB configuration are plotted and h parameters are found.

a) Input impedance (h_{ib}) =

b) Forward current gain (h_{fb}) =

c) Output admittance (h_{ob}) =

d) Reverse voltage gain (h_{rb}) =

Conclusion:

1.

2.

Viva questions:

1. How to determine input characteristics of CB Configuration?

2. How to determine output characteristics of CB Configuration?

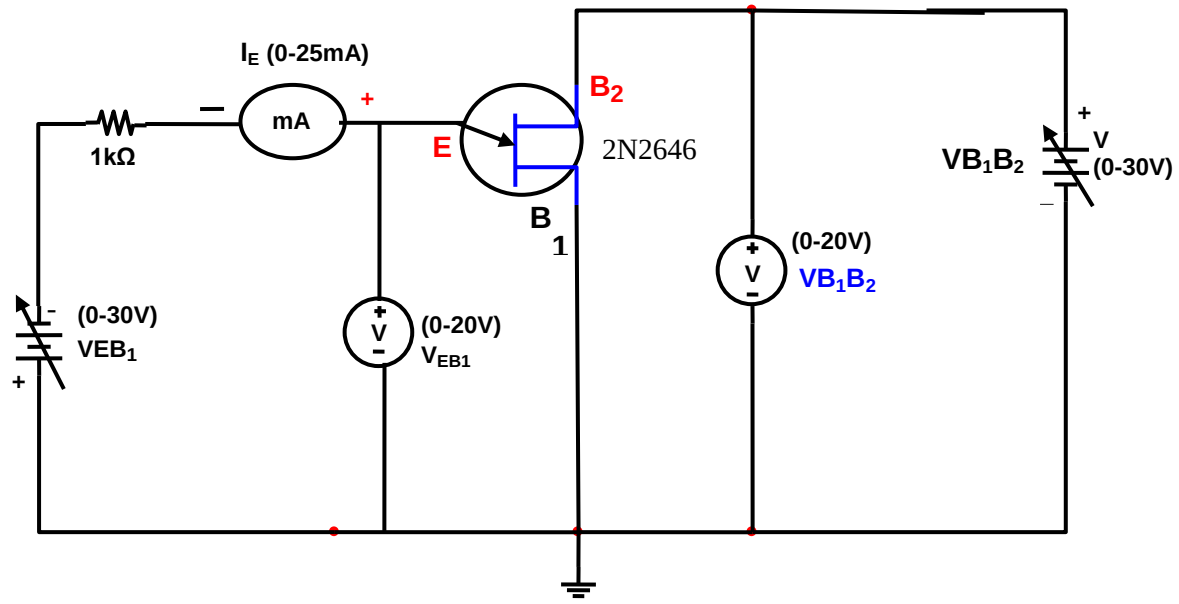
3. List the applications of CB Configuration.

4. List the advantages and disadvantages of CB Configuration.

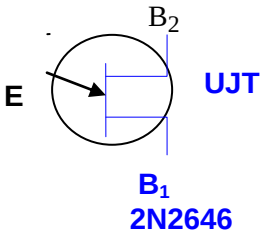
5. Determine the H-Parameters of CB Configuration.

Circuit Diagram:

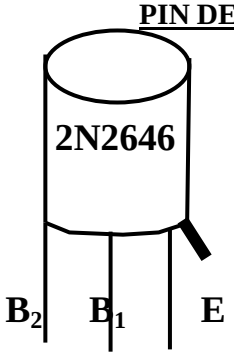
UJT CHARACTERISTICS:-



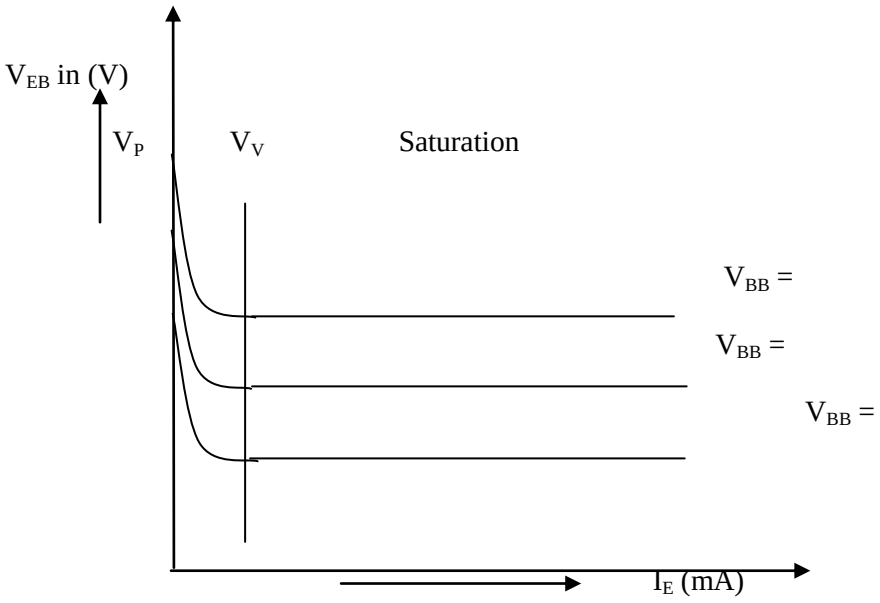
SYMBOL OF BJT:



PIN DETAILS OF UJT :



Model Graph:



Exp: 09 **Date:**

V-I CHARACTERISTICS OF UJT

Aim: To observe the characteristics of UJT and to calculate the Intrinsic Stand-Off Ratio (η).

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	Power Supply(RPS)	0-30V	2
2	Transistor-UJT	2N2646	1
3	DC Ammeter	0-50mA	1
4	DC Voltmeter	0–30V	1
5	Digital Multimeter(DMM)	--	1
6	Resistors	1KΩ	1
7	Bread board	--	1
8	Connecting wires	--	Required

Theory: A Uni-junction Transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT Uni-junction Transistor (UJT) has three terminals, an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance. The original uni-junction transistor, or UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length. The 2N2646 is the most commonly used version of the UJT.

Procedure:

1. Connect the circuit as per the circuit diagram shown in fig (1).
2. Simulate the circuit.
3. Output voltage is fixed at a constant level and by varying input voltage corresponding emitter current values are noted down.
4. This procedure is repeated for different values of output voltages.
5. All the readings are tabulated and Intrinsic Stand-Off ratio is calculated using

$$\eta = (V_p - V_D) / V_{BB}$$

6. A graph is plotted between V_{EE} and I_E for different values of $V_{BE.}$

Observations:

At V_{BB}=5V constant		At V_{BB}=10V constant	
V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)

Calculations:

$V_P = \eta V_{BB} + V_D$

$\eta = (V_P - V_D) / V_{BB}$

$\eta = (\eta_1 + \eta_2 + \eta_3) / 3$

Result: The Emitter characteristics of a UJT are studied and plotted. The peak voltage (Vp) and valley voltage (Vv) for a given UJT are found.

1. The peak voltage (VP) of a UJT is _____.
2. The valley voltage (Vv) of a UJT is _____.

Conclusion:

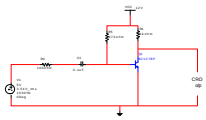
1.

2.

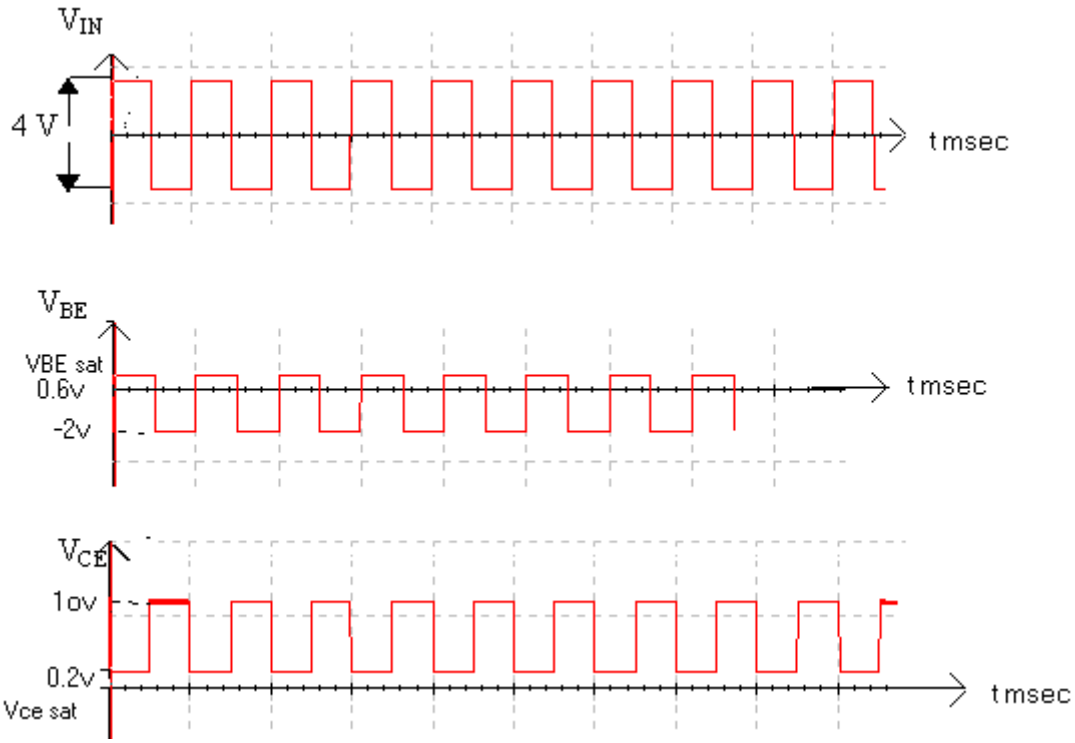
Viva questions:

1. What are the characteristics of UJT?
2. What is difference between UJT and BJT?
3. What is valley point in UJT?
4. What is negative resistance in UJT?
5. What is a relaxation oscillator used for?

Circuit Diagram



Model Waveforms



Exp: 10 **Date:**

TRANSISTOR AS A SWITCH

Aim: To study the operation of Transistor as a switch.

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	Function Generator	0-3Mhz	1
2	CRO	0-30MHz	1
3	RPS	0-30 V	1
4	Transistor	BC 547 or BC 107	1
5	Digital Multimeter (DMM)		1
6	capacitor	100pf	1
7	Resistors	1kΩ,15k,330k	each 1
8	Bread board	--	1
9	Connecting wires	--	Required

Theory:

A transistor can work in 3 regions i.e., Active region Saturation region and Cut-off region. When the transistor is connected in CE configuration the conditions for active region is base-emitter junction forward bias and collector-emitter junction reverse bias. In this region transistor can act as an amplifier.

When emitter to base junction and collector emitter junction both are forward bias the transistor is said to be in 'Saturation Region'.

When emitter to base junction and collector to emitter junction are reverse bias the transistor is said to be in 'Cut-off region'.

To operate transistor as a switch it is made to operate in saturation or cut-off region. If the switch is ON it is saturation region. If the switch is OFF it is in cut-off region.

A pulse train with sufficient amplitude is applied to the transistor base. When pulse is at high the emitter -base and collector-base junctions are forward bias.

Thus transistor enters into saturation or is ON. When pulse is at low both the junctions are reverse biased and the transistor is cut-off or open circuited.

Depending up on the base control voltage the switch may be ON or OFF.

Procedure:

1. Connect the circuit elements as shown in the Circuit Diagram.
2. Applying the square wave voltage of 10V and frequency of 1000 Hz is applied to the circuit as an input.
3. Observe the corresponding output wave form at the collector of the transistor.
4. Note down the corresponding output wave forms in C.R.O and Plot the graph.

Precautions:

1. Check the wires for continuity before use.
2. Keep the power supply at zero volts before staring the experiment.
3. All the connections must be intact

Result:

Conclusion:

1.

2.

Viva questions:

1 .In which region of the characteristics transistor acts as a switch?

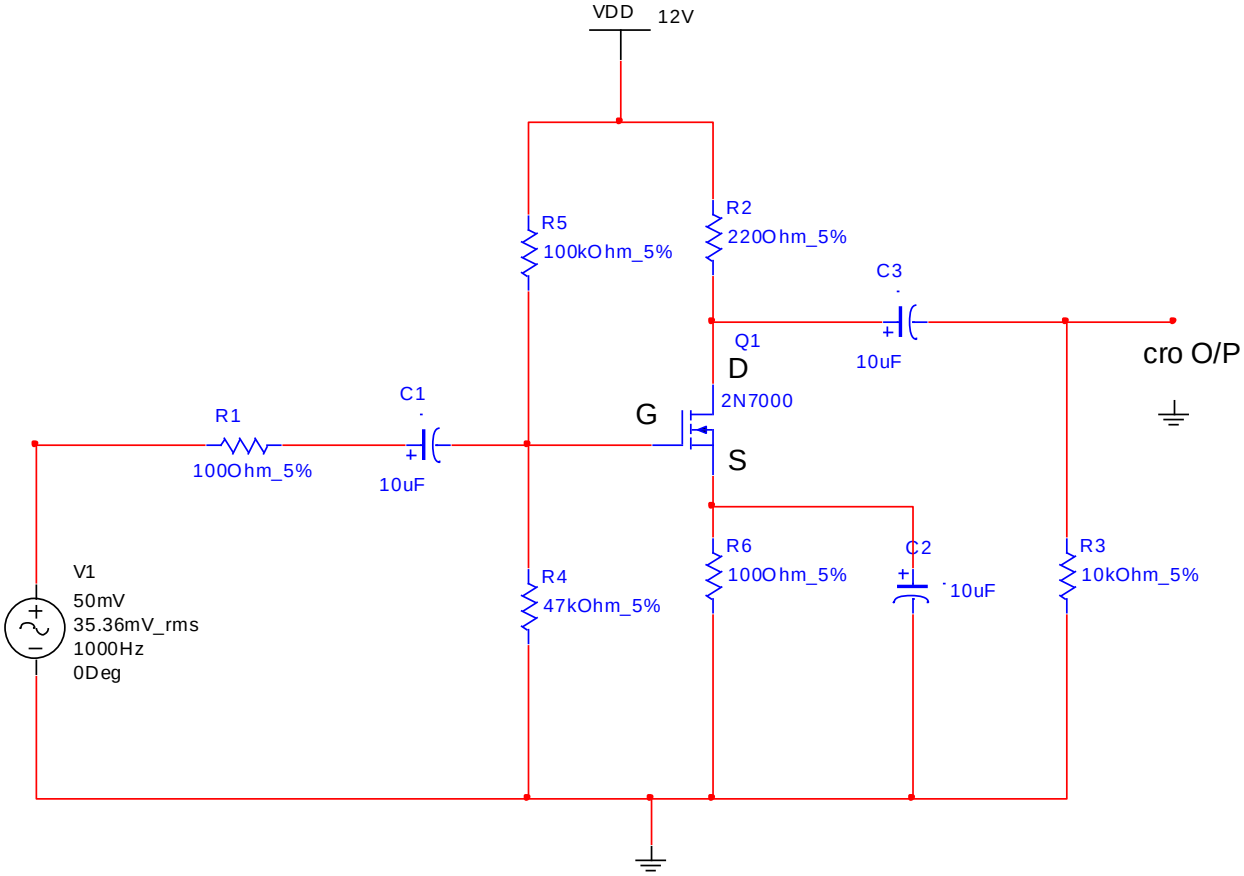
2. What is the typical value of the collector current on ON state?

3. How the junctions of Transistor are biased in ON state and OFF state?

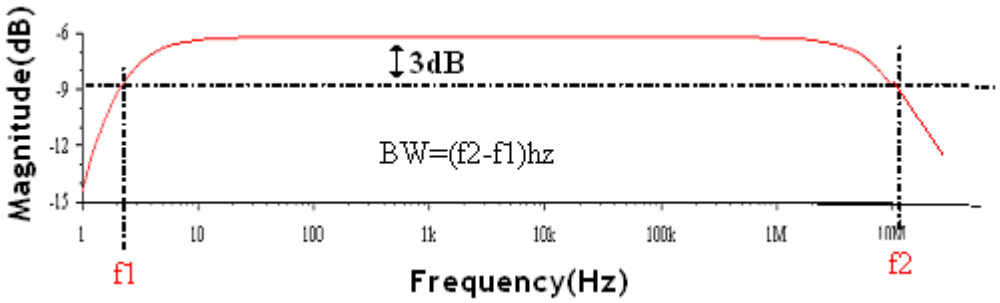
4. How does a transistor act as a switch?

5. Which transistor is best for switching?

Circuit Diagram:



Frequency response:



Exp: 11 **Date:**

MOSFET (common source) AMPLIFIER

Aim: 1).To Obtain Frequency Response of MOSFET (common source) Amplifier.

2).To Find voltage gain, current gain, input impedance, output impedance, and Bandwidth from Frequency Response curve

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	Function Generator	0-3Mhz	1
2	CRO	0-30MHz	1
3	RPS	0-30 V	1
4	MOSFET	2N7000	1
5	capacitor	10µf	3
6	Resistors	100Ω-02,47KΩ ,100k,220Ω,10kΩ	1
7	Bread board	--	1
8	Connecting wires	--	Required

Theory:

Procedure:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar. Using component tool bar place all the components on the circuit window and wire the circuit.

2. Connect the circuit diagram as per the given specifications. Simulate the circuit.

3. Observe the response from oscilloscope and obtain the magnitude plot.

4. Extract the output voltage from the magnitude plot and determine voltage gain in dB.

5. Plot the frequency response and determine bandwidth.

$$BW = f_2 - f_1.$$

Tabular Column: **Input Voltage, V_i =**

S.no	Frequency (Hz)	Output voltage(v_0)(mV)	Voltage gain (A_v)=v_0/v_i	Gain(dB) 20 $\log_{10}\lvert A_v \rvert$

Result:

The Bandwidth of CS Amplifier is

BW = $f_H - f_{L=}$_____Hz.

Conclusion:

1.

2.

Viva questions:

1. What are the advantages of JFET over MOSFET?

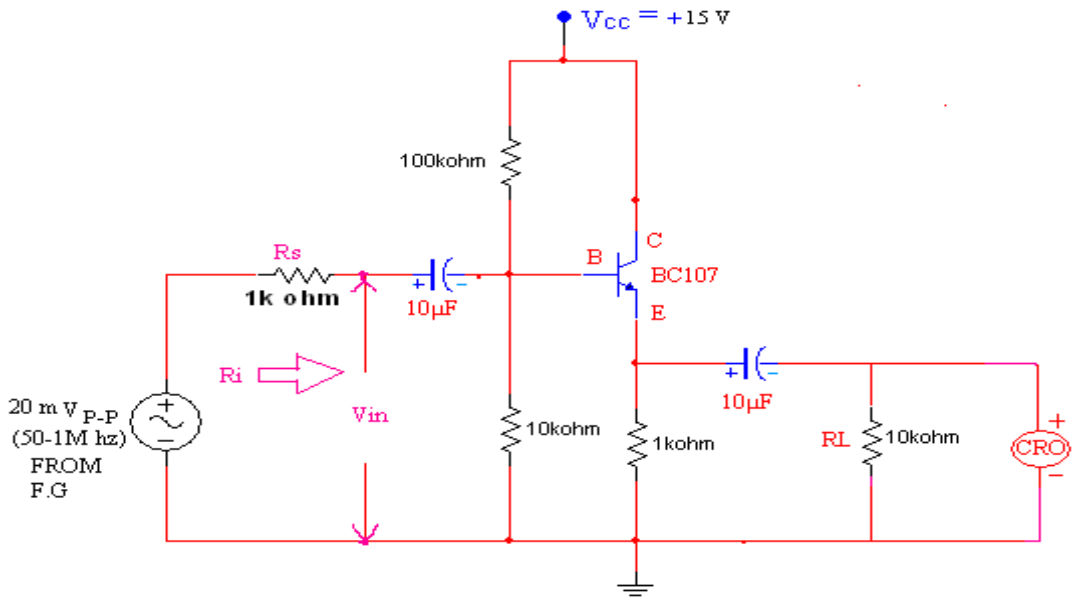
2. What are the types of MOSFET?

3. Compare JFET and MOSFET?

4. Write equation of FET I_D in terms of V_{GS} and V_P?

5. What are the applications of MOSFET?

Circuit Diagram:



Fig(1) Emitter Follower

Tabular Column: **Source Voltage V_S=** **Input Voltage, V_i =**

S.no.	Frequency (Hz)	Output voltage(v_0)(mV)	Voltage gain (A_v)=v_0/v_i	Gain (dB) 20 $\log_{10}\|A_v\|$

Exp: 12 **Date:**

COMMON EMITTER (Emitter Follower) AMPLIFIER

Aim: 1).To Obtain Frequency Response of Common Emitter Amplifier.

2).To Find voltage gain, current gain, input impedance, output impedance, and Bandwidth from Frequency Response curve

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	Function Generator	0-3Mhz	1
2	CRO	0-30MHz	1
3	RPS	0-30 V	1
4	BJT	BC547	1
5	capacitor	10µf	2
6	Resistors	1KΩ ,100kΩ,10kΩ	2
7	Bread board	--	1
8	Connecting wires	--	Required

Theory:

The CE amplifier provides high gain &wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal.

A very small change in base current produces a much larger change in collector current. When +VE half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage more –VE. Thus when input cycle varies through a -VE half-cycle, increases the forward bias of the circuit, which causes the collector current to increases thus the output signal is common emitter amplifier is in out of phase with the input signal.

Procedure:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar. Using component tool bar place all the components on the circuit window and wire the circuit.

2. Connect the circuit diagram as per the given specifications. Simulate the circuit.

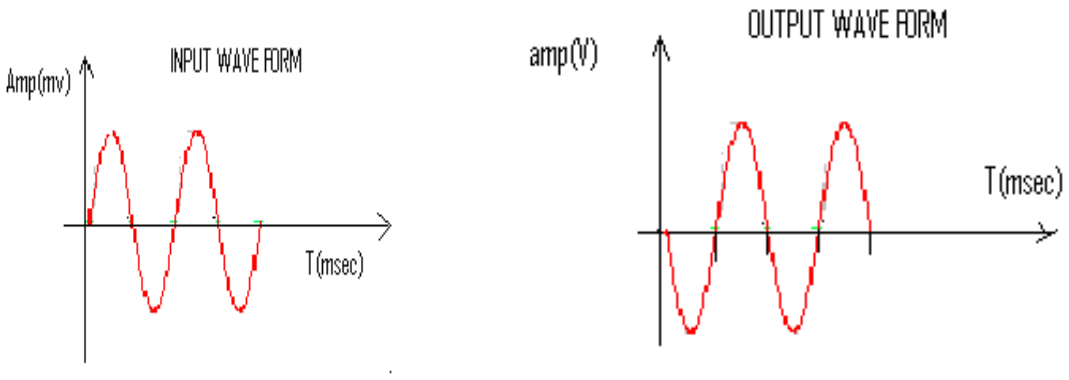
3. Observe the response from oscilloscope and obtain the magnitude plot.

4. Extract the output voltage from the magnitude plot and determine voltage gain in dB.

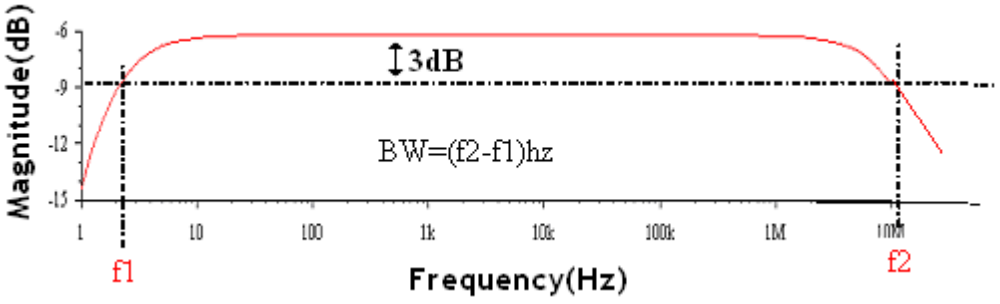
5. Plot the frequency response and determine bandwidth.

$$BW = f_2 - f_1.$$

Model waveforms:



Frequency response:



Calculations:

Voltage gain (A_v) =V_o/V_i =

Input resistance (R_i) =

$$Ri = \frac{Vi\ X\ Rs}{Vs - Vi}$$

Band width (BW) = $f_2 - f_1$ =

Precautions:

4. Avoid loose connections
5. Carefully note the readings from CRO without parallax error.
6. Carefully connect the transistor terminals.

Result:

Frequency Response of Common Emitter Amplifier is obtained.

Voltage gain A_V =

Input resistance R_i =

Bandwidth BW =

Conclusion:

1.

2.

Viva questions:

6. Define Amplifier.

7. Define voltage gain.

8. What are the various types of biasing a Transistor?

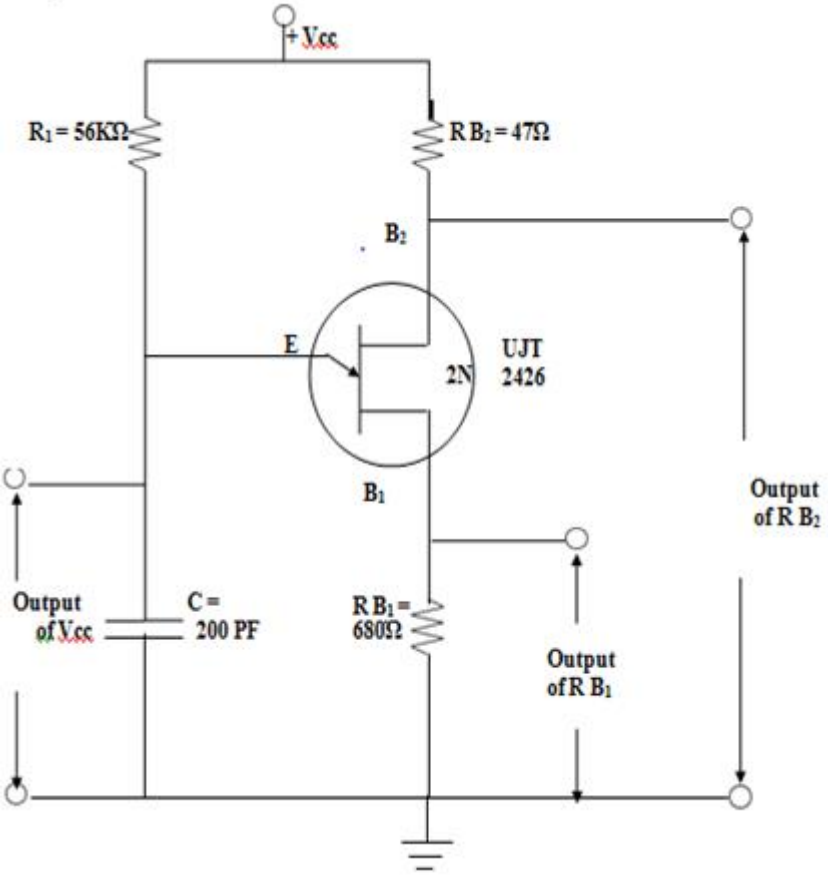
9. What are the Applications of CE amplifiers?

10. Draw the H-parameter equivalent circuit of CE amplifier.

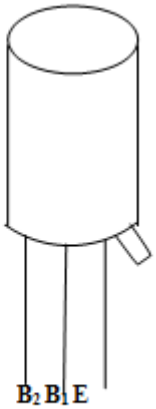
ADDITIONAL EXPERIMENTS

SIMULATION LAB EXPERIMENTS

Circuit Diagram



UJT PIN DETAILS:



Exp: 13 **Date:**

UJT RELAXATION OSCILLATOR

AIM: To construct and verify the UJT Relaxation Oscillator and its output waveform.

Software Required: Multisim software 14.1 version.

Hardware Required: Personal Computer

Theory:

The UJT Sweep circuit is as shown in diagram. We studied that a UJT is off as long as VE, VR1 the peak voltage. Hence initially when UJT is OFF the capacitor "C" charges through resistor from the supply. It is seen that when capacitor voltage rises to a certain value the UJT readily conducted when UJT raises on the capacitor discharges and its voltage falls. When voltage falls to the valley point the UJT becomes off the capacitor charges again to Vp. The cycle of charging and discharging of the capacitor repeat and as a result a sawtooth wave form of voltage across "C" is generated.

Procedure:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar. Using component tool bar place all the components on the circuit window and wire the circuit. Connect the circuit diagram as per the given specifications.

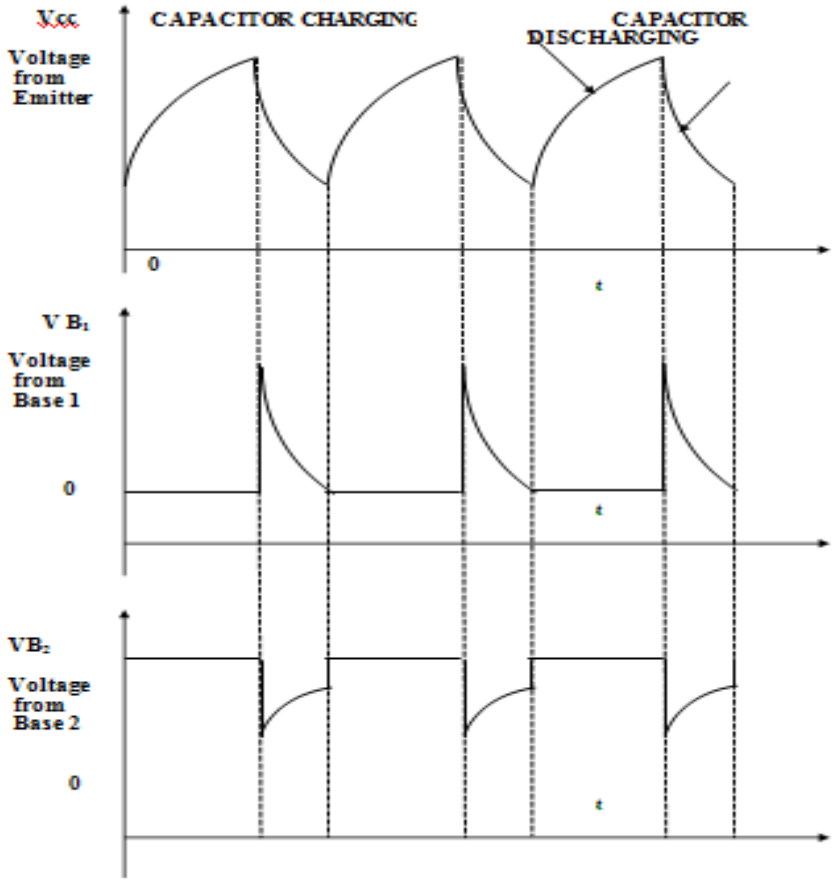
2. Apply the voltage $V_{CC} = 12V$.

3. The output wave forms of emitter, base1 and base2 are noted from the CRO and the graph were plotted.

Result:

The construction and verification of UJT relaxation oscillator and its output waveforms has been done.

MODEL GRAPH:



Observation:

S. No	Waveform	Amplitude	Frequency	
			T_{on}	T_{off}
	$V_{E(V)}$			
	$V_{B1(V)}$			
	$V_{B2(V)}$			

RESULT:

Conclusion:

1.

2.

Viva questions:

1. What is a UJT relaxation oscillator?

2. What is a relaxation oscillator used for?

3. What triggers UJT?

4. What is the main function of Uni-junction transistor UJT?

5. Why UJT is called relaxation oscillator?

Exp: 14 **Date:**

IMPLEMENTATION OF LOGIC GATES USING DIODES AND TRANSISTORS

AIM: To verify the truth table for various logic gates using resistors, diodes and transistors.

Software Required: Multisim software 14.1 version.

Hardware Required: Personal Computer

Theory:

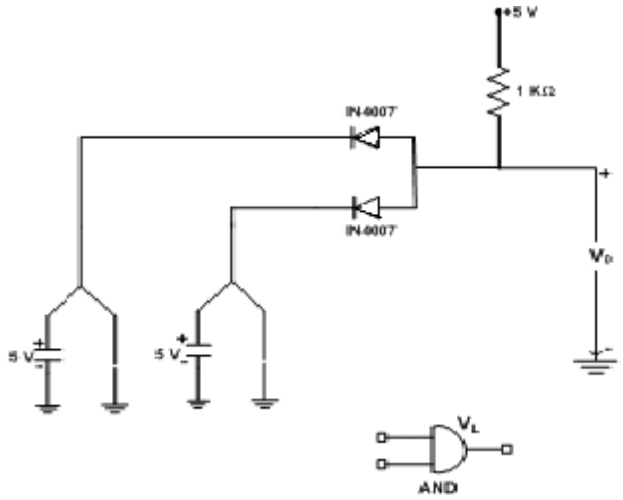
Circuits used to process digital signals are called logic gates. Gate is a digital circuit with one or more inputs but only one output. The basic gates are AND, OR, NOT, NAND, NOR. By connecting these gates in different ways we can build circuits that can perform arithmetic and other functions. The logic gates NAND, NOR are universal gates.

Procedure:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar. Using component tool bar place all the components on the circuit window and wire the circuit. Connect the circuit diagram as per the given specifications.
2. Output is taken across the load resistance
3. Outputs are tabulated and truth table is verified

Result:

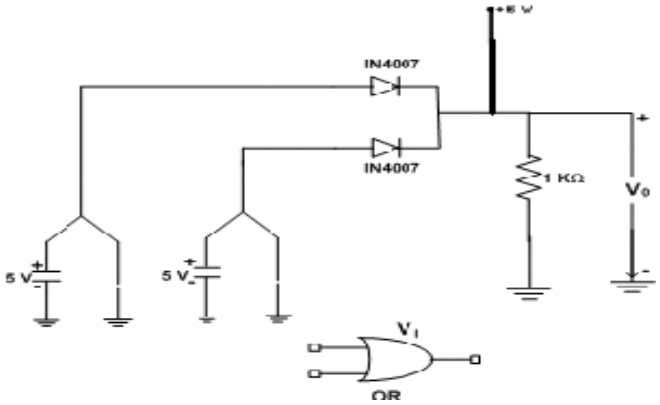
AND GATE



TRUTH TABLE

A	B	0/P
0	0	
0	1	
1	0	
1	1	

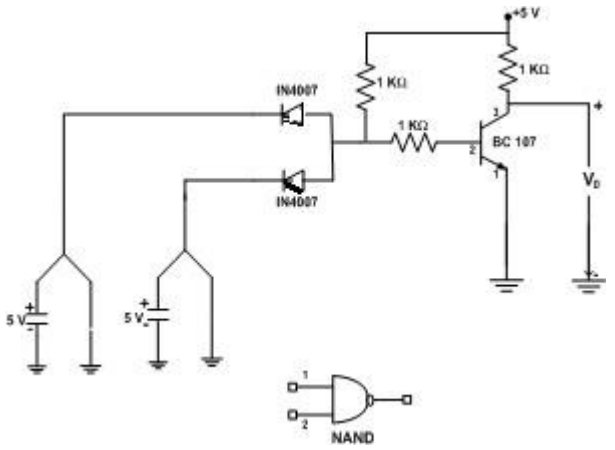
1. OR GATE



TRUTH TABLE

A	B	O/P
0	0	
0	1	
1	0	
1	1	

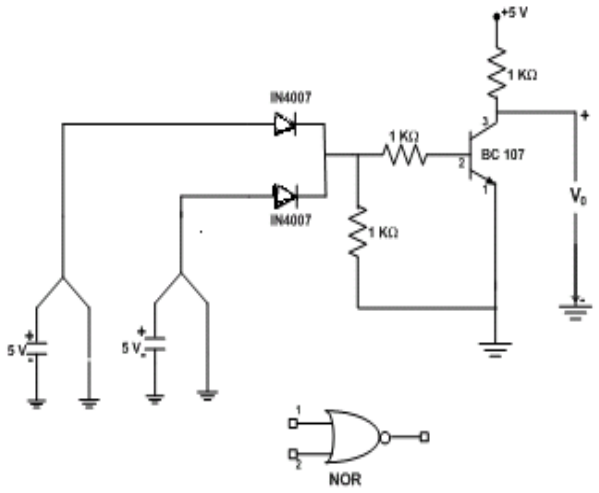
2. NAND GATE



TRUTH TABLE

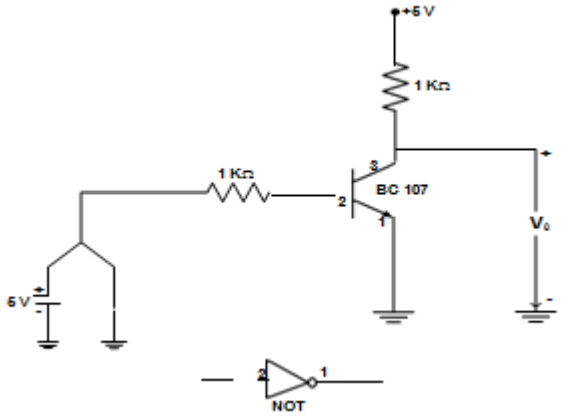
A	B	0/P
0	0	
0	1	
1	0	
1	1	

3. NOR GATE



A	B	O/P
0	0	
0	1	
1	0	
1	1	

4. NOT GATE



TRUTH TABLE

A	0/P
0	
1	

Conclusion:

1.

2.

Viva questions:

1. What are different types of logic gates?

2. What are universal gates? Why called so?

3. Explain the operation of each gate using resistors and transistors?

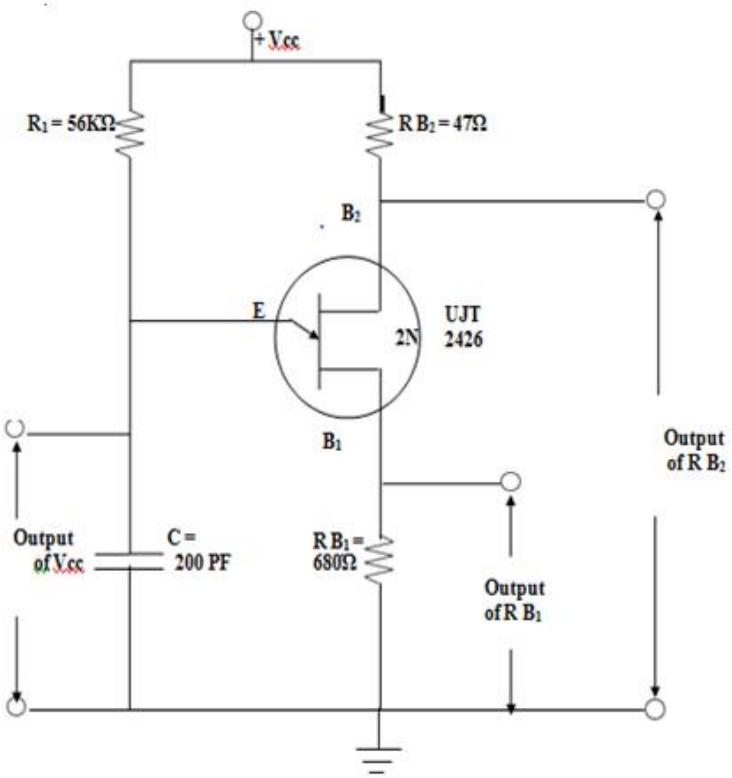
4. Explain logic gates using switches?

5. Draw the truth table for Exclusive OR operation.

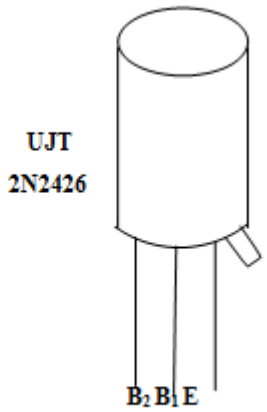
ADDITIONAL EXPERIMENTS

HARDWARE LAB EXPERIMENTS

Circuit Diagram



UJT PIN DETAILS:



Exp: 13 **Date:**

UJT RELAXATION OSCILLATOR

Aim: To construct and verify the UJT Relaxation Oscillator and its output waveform.

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	UJT	2N2426	1
2	CAPACITOR	0.1μF	1
3	Resistors	4.7 KΩ ,680 Ω,470 Ω	4
4	Bread board		
5	Connecting wires		
6	CRO Probes		2
7	RPS	(0-30V)	1
8	CRO		1

Theory:

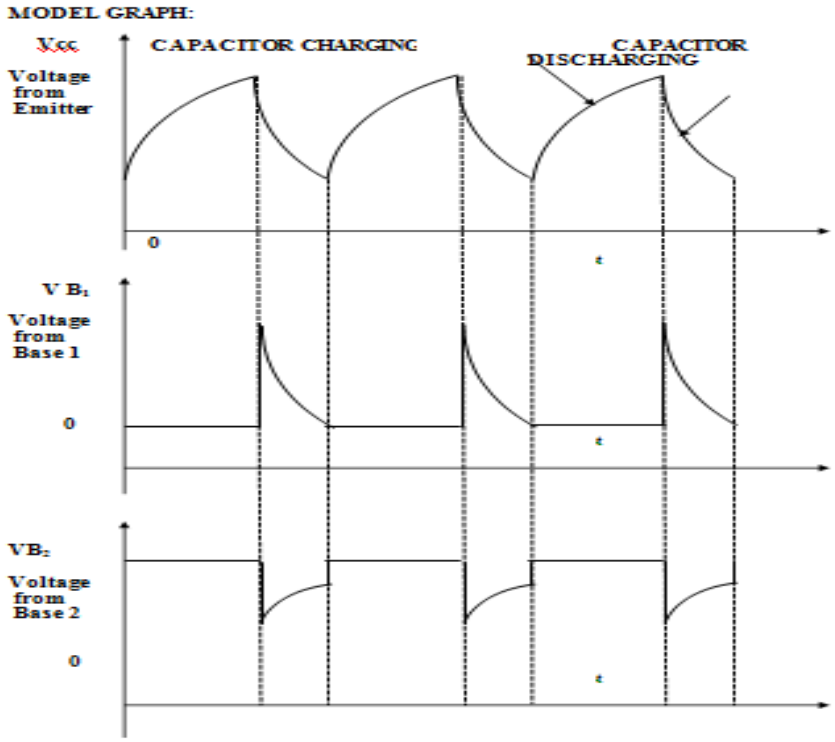
The UJT Sweep circuit is as shown in diagram. We studied that a UJT is off as long as VE, VR1 the peak voltage. Hence initially when UJT is OFF the capacitor "C" charges through resistor from the supply. It is seen that when capacitor voltage rises to a certain value the UJT readily conducted when UJT raises on the capacitor discharges and its voltage falls. When voltage falls to the valley point the UJT becomes off the capacitor charges again to Vp. The cycle of charging and discharging of the capacitor repeat and as a result a sawtooth wave form of voltage across "C" is generated.

Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Apply the voltage V_{CC} = 12V.
3. The output wave forms of emitter, base1 and base2 are noted from the CRO and the graph were plotted.

Result:

Model Graph:



Observation:

S. No	Waveform	Amplitude	Frequency	
			T_{on}	T_{off}
	$V_{E(V)}$			
	$V_{B1(V)}$			
	$V_{B2(V)}$			

Conclusion:

1.

2.

Viva questions:

1. Is UJT is used an oscillator? Why?

2. What are the applications of UJT?

3. Write the formula for the intrinsic standoff ratio?

4. What does it indicates the direction of arrow in the UJT?

5. What is the difference between FET and UJT?

Exp: 14 **Dates:**

IMPLEMENTATION OF LOGIC GATES USING DIODES AND TRANSISTORS

Aim: To Verify the Truth Table for Various Logic Gates using Resistors, Diodes and Transistors.

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	Diodes	1N4007	2
2	Transistor	BC107	1
3	Resistors	1K	3
4	Bread board		1
5	Connecting wires		As per required
6	RPS		1

Theory:

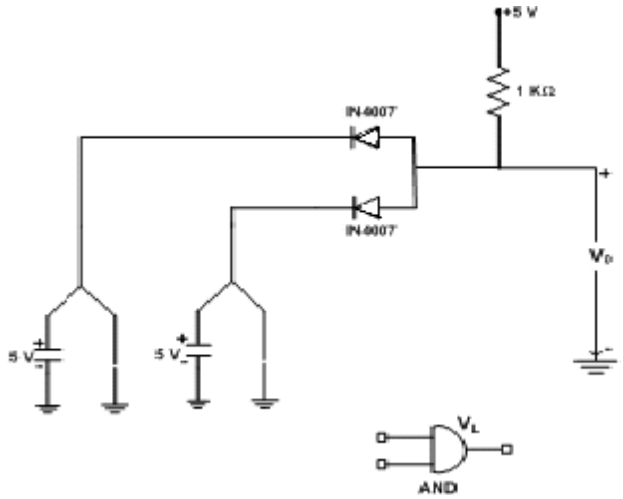
Circuits used to process digital signals are called logic gates. Gate is a digital circuit with one or more inputs but only one output. The basic gates are AND, OR, NOT, NAND, NOR. By connecting these gates in different ways we can build circuits that can perform arithmetic and other functions. The logic gates NAND, NOR are universal gates.

Procedure:

1. Connections are made as per the circuit diagram.
2. Power supply is switched ON and set the desired inputs
3. Output is taken across the load resistance.
4. Outputs are tabulated and truth table is verified.

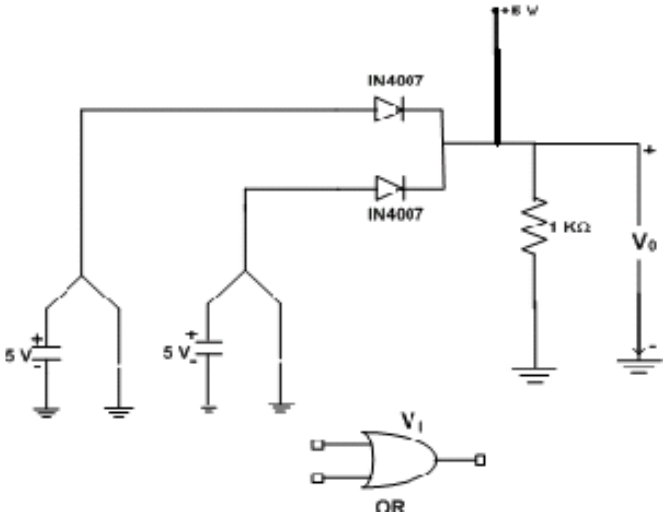
Result: The truth table of various logic gates is verified.

1. AND GATE



TRUTH TABLE

A	B	0/P
0	0	
0	1	
1	0	
1	1	

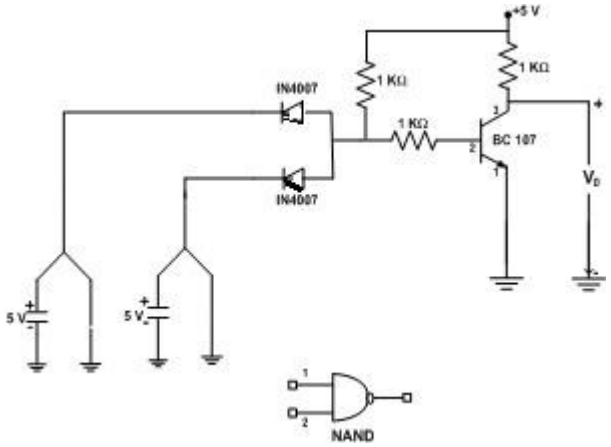


A	B	O/P
0	0	
0	1	
1	0	
1	1	

2. OR GATE

TRUTH TABLE

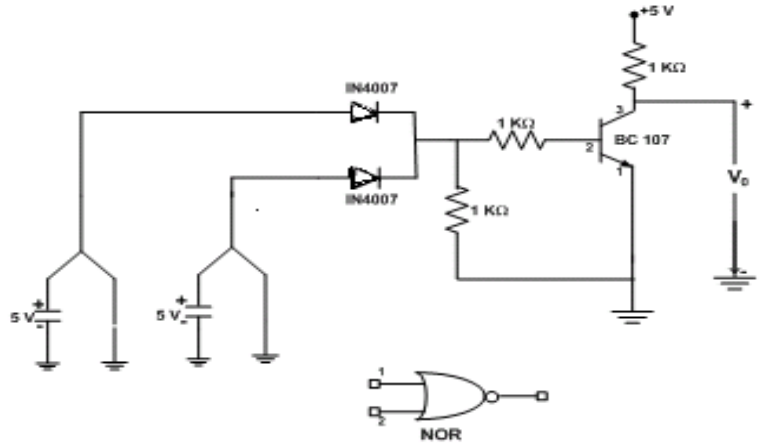
3. NAND GATE



TRUTH TABLE

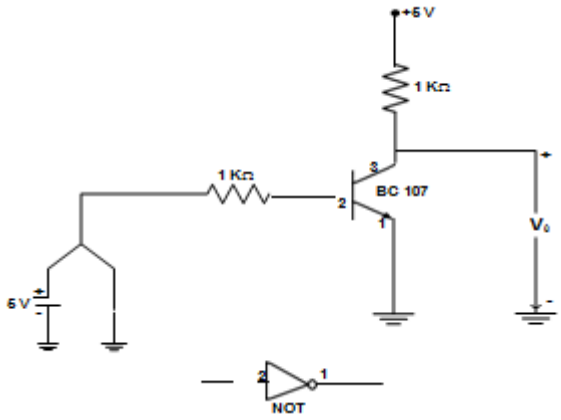
A	B	0/P
0	0	
0	1	
1	0	
1	1	

4. NOR GATE



A	B	O/P
0	0	
0	1	
1	0	
1	1	

5. NOT GATE



TRUTH TABLE

A	0/P
0	
1	

Conclusion:

1.

2.

Viva questions:

1. What are the seven logic gates?

2. What do you mean by logic gates?

3. What are used to complement logic gates?

4. What is the principle of logic gates?

5. Who invented logic gates?