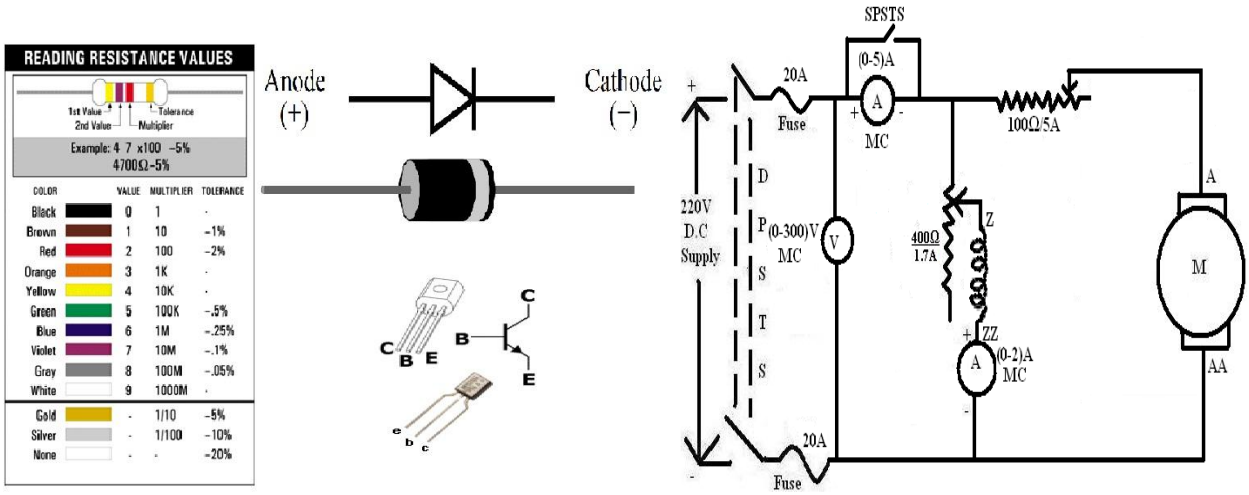
BASIC ELECTRICAL & ELECTRONICS LAB MANUAL



Department of Electronics & Communication Engineering

VEMU INSTITUTE OF TECHNOLOGY::P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

(Approved by AICTE, New Delhi & Affiliated to JNTUA, Anantapuramu)

BASIC ELECTRICAL & ELECTRONICS LAB MANUAL

Name:_____

H.T.No:_____

Year/Semester:_____

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VEMU Institute of Technology
Dept. of Electronics and Communication Engineering
Vision of the institute

To be one of the premier institutes for professional education producing dynamic and vibrant force of technocrats with competent skills, innovative ideas and leadership qualities to serve the society with ethical and benevolent approach.

Mission of the institute

Mission_1: To create a learning environment with state-of-the art infrastructure, well equipped laboratories, research facilities and qualified senior faculty to impart high quality technical education.

Mission_2: To facilitate the learners to inculcate competent research skills and innovative ideas by Industry-Institute Interaction.

Mission_3: To develop hard work, honesty, leadership qualities and sense of direction in learners by providing value based education.

Vision of the department

To develop as a center of excellence in the Electronics and Communication Engineering field and produce graduates with Technical Skills, Competency, Quality, and Professional Ethics to meet the challenges of the Industry and evolving Society.

Mission of the department

Mission_1: To enrich Technical Skills of students through Effective Teaching and Learning practices to exchange ideas and dissemination of knowledge.

Mission_2: To enable students to develop skill sets through adequate facilities, training on core and multidisciplinary technologies and Competency Enhancement Programs.

Mission_3: To provide training, instill creative thinking and research attitude to the students through Industry-Institute Interaction along with Professional Ethics and values.

Programme Educational Objectives (PEOs)

PEO 1: To prepare the graduates to be able to plan, analyze and provide innovative ideas to investigate complex engineering problems of industry in the field of Electronics and Communication Engineering using contemporary design and simulation tools.

PEO-2: To provide students with solid fundamentals in core and multidisciplinary domain for successful implementation of engineering products and also to pursue higher studies.

PEO-3: To inculcate learners with professional and ethical attitude, effective communication skills, teamwork skills, and an ability to relate engineering issues to broader social context at work place

Programme Outcomes(Pos)

PO_1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO_2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO_3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO_4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO_5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO_6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO_7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO_8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO_9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO_10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO_11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO_12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Programme Specific Outcome(PSOs)

PSO_1	**Electronic System Design/Analysis:** Apply the fundamental concepts of Electronics and Communication Engineering to design and analysis of Electronics Systems for applications including Signal Processing, Communication & Networking, Embedded Systems, VLSI design and Control Systems.
PSO_2	**Software Tools:** Proficiency in specialized software tools and computer programming useful for the design and analysis of complex electronic systems to meet challenges in contemporary business environment.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
I B.Tech– I SEM

(20A02101P) BASIC ELECTRICAL & ELECTRONICS ENGINEERING LAB

(Civil, Mechanical & CSE)

Part A: Electrical Engineering Lab

Course Objectives:

- To Verify Kirchoff's laws and Superposition theorem
- To learn performance characteristics of DC Machines.
- To perform various tests on 1- Phase Transformer.
- To Study the I – V Characteristics of Solar PV Cell

List of experiments: -

1. Verification of Kirchhoff laws.
2. Verification of Superposition Theorem.
3. Magnetization characteristics of a DC Shunt Generator.
4. Speed control of DC Shunt Motor.
5. OC & SC test of 1 – Phase Transformer.
6. Load test on 1-Phase Transformer.
7. I – V Characteristics of Solar PV cell
8. Brake test on DC Shunt Motor.

Course Outcomes:

After completing the course, the student will be able to

- Understand Kirchoff's Laws & Superposition theorem.
- Analyze the various characteristics on DC Machines by conducting various tests.
- Analyze I – V Characteristics of PV Cell
- Apply the knowledge to perform various tests on 1-phase transformer

Part B: Electronics Engineering Lab

Course Outcomes:

- o verify the theoretical concepts practically from all the experiments.
- To analyze the characteristics of Diodes, BJT, MOSFET, UJT.
- To design the amplifier circuits from the given specifications.
- Exposed to linear and digital integrated circuits.

List Of Experiments:

1. PN Junction diode characteristics A) Forward bias B) Reverse bias.
2. Zener diode characteristics and Zener as voltage Regulator.
3. Full Wave Rectifier with & without filter.
4. Wave Shaping Circuits. (Clippers & Clampers)
5. Input & Output characteristics of Transistor in CB / CE configuration.
6. Frequency response of CE amplifier.
7. Inverting and Non-inverting amplifiers using Op-AMPs.
8. Verification of Truth Table of AND, OR, NOT, NAND, NOR, Ex-OR, Ex-NOR gates using ICs.
9. Verification of Truth Tables of S-R, J-K& D flip flops using respective ICs.

Tools / Equipment Required: DC Power supplies, Multi meters, DC Ammeters, DC Voltmeters, AC Voltmeters, CROs, all the required active devices.

Course outcomes:

- Learn the characteristics of basic electronic devices like PN junction diode, Zener diode & BJT.
- Construct the given circuit in the lab
- Analyze the application of diode as rectifiers, clippers and clampers and other circuits.
- Design simple electronic circuits and verify its functioning.

Note: Minimum Six Experiments to be performed in each section.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
I B.Tech– I SEM

(20A02101P) BASIC ELECTRICAL & ELECTRONICS ENGINEERING LAB

(Civil, Mechanical & CSE)

Part B: Electronics Engineering Lab

COURSE OUTCOMES (CO_{S})

CO1	Explain the Characteristics of basic electronic devices like PN junction diode, Zener diode and BJT.
CO2	Construct the given circuit in the lab.
CO3	Analyze the application of diode as rectifiers, clippers and clampers and other circuits.
CO4	Design simple electronic circuits and verify its functioning.

List of Experiments:

1. PN Junction diode characteristics A) Forward bias B) Reverse bias.
2. Zener diode characteristics and Zener as voltage Regulator.
3. Full Wave Rectifier with & without filter.
4. Wave Shaping Circuits. (Clippers & Clampers)
5. Input & Output characteristics of Transistor in CB / CE configuration.
6. Frequency response of CE amplifier.
7. Inverting and Non-inverting amplifiers using Op-AMPs.
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Department of Electronics &Communication Engineering

(20A02101) BASIC ELECTRICAL AND ELECTRONICS LABORATORY
I B.Tech– I SEM

LIST OF EXPERIMENTS TO BE CONDUCTED

PART-B:

1. V-I Characteristics of PN Junction Diode.
2. V-I Characteristics of Zener Diode and Zener Diode as Voltage Regulator.
3. Full wave Rectifier with and without Filter.
4. Wave shaping Circuits (Clippers & Clampers)
5. Input and output characteristics of Transistor in CB/CE configuration.
6. Verification of Truth Table of AND, OR, NOT, NAND, NOR, Ex-OR Gates using IC's.

ADDITIONAL EXPERIMENTS (BEYOND CURRICULUM)

7. Transistor as a switch.
8. Verification of Truth Table of half adder by using IC's.

DOS & DONT'S IN LABORATORY

1. While entering the Laboratory, the students should follow the dress code Wear
2. shoes, White Apron & Female students should tie their hair back).
3. The students should bring their observation note book, practical manual, record note book, calculator, necessary stationary items and graph sheets if any for the lab classes without which the students will not be allowed for doing the practical.
4. All the equipments and components should be handled with utmost care. Any breakage/damage will be charged.
5. If any damage/breakage is noticed, it should be reported to the instructor immediately.
6. If a student notices any short circuits, improper wiring and unusual smells immediately the same thing is to be brought to the notice of technician/lab in charge.
7. At the end of practical class the apparatus should be returned to the lab technician and take back the indent slip.
8. Each experiment after completion should be written in the observation note book and should be corrected by the lab in charge on the same day of the practical class.
9. Each experiment should be written in the record note book only after getting signature from the lab in charge in the observation note book.
10. Record should be submitted in the successive lab session after completion of the experiment.
11. 100% attendance should be maintained for the practical classes.

CONTENTS

SCHEME OF EVALUVATION

S NO	NAME OF EXPERIMENT	DATE	MARKS AWARDED				TOTAL (30M)
			Record (10M)	Observation (10M)	Viva voce (10M)	Attendance (10M)	
1	V-I Characteristics of PN Junction Diode.						
2	V-I Characteristics of Zener Diode and Zener Diode as Voltage Regulator.						
3	Full wave Rectifier with and without Filter.						
4	Wave shaping Circuits (Clippers & Clampers)						
5	Input and output characteristics of Transistor in CB/CE configuration.						
6	Verification of Truth Table of AND, OR, NOT, NAND, NOR, Ex-OR Gates using IC's.						
Additional Experiments (Beyond Curriculum)							
7.	Transistor as a switch.						
8.	Verification of Truth Table of half adder by using IC's.						

Signature of Lab In-charge

PART - B

ELECTRONICS ENGINEERING LAB

Circuit diagram: (Forward bias):

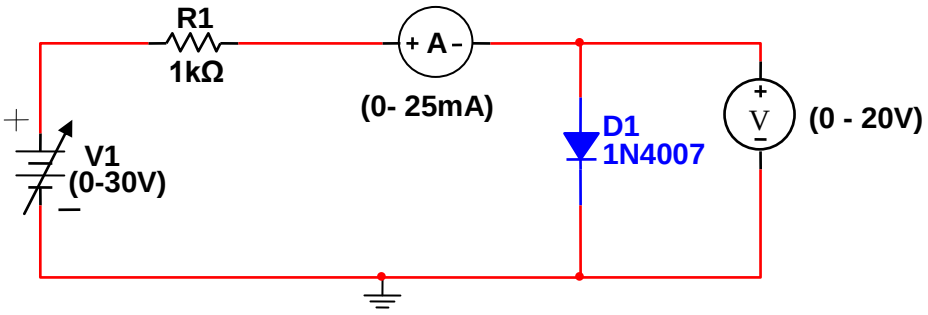


Fig.(1) Forward biased PN Junction Diode

Reverse Bias:

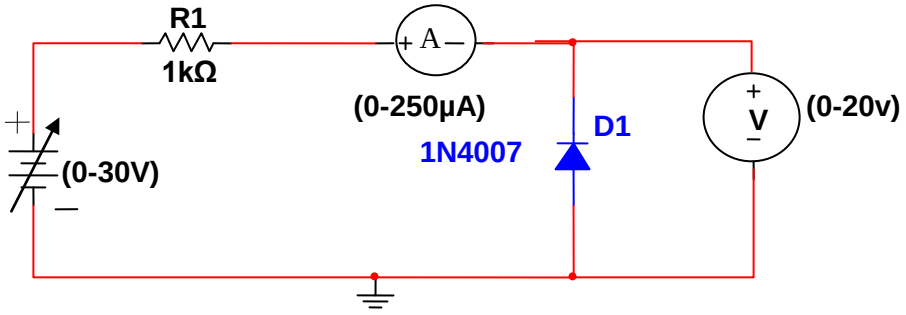
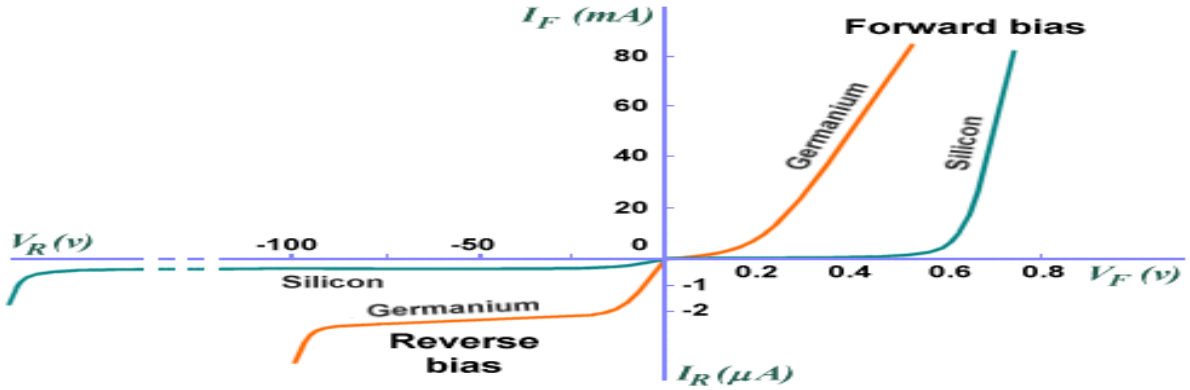


Fig. (2) Reverse biased PN Junction Diode

Model Graph:



Volt and Ampere Characteristics of PN Junction Diode

Exp: 1 **Date:**

PN- JUNCTION DIODE CHARACTERISTICS

Aim: 1.To plot the Volt - Ampere characteristics of given P–N junction Diode
2. To find the static, dynamic and reverse resistances.

Apparatus:

S. No.	Apparatus	Range/Rating	Quantity
1	Diode-	1N4007	1
2	Resistors	1KΩ	1
3	DC Ammeter	0-50mA	1
		0-100µA	1
4	DC Voltmeter	0-1V	1
		0-10V	1
5	RPS	0-30V	1
6	Bread board	--	1
7	Connecting wires	--	Required

Procedure: (Forward Bias)

1. Connect the circuit as per the circuit diagram shown in Fig.(1).For Both Silicon and Germanium Diodes.
2. Vary the power supply in such a way that the readings are taken in steps of 0.1V, to the maximum reading of power supply of 10V
3. Note down the corresponding Ammeter and Voltmeter readings.
4. Plot the graph between Forward voltage and current (V_F and I_F.)
5. Find the Static Forward Resistance $R_F = V/I\ \Omega$.
6. Find the Dynamic Forward Resistance $r_F = \frac{\Delta V}{\Delta I}\Omega$

Reverse Bias:

1. Connect the circuit as per the circuit diagram shown in Fig. (2).
2. Vary the power supply in such a way that the readings are taken in steps of 2V, to the maximum reading of power supply of 30V.
3. Note the corresponding Ammeter and Power Supply readings.
4. Plot the graph between V_R and I_R.
5. Find the Static Reverse Resistance.
6. Find the Dynamic Reverse Resistance.

Tabular Column:

Forward Bias:

S. No.	Silicon Diode	
	V_F(V)	I_F (mA)

Reverse Bias:

S. No.	Silicon Diode	
	V_R(V)	I_R(μA)

Result:

Successfully verified operation of PN Junction diode under forward and reverse biased conditions and plotted Volt-Ampere Characteristics.

Determined the static and dynamic diode resistances from the plot.

1. Static Forward Resistance R_F =
2. Static Reverse Resistance R_r =
3. Dynamic Forward Resistance =
4. Dynamic Reverse Resistance =

Precautions:

1. Don’t give voltage to the circuit beyond prescribed range.
2. Don’t short circuit the output terminal of power supply.
3. Carefully connect meter terminals (+ and –).

Conclusion:

1.

2.

Viva questions:

1. What is Zener break down and avalanche break down?

2. Draw the symbols of special purpose diodes?

3. What is Barrier Potential?

4. How P-N Junction Formed?

5. Why reverse saturation current is high in germanium than silicon?

Circuit Diagram:

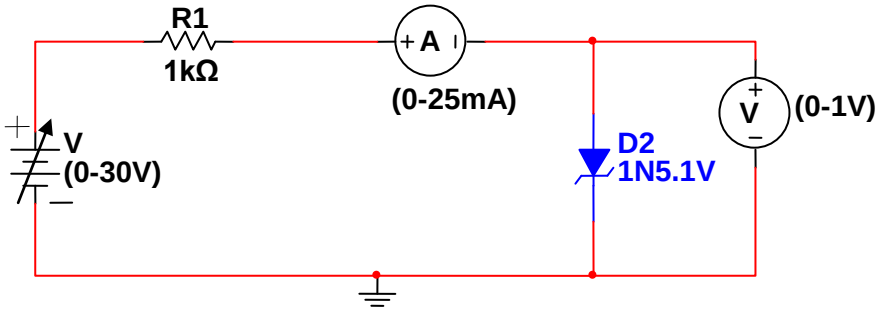


Fig 1. Forward bias characteristics

Reverse bias:

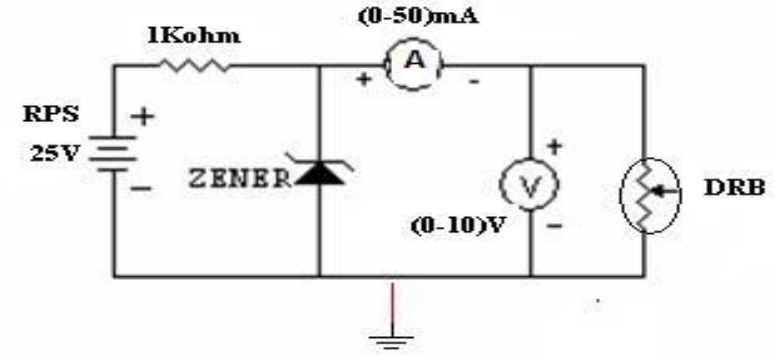
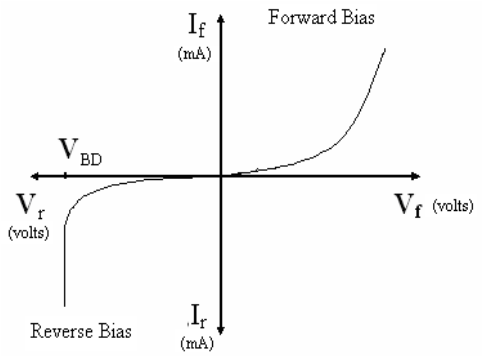


Fig. 2.Zener Diode based Voltage Regulator

Model Graph:



V-I Characteristics

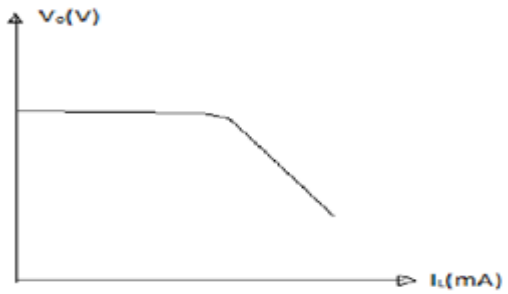


Fig. Regulation Characteristics

Exp: 2 **Date:**

ZENER DIODE CHARACTERISTICS and ZENER AS VOLTAGE REGULATOR

Aim:

1.To Plot the Volt – Ampere characteristics of a Zener diode.

2.To Find and verify the Zener diode as voltage regulator.

Apparatus :

S.NO	APPARATUS	RANGE	QUANTITY
1	Zener Diode `	5.1V	1
2	Resistors	1KΩ	1
3	DC Ammeter	0-50mA	1
4	DC Voltmeter	0-1V	1
		0-10V	1
5	RPS	0-30V	1
6	Bread board	--	1
7	Connecting wires	--	Required

Theory:

A Zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage.

High current through the diode can permanently damage the device. To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals whatever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

Procedure:

(a) Forward Bias:

1. Connect the circuit as per the circuit diagram shown in Fig(1).
2. Vary the power supply voltage in such a way that the readings are taken in steps of 0.1 V, to the maximum reading of power supply of 20 V.
3. Note down the corresponding Ammeter and Voltmeter readings.
4. Plot the graph between V_F and I_F.

$$r_f = \frac{\Delta V}{\Delta I}\Omega$$

5. Find the dynamic forward resistance using

Load Regulation Characteristics:

1. Connect the circuit as per the circuit diagram in figure 1.
2. Fix the DC supply at 20V.
3. By varying the load resistances tabulate the load voltage $V_L$and load current I_L.
4. Plot the graph between load voltages V_L and load current I_L.

Result:

1. Volt – Ampere Characteristics of Zener Diode are plotted.
2. Zener Break Down Voltage =
3. Dynamic Forward Resistance =
4. Dynamic Reverse Resistance =

Tabular column:

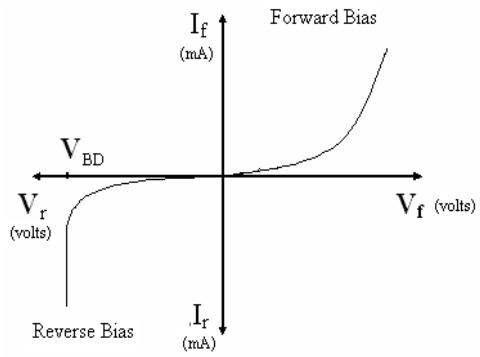
Forward Bias:

S.NO	V_F(V)	I_F(mA)

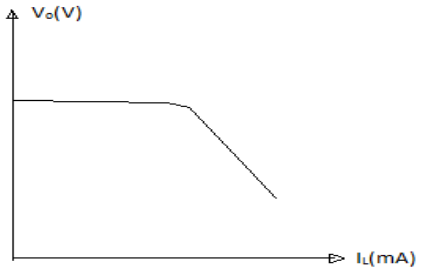
Load Regulation Characteristics:

S. No.	Voltage across Load V_L(V)	Current through the load resistance I_L(mA)

Model Graph:



V-I Characteristics



Regulation Characteristics

Precautions:

1. Carefully connect the meter terminals (+ and –).
2. Carefully connect the Zener diode terminals (Anode & Cathode)

Conclusions:

1.

2.

Viva Questions:

1. Define what is zener voltage?
2. What is break down? What are its types?
3. Why is zener diode used as a voltage regulator?
4. What is avalanche break down?.
5. .How does the avalanche breakdown voltage vary with temperature.

CIRCUIT DIAGRAM:-

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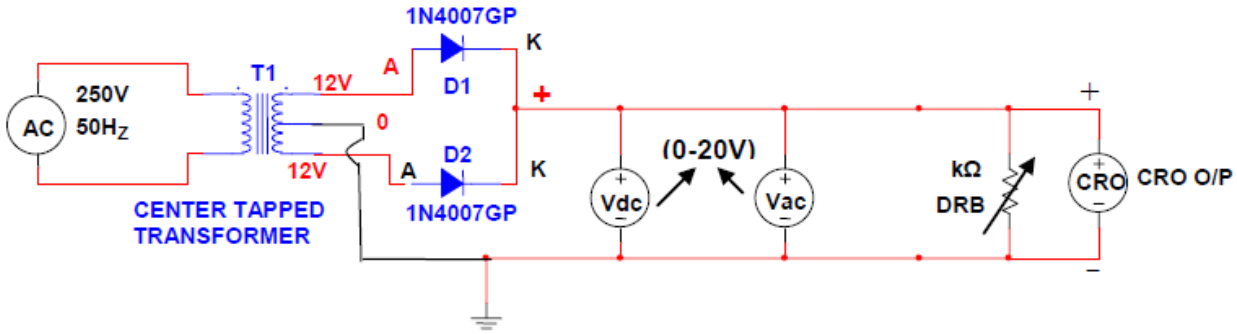

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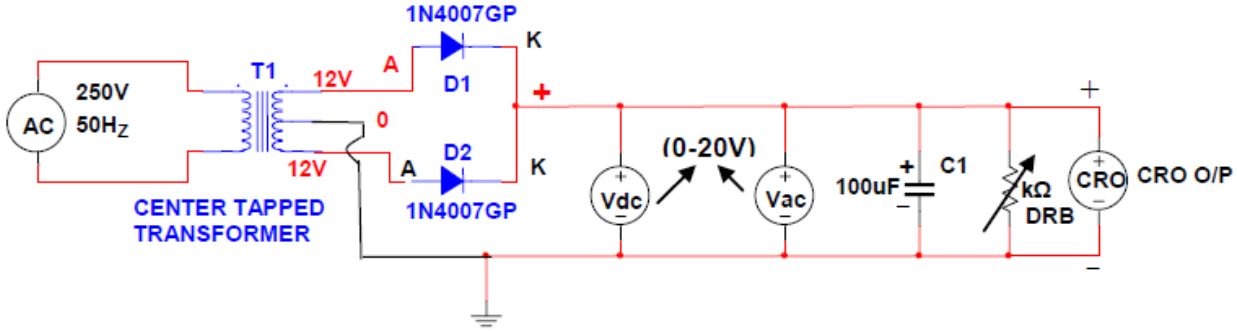
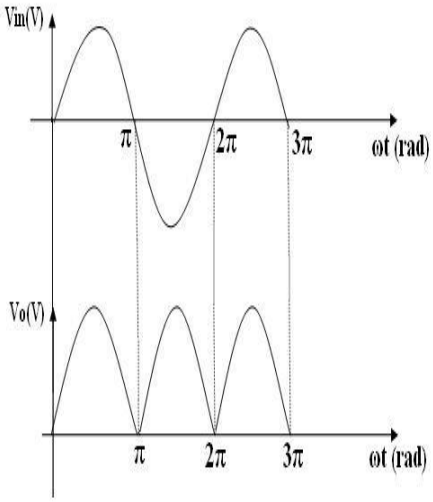


Model Waveforms:

WITHOUT FILTER:

input

Output



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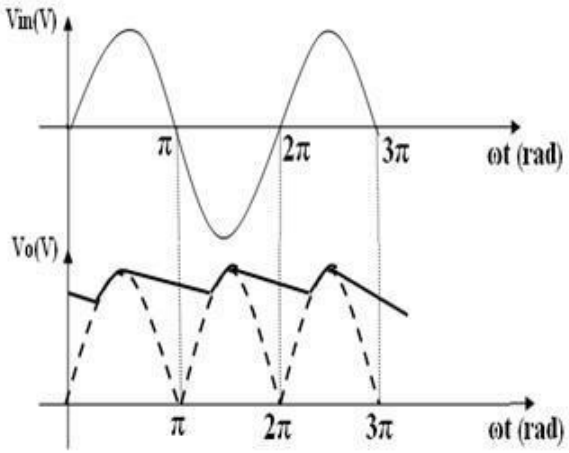


Exp: 3 **Date:**

FULL WAVE RECTIFIER WITHOUT FILTER

Aim: To Find the Ripple factor and Percentage of Regulation of a Full Wave Rectifier with and without Filter.

Apparatus:

S. No.	APPARATUS	RANGE/RATING	QUANTITY
1	Step down transformer	(12-0-12) V	1
2	Diode	1N4007	2
3	Capacitor	47µ/63V	1
4	Decade Resistance Box (DRB)		1
5	Digital Multimeter (DMM)	--	1
6	Bread board	--	1
7	Connecting wires		Required

Procedure:

1. Connect the circuit as per the circuit diagram shown in Fig.
2. Note down the No Load DC Voltage V_{dc0} when $I_{dc} = 0$
3. Vary the load resistance R_L (DRB) and note down I_{dc} and V_{dc}, V_{ac} using Multi meter.
4. Calculate the ripple factor $r = \frac{RMS\ values\ of\ AC\ component}{Average\ value} = \frac{Vac}{Vdc}$
5. Calculate the Percentage of Regulation = $[(V_{dc0} - V_{dc})/V_{dc}]$ x 100

   (or) $(V_{NL} - V_{FL})/V_{FL}$ X100
6. Draw the following graphs:
   - Percentage of Regulation versus I_{dc} taking I_{dc} on x – axis.
   - I_{dc} versus Ripple factor

Precautions:

1. Don't short circuit the output terminal.
2. Carefully connect meter & electrolytic capacitors terminals (+ and –)
3. Carefully connect diode terminals (anodes and cathodes).

Result:

Successfully verified the operation of Full Wave Rectifier with and without filter circuit and calculated the Ripple factor and Percentage of Regulation.

Ripple Factor =

Percentage of Regulation =

Tabular Column:

Without Filter: **No load D.C Voltage, V_{dc0} =**

S. No.	R_L (Ω)	V_{dc} (V)	V_{ac} (V)	$r = V_{ac}/V_{dc}$	% Regulation $[(V_{dco} - V_{dc})/V_{dc}] \times 100$

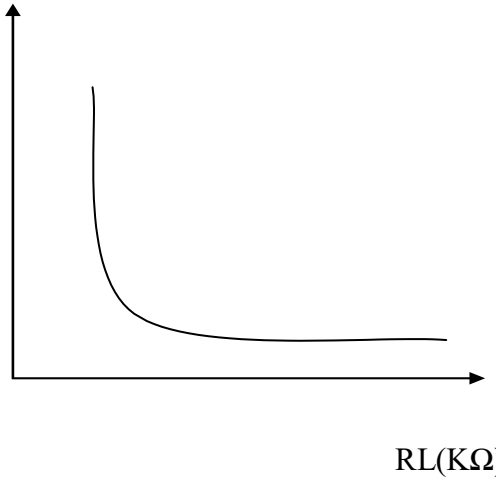
With filter:

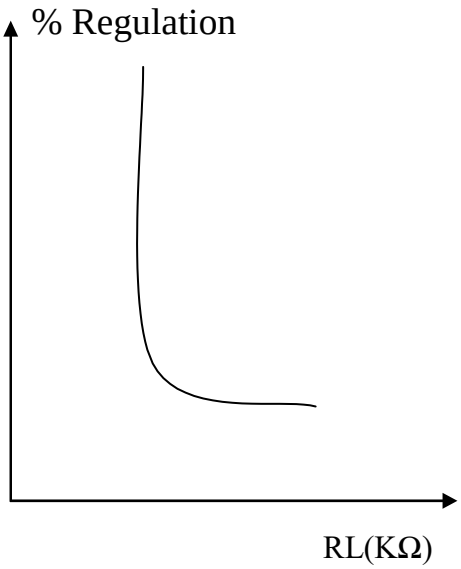
No load D.C Voltage, V_{dc0} =

S. No.	R_L (Ω)	V_{dc} (V)	V_{ac} (V)	$r = V_{ac}/V_{dc}$	% Regulation $[(V_{dco} - V_{dc})/V_{dc}] \times 100$

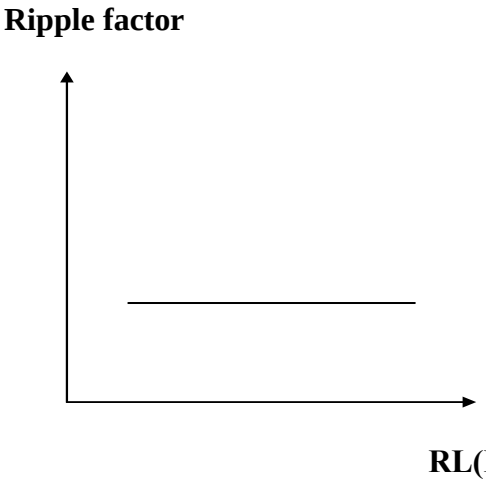
Model Graphs:

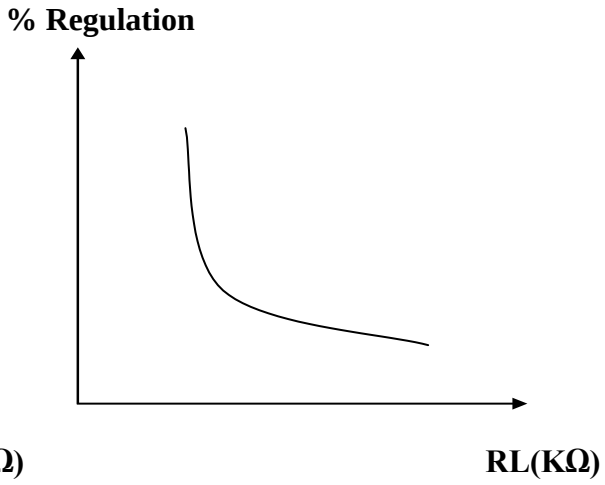
WITHOUT FILTER:





WITH FILTER:





Calculations :

Calculate the ripple factor (r) = $\frac{R.M.S\ VALUES\ OF\ A.C\ COMPONENT}{AVERAGE\ VALUE} = \frac{Vac}{Vdc}$

Calculate the Percentage of Regulation = $[(V_{dc0} - V_{dc})/V_{dc}]$ x 100
(or) $(V_{NL} - V_{FL})/V_{FL}$ X100

Conclusions:

1.

2.

Viva Questions:

1. What is Rectification?

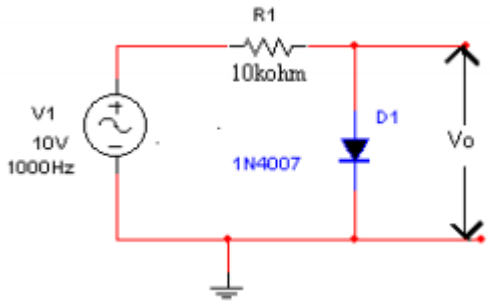
2. What is difference between HWR and FWR.

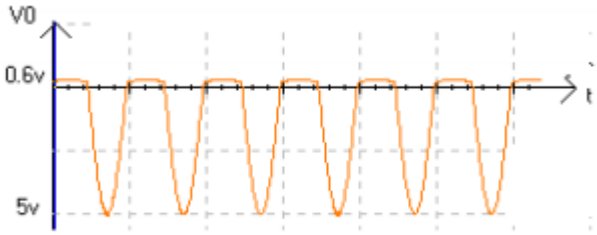
3. Define Step-up Transformer.

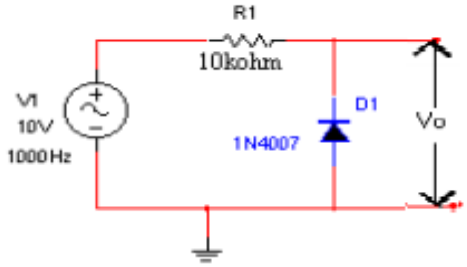
4. What are the types of Rectifier.

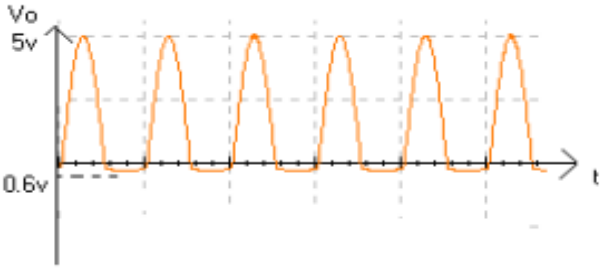
5. What is ripple.

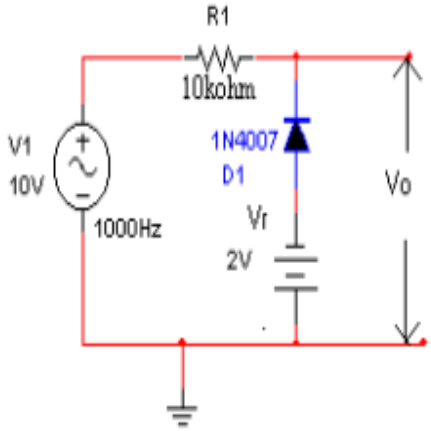
Clipper Circuits with their corresponding output waveforms:

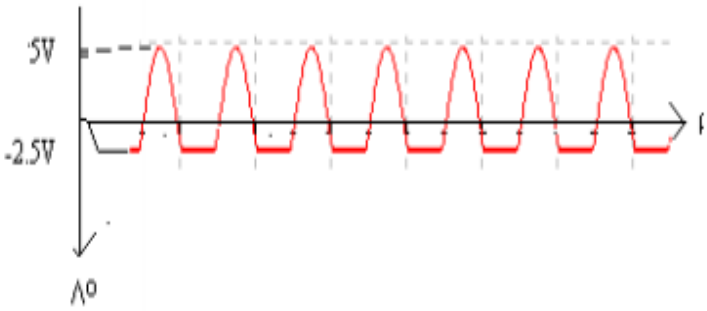


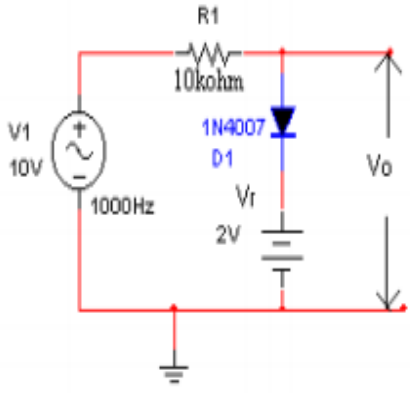


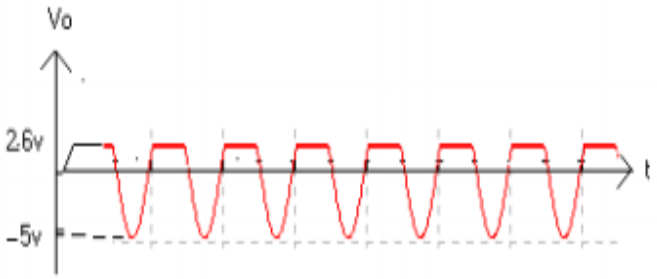












Exp: 4(a) **Date:**

DIODE APPLICATIONS-CLIPPERS & CLAMPERS

CLIPPERS

Aim: a) To study the clipping circuits using diodes.

b) To observe the transfer characteristics of all the clipping circuits in CRO.

Apparatus :

S. No.	APPARATUS	RANGE/RATING	QUANTITY
1	Regulated Power Supply	0 – 30 V	1
2	Diode	1N4007	2
3	Resistors	10 KΩ	1
4	Function Generator	0 – 30 V	1
5	CRO	0 - 20 MHz	1
7	Bread board	--	1
8	Connecting Wires	-	As required

Procedure:

1. Connect the circuit as per the circuit diagram in Figure.
2. In each case apply 10 VP-P, 1 KHz Sine wave I/P using a signal generator.
3. O/P is taken across the load R_L.
4. Observe the O/P waveform on the CRO and compare with I/P waveform.
5. Sketch the I/P as well as O/P waveforms and mark the numerical values.
6. Obtain the transfer characteristics of Fig.1, by keeping CRO in X-Y mode.
7. Repeat the above steps for all the clipping circuits.

S. No	Waveform	Amplitude	Frequency
1.			

Result:

The practical values

V= $\gamma + V_R$

V= $\gamma - V_R$

Clipping circuits for different reference voltages are studied.

Conclusion:

1.

2.

Viva questions:

1. Define clipping? Describe (i)Positive clipper (ii)Biased Clipper (iii)Combination clipper.

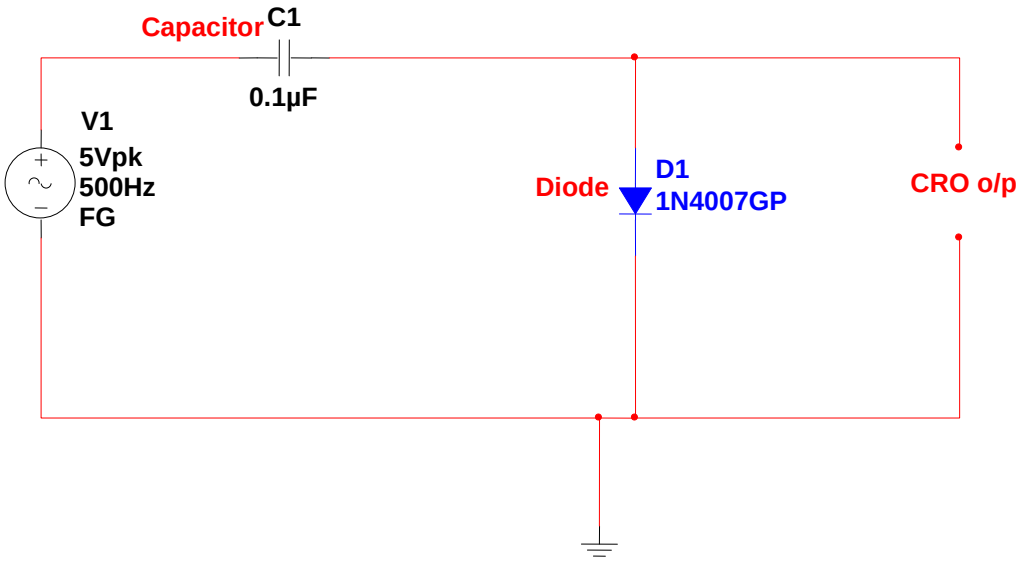
2. Define clamping?

3. Define peak inverse voltage of diode?

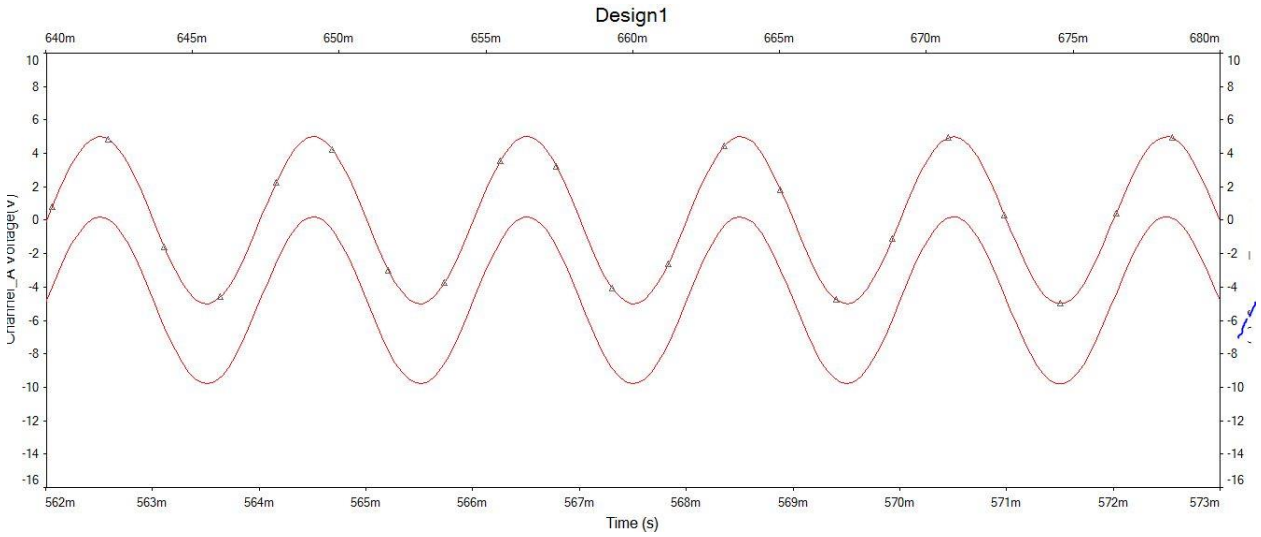
4. What are the other names for the clamper?

5. List different types of Clippers.

Circuit Diagram: Clamper Circuit :



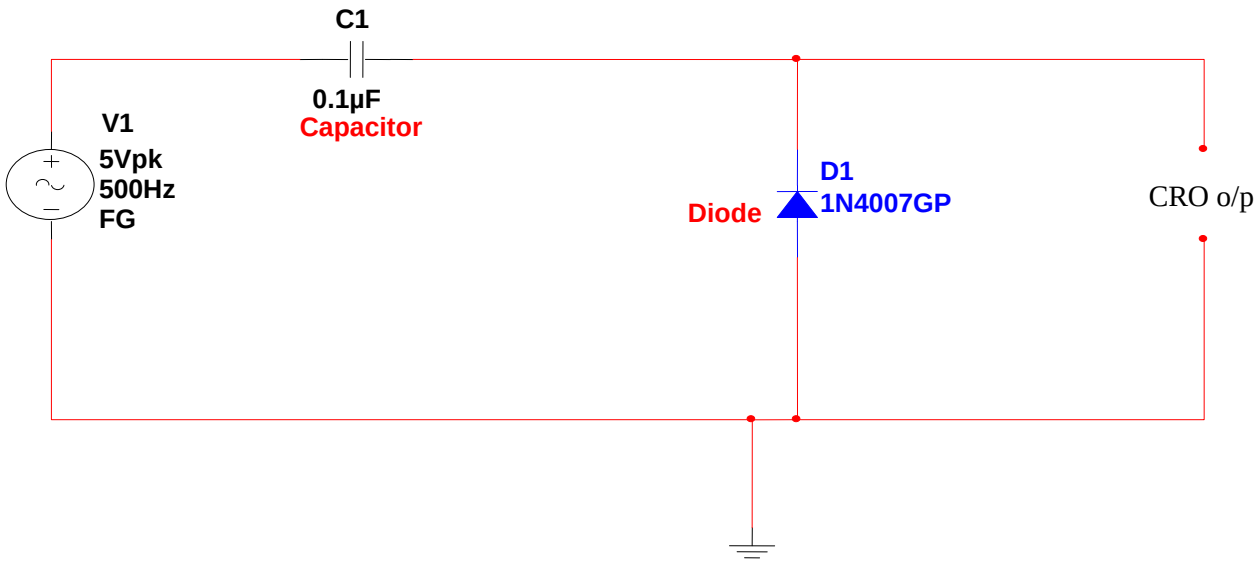
Input and Output waveform:



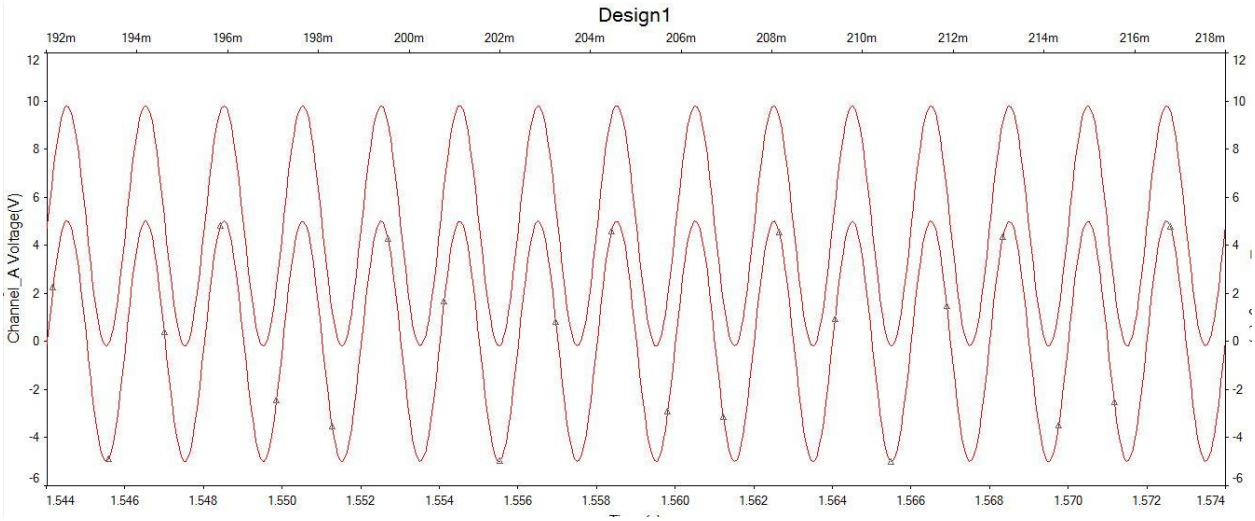
Tabular column:

S. No	Waveform	Amplitude	Frequency (time period)
1.			

Circuit Diagram: Clamper Circuit:



Input and Output waveform:



Tabular column:

S. No	Waveform	Amplitude	Frequency (time period)
1.			

Exp: 4(b) **Date:**

CLAMPERS

Aim: To study the clamping circuits.

Apparatus :

S. No.	APPARATUS	RANGE/RATING	QUANTITY
1	Diode	1N4007	1
2	Capacitors	0.1 µF	1
3	Function Generator	0 – 30 V	1
4	CRO	20 MHz	1
5	Bread board	--	1
6	Connecting Wires	-	As required

Procedure:

1. Connect the circuit as per the circuit diagram in Figure
2. In each case apply 10 VP-P, 1 KHz Sine wave I/P using a signal generator.
3. O/P is taken across the load R_L.
4. Observe the O/P waveform on the CRO and compare with I/P waveform.
5. Sketch the I/P as well as O/P waveforms and mark the numerical values with V_R = 2 V, 3 V.
6. Repeat the above steps for all the clamping circuits.

Result:

Successfully verified the output waveforms of different types of clamper circuits.

Conclusion:

1.

2.

Viva questions:

1.List different types of clampers.

2.Define series positive clipper.

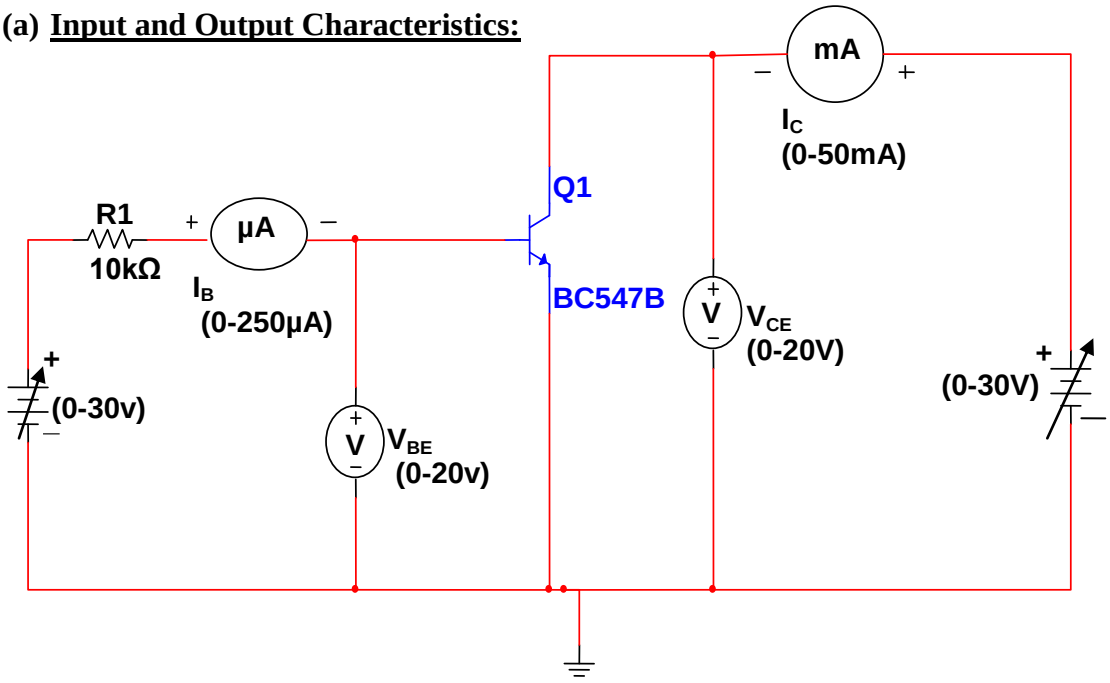
3.Define clamper.

4.Define biased clamper.

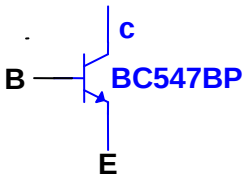
5. What are the applications of clampers?'

Circuit diagram:

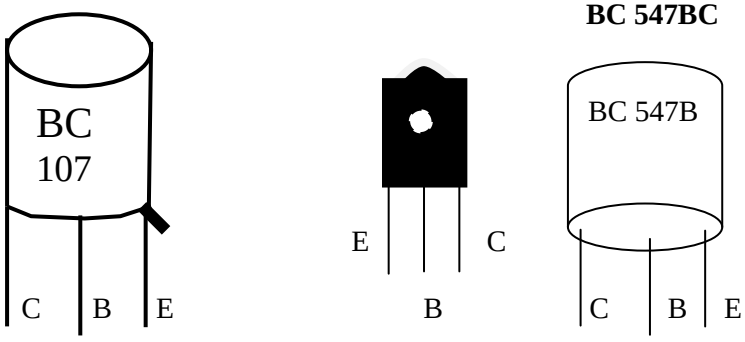
(a) Input and Output Characteristics:



SYMBOL OF TRANSISTOR:

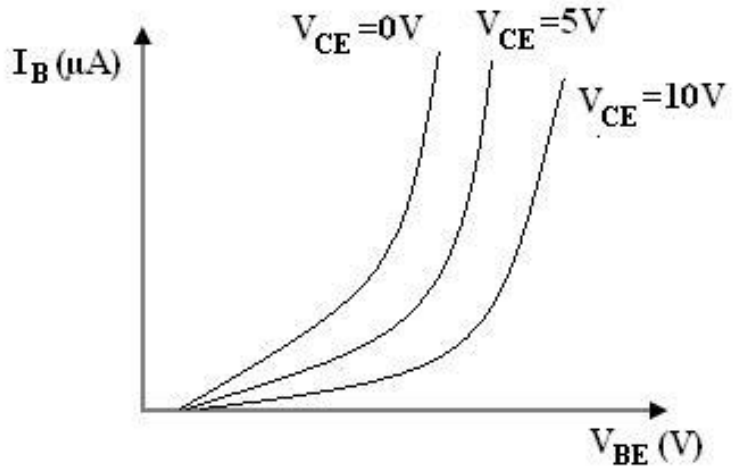


PIN DETAILS OF TRANSISTOR :

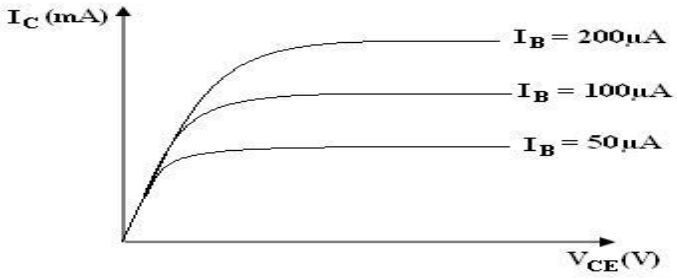


Model Graph:

Input characteristics:



Output characteristics:



Typical values:-

h_{ie}	h_{re}	h_{fe}	h_{oe}
1100Ω	2.5×10^{4}	50	25μΩ

Calculations:

1. Reverse voltage gain $h_{re}= \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right/$ **IB** Constant =
2. Input Impedance $h_{ie}= \left.\frac{\Delta V_{BE}}{\Delta I_B}\right/$ $\mathbf{V_{CE}}$ Constant =
3. Output admittance $h_{oe}= \left.\frac{\Delta I_C}{\Delta V_{CE}}\right/$ **IB** Constant =
4. Forward current gain $h_{fe}= \left.\frac{\Delta I_C}{\Delta I_B}\right/$ $\mathbf{V_{CE}}$ Constant =

Exp: 5(a) **Date:**

BJT CHARACTERISTICS (CE CONFIGURATION)

Aim:1. To Obtain Input and Output characteristics of transistor connected in Common Emitter Configuration.

2. To determine the h-parameters for CE configuration.

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	Power Supply(RPS)	0-30V	1
2	Transistor	BC107or BC 547	1
3	DC Ammeter	0-50mA	1
		0–500mA	1
4	DC Voltmeter	0–10V	1
		0 – 1V	1
5	Digital Multimeter(DMM)		1
6	Resistor	10KΩ	1
7	Bread board	--	1
8	Connecting wires	--	Required

Theory:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal `is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement IB increases less rapidly with VBE. Therefore input resistance of CE circuit is higher than that of CB circuit. The output characteristics are drawn between Ic and VCE at constant IB. the collector current varies with VCE unto few volts only. After this the collector current becomes almost constant, and independent of VCE. The value of VCE up to which the collector current changes with V CE is known as Knee voltage. The transistor always operated in the region above Knee voltage, IC is always constant and is approximately equal to IB. The current amplification factor of CE configuration is given by

$$\beta = \Delta I_C / \Delta I_B$$

Tabular column:
(a)Input characteristics:

S.NO	V_{CE}=		V_{CE}=		V_{CE}=	
	V_{BE}(V)	I_B (μA)	V_{BE}(V)	I_B (μA)	V_{BE}(V)	I_B (μA)

Tabular column:
b). output characteristics

S.No	I_B=		I_B=		I_B=	
	V_{CE}(V)	I_C (mA)	V_{CE}(V)	I_C (mA)	V_{CE}(V)	I_C (mA)

Procedure:

Input characteristics:

1. Connect the circuit as per the circuit diagram shown in Fig (1)
2. Simulate the circuit.
3. Set V_{CE} = 0 by adjusting V_{CC}.
4. Vary the input voltage V_{BB} and note the readings of I_B and V_{BE}.
5. Repeat the above procedure for V_{CE} = 2Vand 5V.
6. Plot the input characteristics V_{BE} Vs I_B for constant Values of V_{CE} = 0V, 2Vand 5V
7. Calculate h- parameters from input characteristics graph

$$\mathbf{V_{BE} = h_{ie}\, I_B + h_{re}\, V_{CE}}$$
$$\mathbf{I_C = h_{fe}\, I_B + h_{oe}\, V_{CE}}$$

a) Reverse voltage gain $h_{re} = \left.\frac{\Delta V_{EB}}{\Delta V_{CB}}\right|_{I_B \text{ Constant}}$

b) Input Impedance $h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} \text{ Constant}}$

Output characteristics:

1. Connect the circuit as per the circuit diagram shown in fig (2).
2. Simulate the circuit.
3. Set I_B = 50 μA by adjusting $V_{BB.}$
4. Vary the supply voltage V_{CC} and note the readings of I_C and V_{CE}. Take V_{CE}=V_{CC}.
5. Repeat the above procedure for I_B = 100 μA and 200 μA,
6. Plot the output characteristics V_{CE} vs I_C for constant Values of

   I_B =50 μA, 100 μA and 200 μA.
7. Calculate h- parameters from output characteristics graph

c. Output admittance $h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B \text{ Constant}}$

d. Forward current gain $h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} \text{ Constant}}$

Result: The input and output characteristics of a transistor in CE configuration are drawn. The Input (Ri) and Output resistances (Ro) of a given transistor are calculated.

1. The Input resistance (Ri) of a given Transistor is_____
2. The Output resistance (Ro) of a given Transistor is_____
3. The Current amplification factor is_____

Conclusion:

1.

2.

Viva questions:

1. What is a transistor?

2. What are the different types of BJT?

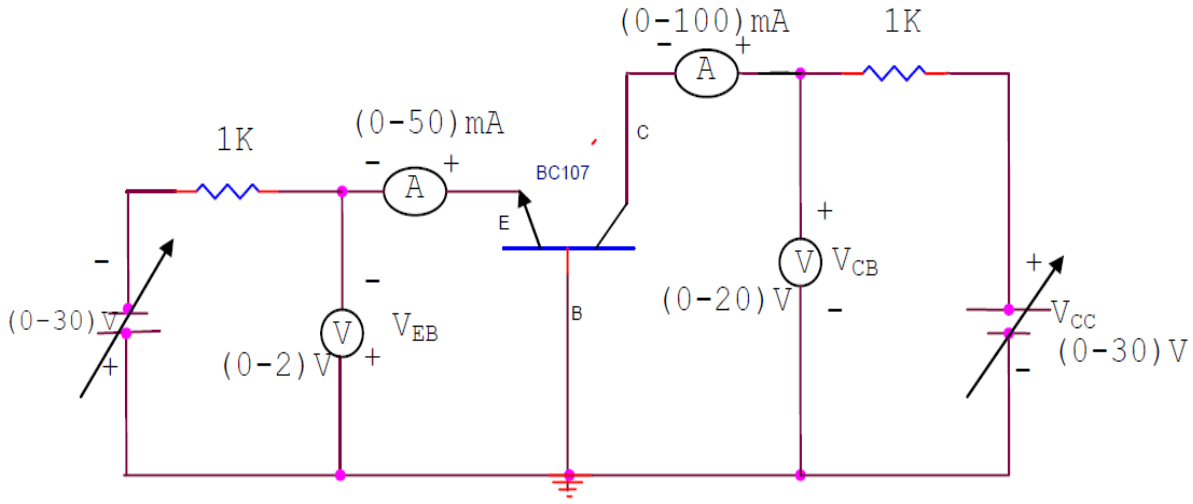
3. Define Cut-off, active and saturation regions?

4. What are the different configuration of transistor?.

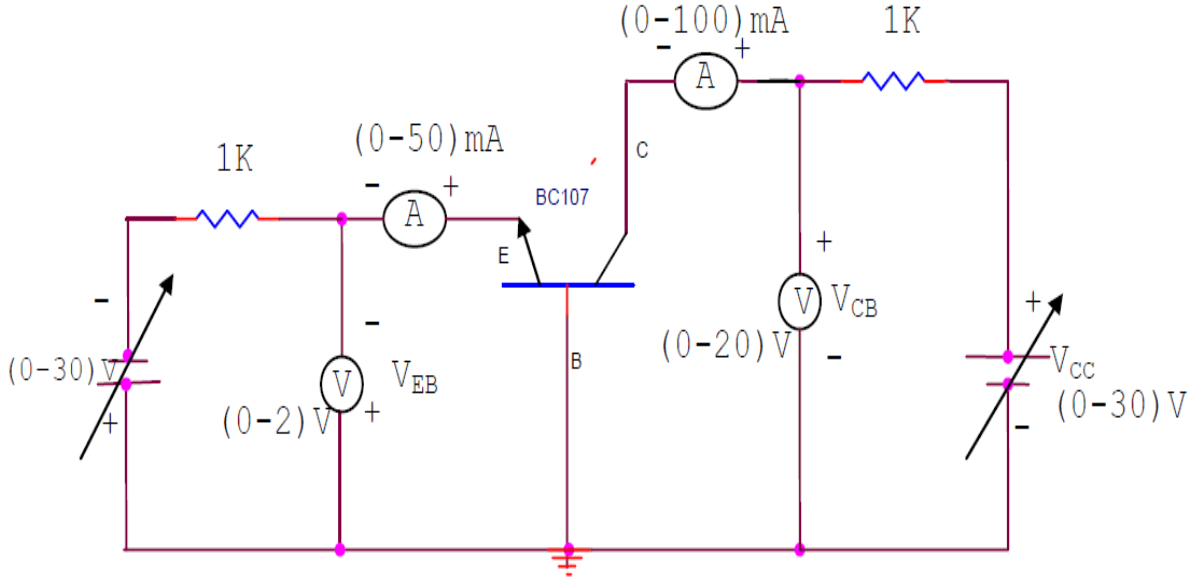
5. What is meant by Q-Point?

Circuit diagram:

(a)Input Characteristics:

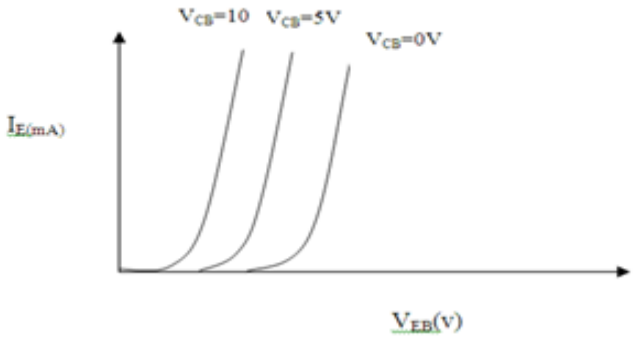


Output characteristics Circuit Diagram:

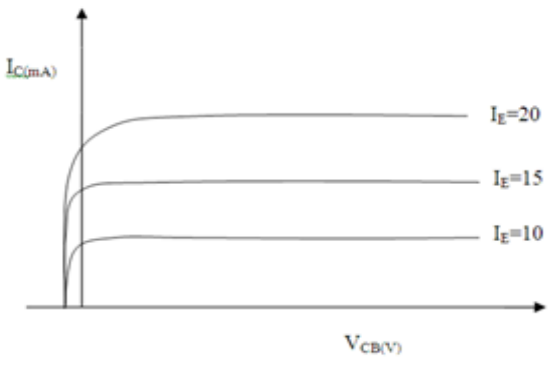


Model Graph:

Input characteristics:



Output characteristics:



Exp: 5(b) **Date:**

BJT CHARACTERISTICS (CB CONFIGURATION)

Aim: 1. To Obtain Input and Output characteristics of transistor connected in Common Base Configuration.

2. To determine the h-parameters for CB configuration.

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	Power Supply(RPS)	0-30V	1
2	Transistor	BC107or BC 547	1
3	DC Ammeter	0-50mA	1
		0–100 mA	1
4	DC Voltmeter	0–10V	1
5	Digital Multimeter (DMM)		1
6	Resistor	1KΩ	2
7	Bread board	--	1
8	Connecting wires	--	Required

Theory:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. In Common Base configuration the input is applied between emitter and base and the output is taken from collector and base. Here base is common to both input and output and hence the name common base configuration. Input characteristics are obtained between the input current and input voltage taking output voltage as parameter. It is plotted between VEB and IE at constant VCB in CB configuration. Output characteristics are obtained between the output voltage and output current taking input current as parameter. It is plotted between VCB and IC at constant IE in CB configuration.

The current amplification factor of CE configuration is given by $\alpha = \Delta I_C/\Delta I_E$

Result:

Thus the input and output characteristics of CB configuration are plotted and h parameters are found.

a) Input impedance (hib) =

b) Forward current gain (hfb) =

c) Output admittance (hob) =

d) Reverse voltage gain(hrb) =

(a)Input characteristics:

S.NO	V_{CB}=		V_{CB}=		V_{CB}=	
	V_{EB}(V)	I_E (mA)	V_{EB}(V)	I_E (mA)	V_{EB}(V)	I_E (mA)

Output characteristics:

S.No	I_E=		I_E=		I_E=	
	V_{CB}(V)	I_E (mA)	V_{CB}(V)	I_E (mA)	V_{CB}(V)	I_E (mA)

Calculations:

1. Reverse voltage gain $h_{rb}= \frac{\Delta V_{EB}}{\Delta V_{CB}} \Big/ I_E$ Constant =
2. Input Impedance $h_{ib}= \frac{\Delta V_{EB}}{\Delta I_E} \Big/ V_{CB}$ Constant =
3. Output admittance $h_{ob}= \frac{\Delta I_C}{\Delta V_{CB}} \Big/ I_E$ Constant =
4. Forward current gain $h_f \quad \frac{\Delta I_C}{\Delta I_E} \Big/ V_{CB}$ Constant =

Procedure:

Input characteristics:

1. Connect the circuit as per the circuit diagram shown in Fig (1)
2. Simulate the circuit.
3. Set V_{CB} = 0 by adjusting V_{CC}.
4. Vary the input voltage V_{EE} and note the readings of I_E and V_{BE}.
5. Repeat the above procedure for V_{CB} = 2Vand 5V.
6. Plot the input characteristics V_{BE} Vs I_E for constant Values of V_{CB}= 0V, 2Vand 5V
7. Calculate h- parameters from input characteristics graph

$$\mathbf{V_{EB} = h_{ib}\, I_E + h_{rb}\, V_{CB}}$$
$$\mathbf{I_C = h_{fb}\, I_E + h_{ob}\, V_{CB}}$$

a) Reverse voltage gain $h_{rb} = \left.\frac{\Delta V_{EB}}{\Delta V_{CB}}\right/ I_E$ Constant

b) Input Impedance $h_{ib} = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right/ V_{CB}$ Constant

Output characteristics:

1. Connect the circuit as per the circuit diagram shown in fig (2).
2. Simulate the circuit.
3. Set I_E = 50 mA by adjusting $V_{EE.}$
4. Vary the supply voltage V_{CC} and note the readings of I_C and V_{CB} Take V_{CB}=V_{CC}.
5. Repeat the above procedure for I_E = 100 mA and 200 mA,
6. Plot the output characteristics V_{CB} vs I_C for constant Values of

   I_E=50 mA, 100 mA and 200 mA.
7. Calculate h- parameters from output characteristics graph

c. Output admittance $h_{ob} = \left.\frac{\Delta I_C}{\Delta V_{CB}}\right|_{I_E}$ Constant

d. Forward current gain $h_{fb} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}}$ Constant

Conclusion:

1.

2.

Viva questions:

1. How to determine input characteristics of CB Configuration?

2. How to determine output characteristics of CB Configuration?

3. List the applications of CB Configuration.

4. List the advantages and disadvantages of CB Configuration.

5. Determine the H-Parameters of CB Configuration.

Exp: 6 **Date:**

VERIFICATION OF LOGIC GATES

Aim: To verify the truth tables of different logic gates.

Components Required:

S.NO	APPARATUS	SPECIFICATIONS	QUANTITY
1	IC's	74LS08, 74LS32, 74LS04, 74LS00, 74LS02, 74LS86	each 1No
2	Digital IC Trainer kit		1
3	Patch cards		Required

Theory:

Binary Logic gates consist of Binary variables and logical operations. The variables are designated by letters of alphabets such as A, B, C ….. or X, Y, Z ..…

With variables having two and only two distinct possible values 0 and 1.

AND: This operation is represented as 'dot'. The IC number of AND gate is 74LS08. The output of logical operation AND is 1 if and only if both inputs are 1 in all other cases it is 0.

$$Z = A \cdot B$$

OR: This operation is represented as 'plus'. The IC number of OR gate is 74LS32. The output of logical operation OR is 1 if any one of the input is 1. If both the inputs are 0, the output is 0.

$$Z = A + B$$

NOT: This operation is represented by a 'bubble' before a common gate. The IC number of NOT gate is 74LS04. The output NOT gate is 1 if the input is 0 and vice versa

$$Z = \overline{A}$$

NAND: This operation is a compliment of the AND function. It is graphically represented by an AND gate followed by a bubble. The IC number of NAND gate is 74LS00. The output is 1, if any of the input is 1.The output is 0 if both the inputs are0.

$$Z = \overline{A \cdot B}$$

NOR: This operation is a compliment of the OR function. It is graphically represented by an OR gate followed by a bubble. The IC number of NOR gate is 74LS02. The output of logical operation NOR is 0, if any one of the input is 1. The output is 1, if both the inputs are 0.

$$Z = A + B$$

EX - OR: The EXCLUSIVE – OR gate has a graphic symbol similar to that of OR gate except for the additional curved lines on the input side. If both the inputs are same the output is 1 otherwise the output is 0.

$$Z = \overline{A} . B + B . \overline{A}$$

Procedure:

1.The IC's are placed on the bread board.

2.A voltage of +5V is applied to pin no.14 and –Ve is applied to pin no.7.

3.Inputs and Outputs are connected according the gates which are taken.

4.For the input 1 we have to connect the input terminal to +5V and for 0 to –Ve.

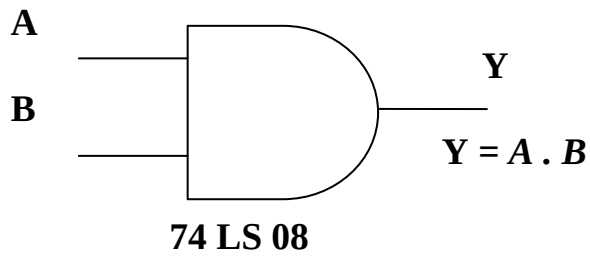
5.Output is verified in LED. If the LED is ON the output is 1, if OFF it is 0.

6.According to the Logic gates truth table we have to verify the inputs and outputs.

Result:

LOGIC GATES TRUTH TABLES

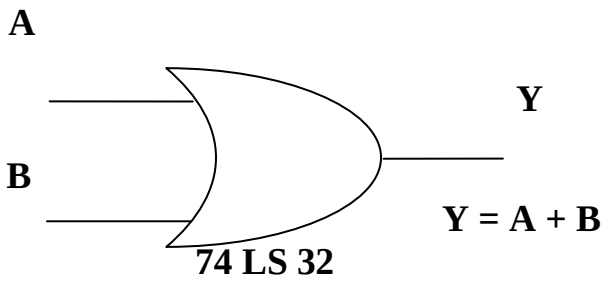
AND GATE:



74 LS 08

Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

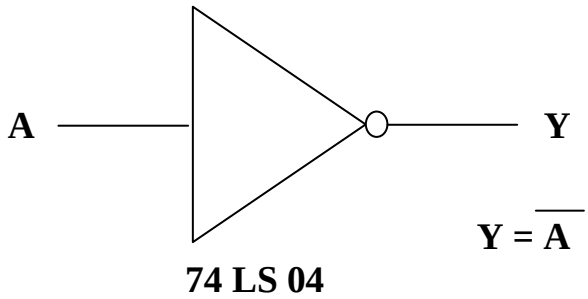
OR GATE:



74 LS 32

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

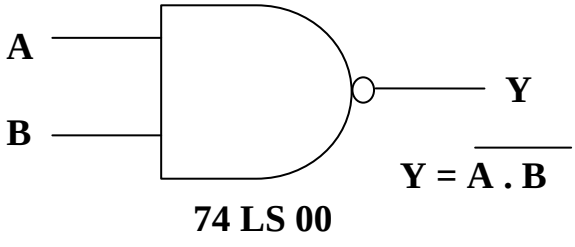
NOT GATE:



74 LS 04

Input	Output
A	Y
0	1
1	0

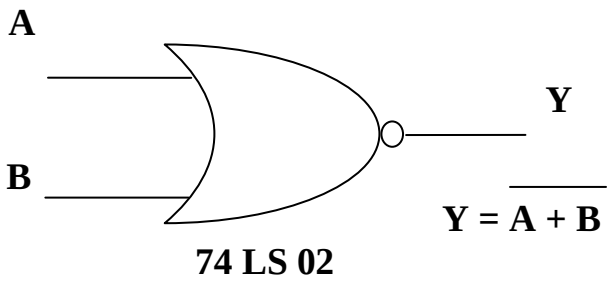
NAND GATE:



74 LS 00

Inputs		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

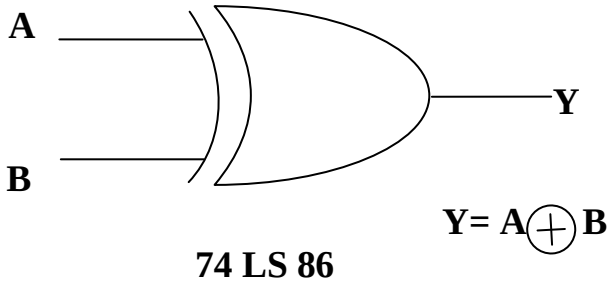
NOR GATE:



74 LS 02

Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

EXCLUSIVE - OR GATE:

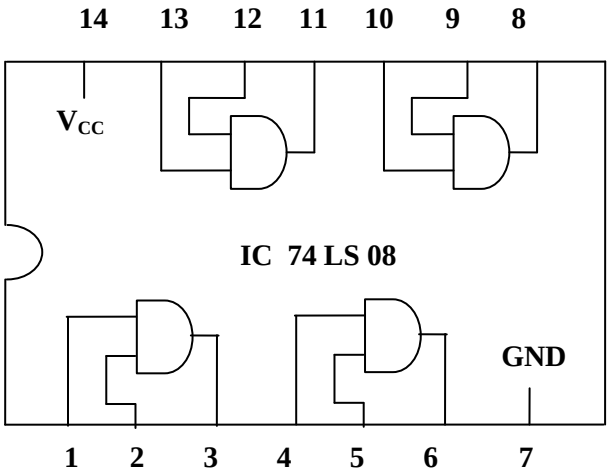


74 LS 86

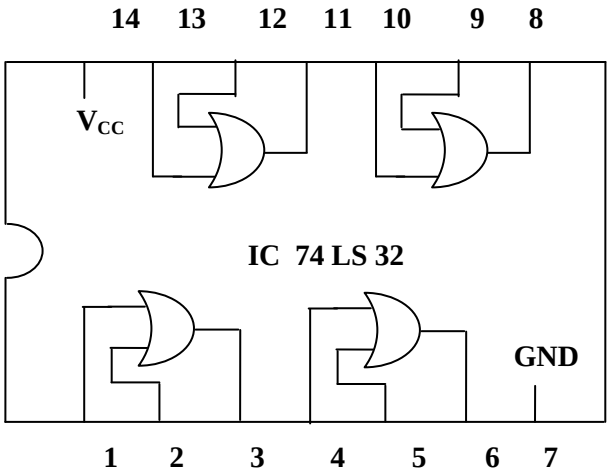
Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Pin details of Gates:

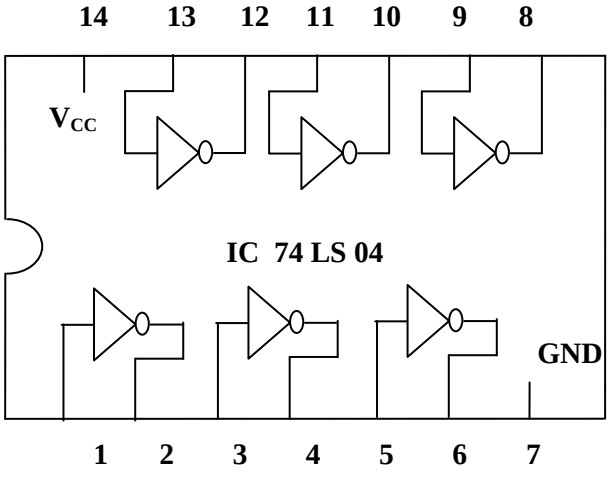
AND GATE



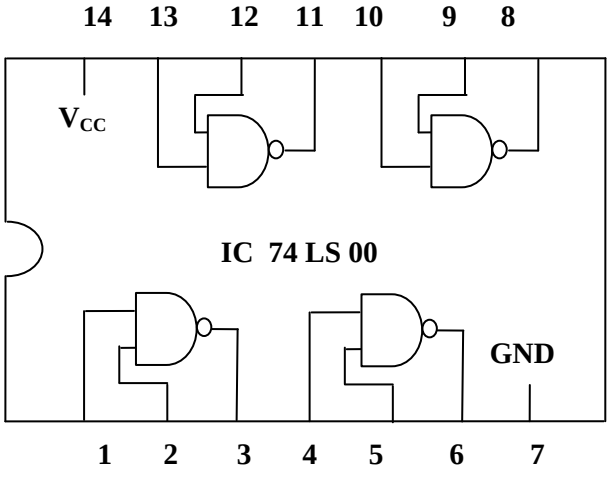
OR GATE



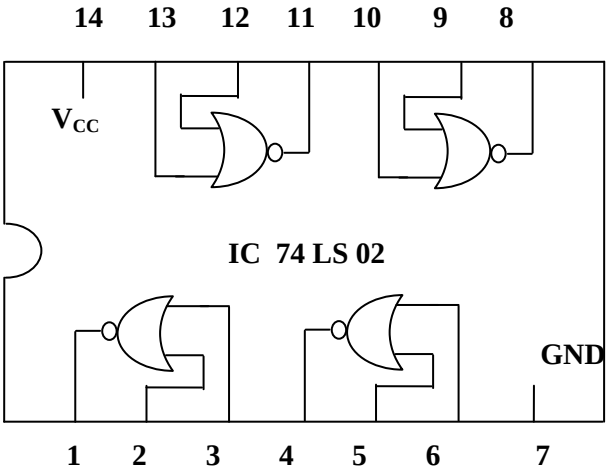
NOT GATE



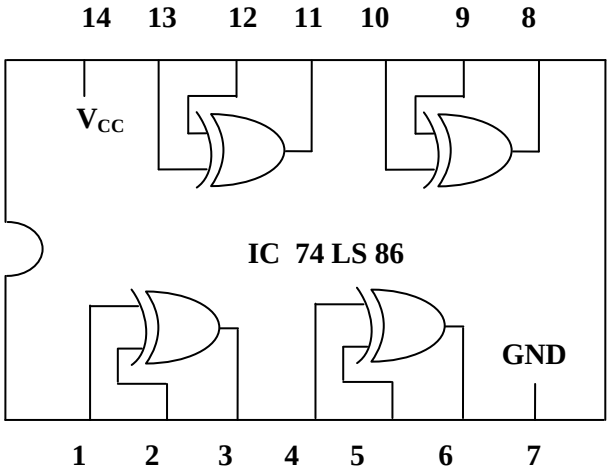
NAND GATE



NOR GATE



EX - OR GATE



Conclusion:

1.

2.

Viva questions:

1. What are the 7 logic gates?

2. What do you mean by logic gates?

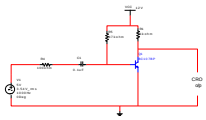
3. What are used to complement logic gates?

4. What is the principle of logic gates?

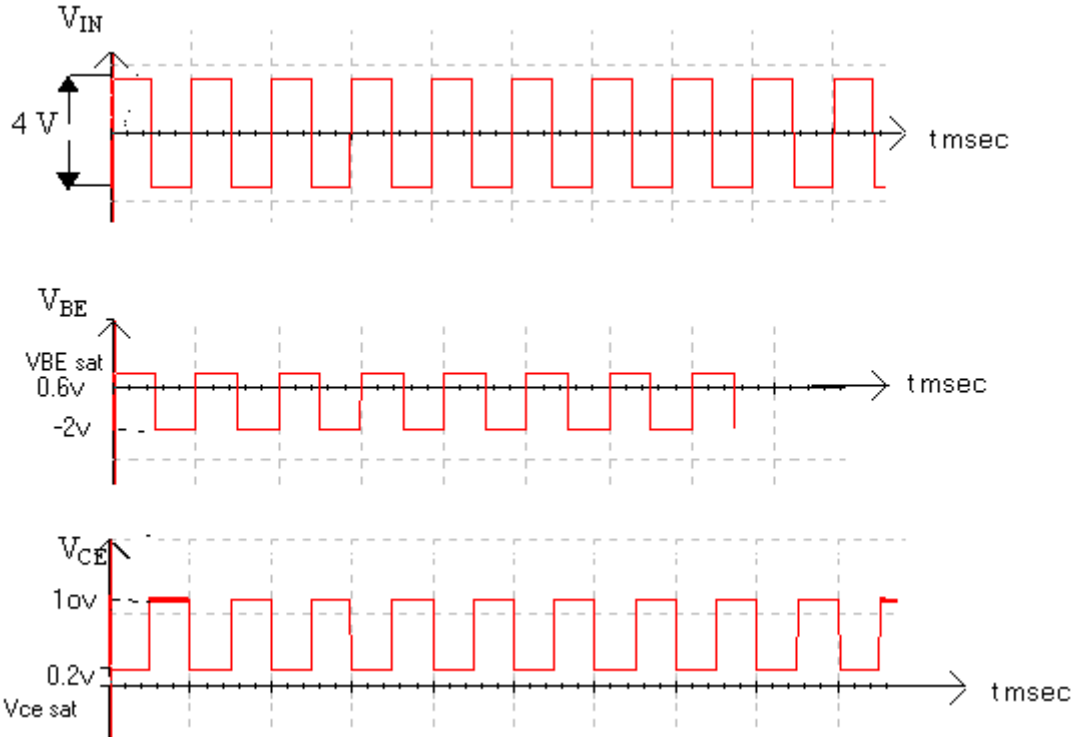
5. Who invented logic gates?

ADDITIONAL EXPERIMENTS

Circuit Diagram



Model Waveforms



Exp: 7 **Date:**

TRANSISTOR AS A SWITCH

Aim: To study the operation of Transistor as a switch.

Apparatus:

S.NO	APPARATUS	RANGE	QUANTITY
1	Function Generator	0-3MHz	1
2	CRO	0-30MHz	1
3	RPS	0-30 V	1
4	Transistor	BC 547/BC107	1
5	Digital Multimeter(DMM)		1
6	Resistors	100Ω,47K,1k	1
7	Bread board	--	1
8	Connecting wires	--	Required

Theory:

A transistor can work in 3 regions i.e., Active region Saturation region and Cut-off region. When the transistor is connected in CE configuration the conditions for active region is base-emitter junction forward bias and collector-emitter junction reverse bias.In this region transistor can act as an amplifier.

When emitter to base junction and collector emitter junction both are forward bias the transistor is said to be in 'Saturation Region'.

When emitter to base junction and collector to emitter junction are reverse bias the transistor is said to be in 'Cut-off region'.

To operate transistor as a switch it is made to operate in saturation or cut-off region. If the switch is ON it is saturation region. If the switch is OFF it is in cut-off region.

A pulse train with sufficient amplitude is applied to the transistor base. When pulse is at high the emitter -base and collector-base junctions are forward bias.

Thus transistor enters into saturation or is ON. When pulse is at low both the junctions are reverse biased and the transistor is cut-off or open circuited.

Depending up on the base control voltage the switch may be ON or OFF.

Procedure:

1. Connect the circuit elements as shown in the Circuit Diagram.
2. Applying the square wave voltage of 10V and frequency of 1000 Hz is applied to the circuit as an input.
3. Observe the corresponding output wave form at the collector of the transistor.
4. Note down the corresponding output wave forms in C.R.O and Plot the graph.

Precautions:

1. Check the wires for continuity before use.
2. Keep the power supply at zero volts before staring the experiment.
3. All the connections must be intact

Result:

Conclusion:

1.

2.

Viva questions:

1 .In which region of the characteristics transistor acts as a switch?

2. What is the typical value of the collector current on ON state?

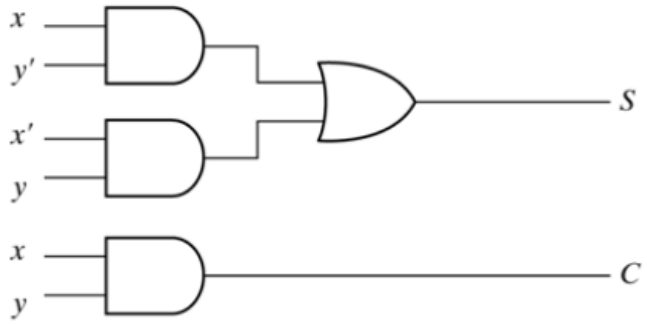
3. How the junctions of Transistor are biased in ON state and OFF state?

4. How does a transistor act as a switch?

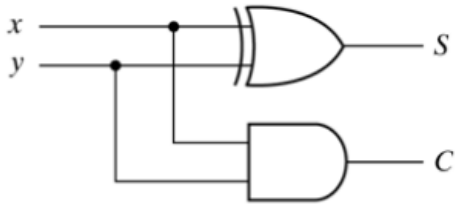
5. Which transistor is best for switching?

The logic circuit to implement is as shown below

HALF ADDER:



(a) $S = xy' + x'y$
$C = xy$



(b) $S = x \oplus y$
$C = xy$

TRUTH TABLE:

A	B	Sum (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Exp: 8 **Date:**

HALF ADDER

Aim: To verify the truth tables of half adder by using IC's.

Components Required:

S.NO	APPARATUS	SPECIFICATIONS	QUANTITY
1	IC's	74LS08, 74LS86	each 1No
2	Digital IC Trainer kit		1
3	Patch cards		Required

Theory:

A Half adder is a combinational circuit that performs addition of two input bits.

Half adder has inputs A, B and outputs sum (S) and carry(C). The carry output is 0 unless both inputs are 1. The simplified Boolean expressions are Sum S is one for input conditions AB=01 and AB=10 therefore $S=\bar{A}B+A\bar{B}$=A EXOR B. The carry C is one for AB=11 therefore C=AB

Procedure:

1.The IC's are placed on the bread board.

2.A voltage of +5V is applied to pin no.14 and –Ve is applied to pin no.7.

3.Inputs and Outputs are connected according the gates which are taken.

4.For the input 1 we have to connect the input terminal to +5V and for 0 to –Ve.

5.Output is verified in LED. If the LED is ON the output is 1, if OFF it is 0.

6.According to the half adder truth table we have to verify the inputs and outputs.

Result:

Conclusion:

1.

2.

Viva questions:

1. What is half adder?

2. What is the limitation of half adder?

3. What are the applications of half ladder?

4. How many gates are required for half adder?

5. What are the two types of basic adder circuits?

BASIC ELECTRICAL ENGINEERING LAB MANUAL

Department of Electrical and Electronics Engineering

VEMU INSTITUTE OF TECHNOLOGY::P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

(Approved by AICTE, New Delhi & Affiliated to JNTUA, Anantapuramu)

BASIC ELECTRICAL ENGINEERING LAB MANUAL

Name:_____

H.T.No:_____

Year/Semester:_____

Department of Electrical and Electronics Engineering

VEMU INSTITUTE OF TECHNOLOGY::P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

(Approved by AICTE, New Delhi & Affiliated to JNTUA, Anantapuramu)

COURSE OUTCOMES

Subject Name and Code	CO id	Course Outcomes	Level
Basic Electrical Engineering Lab (20A02101P)	C119.1	Analyze and verify the Kirchhoff's Laws & Superposition theorem	L4
	C119.2	Analyze the various characteristics on DC Machines by conducting various tests	L4
	C119.3	Analyze I –V Characteristics of PV Cell	L4
	C119.4	Apply the knowledge to perform various tests on 1-phase transformer	L3

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

B.Tech – II Sem

L	T	P	C
0	0	3	1.5

(20A02101P)Basic Electrical & Electronics Engineering Lab

(Civil, Mechanical, CSE, CSSE, IT and Food Technology)

Part A: Electrical Engineering Lab

Course Objectives:

1. To Verify Kirchoff's laws
2. To verify Superposition theorem.
3. To learn performance characteristics of DC Machines.
4. To perform open circuit & Short Circuit test on 1- Phase Transformer.
5. To Study the I – V Characteristics of Solar PV Cell

List of experiments: -

1. Verification of Kirchhoff laws.
2. Verification of Superposition Theorem.
3. Open circuit characteristics of a DC Shunt Generator.
4. Speed control of DC Shunt Motor.
5. OC & SC test of 1 – Phase Transformer.
6. Load test on 1 - Phase Transformer.
7. I – V Characteristics of Solar PV cell
8. Brake test on DC Shunt Motor.

COURSE OUTCOMES

After completing the course, the student will be able to

- Understand Kirchhoff's Laws & Superposition theorem.
- Analyze the various characteristics on DC Machines by conducting various tests.
- Analyze I –V Characteristics of PV Cell
- Apply the knowledge to perform various tests on 1-phase transformer.

CONTENTS

BASIC ELECTRICAL ENGINEERING LAB

PART-A ELECTRICAL ENGINEERING LAB

GENERAL INSTRUCTIONS FOR LABORATORY CLASSES

DO'S

1. Without Prior permission do not enter into the Laboratory.
2. While entering into the LAB students should wear their ID cards.
3. The Students should come with proper uniform.
4. Students should sign in the LOGIN REGISTER before entering into the laboratory.
5. Students should come with observation and record note book to the laboratory.
6. Students should maintain silence inside the laboratory.
7. Circuit connections must be checked by the lab-in charge before switching the supply

DONT'S

8. Students bringing the bags inside the laboratory..
9. Students wearing slippers/shoes insides the laboratory.
10. Students scribbling on the desk and mishandling the chairs.
11. Students using mobile phones inside the laboratory.
12. Students making noise inside the laboratory.
13. Students mishandle the devices.
14. Students write anything on the devices

SCHEME OF EVALUATION

S.No	Experiment name	Date	Marks Awarded				Total 30(M)
			Record (10M)	Observation (10M)	VivaVoce (5M)	Attendance (5M)	
1	Verification of Kirchhoff laws.						
2	Verification of Superposition Theorem.						
3	Open circuit characteristics of a DC Shunt Generator.						
4	Speed control of DC Shunt Motor.						
5	OC & SC test of 1 – Phase Transformer.						
6	Load test on 1 - Phase Transformer.						
7	I – V Characteristics of Solar PV cell						
8	Brake test on DC Shunt Motor.						
ADDITIONAL EXPERIMENTS							
9	Maximum Power Transfer Theorem						
10	Analysis Of RL & RC Circuits For Pulse Excitation						

Signature of Lab In-charge

CONTENTS

(20A02101P) BASIC ELECTRICAL ENGINEERING LAB

(Common to Civil, Mechanical, CSE)

PART-A ELECTRICAL ENGINEERING LAB

CIRCUIT DIAGRAMS:

Kirchho 's Voltage Law (KVL):

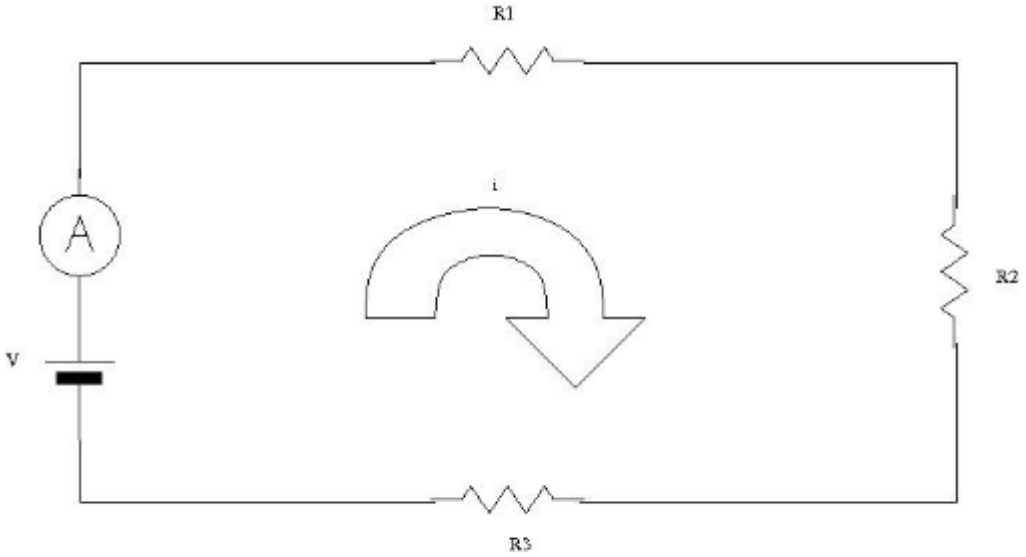


Figure 1: Loop circuit

Kirchhoff's Current Law (KCL) :

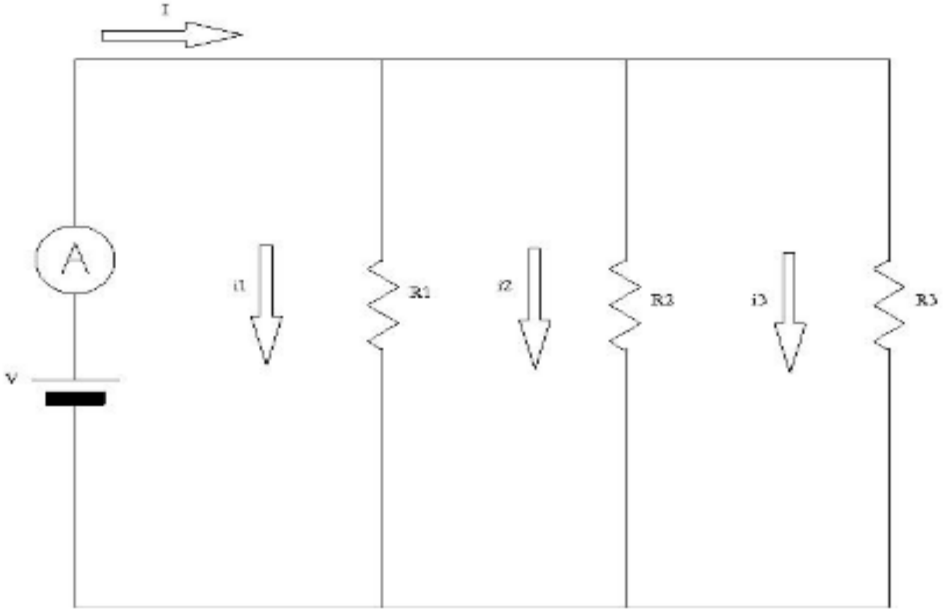


Figure 2: Node circuit

EXP.NO: **DATE:**

Verification of Kirchhoff laws

Aim:

To verify Kirchhoff's Laws by comparing voltages obtained from a real circuit to those predicted by Kirchhoff's Laws.

Apparatus:

1. Proto-board
2. Resistors: (R_1=68$k\Omega$, R_2=47$k\Omega$, R_3=15$k\Omega$, R_4=1000$k\Omega$)
3. Digital multi-meter
4. Variable power supply
5. Wire leads and alligator clips

Theory:

A simple circuit is one that can be reduced to an equivalent circuit containing a single resistance and a single voltage source. Many circuits are not simple and require the use of Kirchhoff's Laws to determine voltage, current, or resistance values. Kirchhoff's Laws for current and voltage are given by equations 1 and 2.

$$Equation\ 1: \sum_{Junction} I = 0,\ \ Junction\ Law$$

$$Equation\ 2: \sum_{Loop} \Delta V = 0,\ \ Loop\ Law$$

In this experiment, we will construct two circuits with 4 resistors and a voltage source. These circuits will not be simple, thus Kirchhoff's Laws will be required to determine the current in each resistor. We will then use a digital multi-meter to obtain an experimental value for the voltage across each resistor in the circuits. Kirchhoff's Laws will then be applied to the circuits to obtain theoretical values for the current in each resistor. By applying Ohm's Law, we can then obtain a theoretical value for the voltage across each resistor. The experimental and theoretical voltages can then be compared by means of % error.

Procedure:

Part 1:

1. Using the proto-board, the 4 resistors, the variable power supply, and the wire leads and alligator clips; construct the circuit shown in Figure 2.
2. Turn on the power supply. Connect the multi-meter across the power supply and adjust the voltage to 8.0 volts.
3. Connect the multi-meter across each of the 4 resistors. Record these 4 values of voltage in the data table.
4. Turn the power supply off and disconnect the circuit.

Procedure:

Part 2:

1. Add a second power supply to the circuit as shown in Figure 3.
2. Turn on the power supplies. Adjust the voltages V_0 and V_1 to 4.0 volts.
3. Connect the multi-meter across each of the 4 resistors. Record these 4 values of voltage in the data table.
4. Turn the power supply off and disconnect the circuit.

Analysis:

1. For the first circuit, use equations 1 and 2 to write a system of linear equations that may be solved for the current in each branch of the circuit. Then, solve the system to obtain a theoretical value for each current. Show your work!
2. Using the currents obtained in step 1 of the analysis; apply Ohm's Law to determine the theoretical voltage across each resistor.
3. Compare the theoretical voltages obtained in step 2 of the analysis to those measured in the actual circuit.
4. Repeat steps 1 to 3 for the second circuit.
5. Record the theoretical voltages, the experimental voltages, and the % errors in the results table.

Tabular columns:

KVL	V THEORITICAL	V PRACTICAL	% ERROR
R1			
R2			
R3			

KCL	V THEORITICAL	V PRACTICAL	% ERROR
R1			
R2			
R3			

RESULT:

Circuit Diagram:

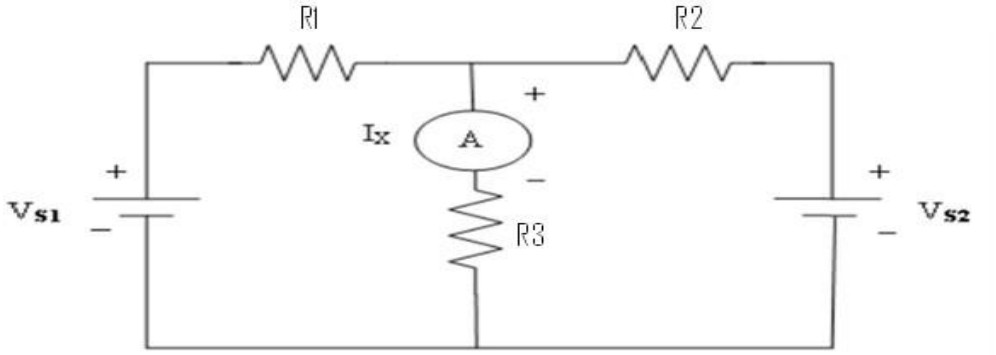


Fig-1

Case I: V_{S1} acting alone

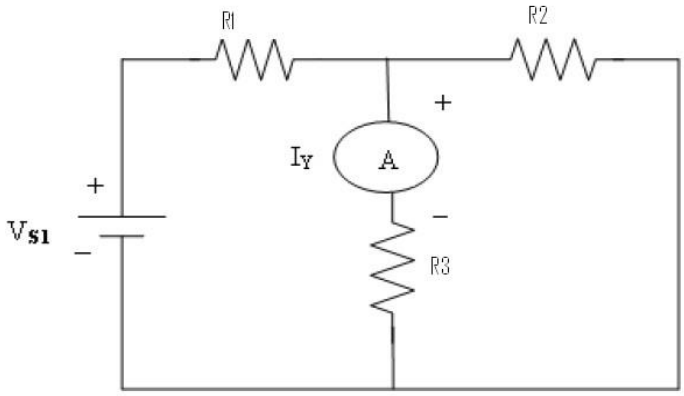
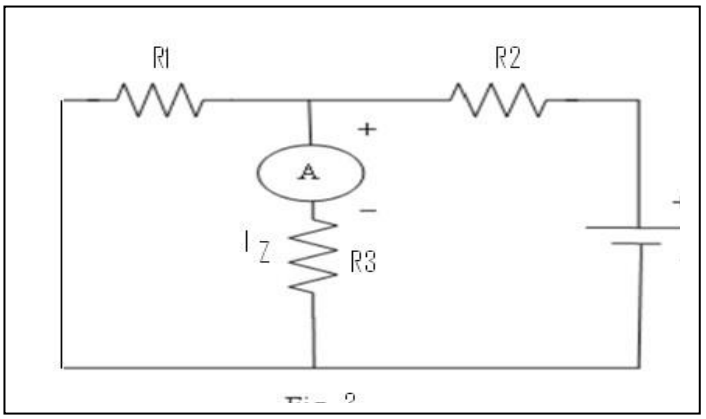


Fig-2

Case I: V_{S2} acting alone



EXP.NO: **DATE**

VERIFICATION OF SUPER POSITION THEOREM

AIM: Verification of Superposition theorem

APPARATUS:

S.No.	Name of the equipment	Range	Type	Quantity
1.	RPS	(0-30)V	..	1
2	Bread Board	..	..	1
3	Resistors			
5	Ammeter	(0-100)mA	MC	1
6	Connecting Wires	..	..	..

SUPERPOSITION THEOREM STATEMENT

In any linear bilateral network containing two or more energy sources the response at any element is equivalent to the algebraic sum of the responses caused by the individual sources.

i.e. While considering the effect of individual sources, the other ideal voltage sources and ideal current sources in the network are replaced by short circuit and open circuit across the terminals. This theorem is valid only for linear systems.

PROCEDURE:

1. Connect the circuit as shown in fig (1)
2. Current through load resistor is noted as I_X by applying both the voltages V1 and V2 through RPS.
3. Make the supply voltage V2 short circuited and apply V1 as shown in fig (2) and note down the current through load resistor as I_Y
4. Make the supply voltageV1 short circuited and apply V2 as shown in fig (3) and note down the current through load resistor as I_Z.
5. Now verify that $I_X = I_Y + I_Z$ theoretically and practically which proves Superposition Theorem.

THEORETICAL CALCULATIONS:-

TABULAR COLUMN:-

WHEN BOTH SOURCES ARE ACTIN FIG (1):

VS_1	VS_2	THEORETICAL Ix	PRACTICAL Ix

WHEN V1 SOURCE ALONE IS ACTING FIG (2):

VS_1	VS_2	THEORETICAL Ix	PRACTICAL Ix

WHEN V1 SOURCE ALONE IS ACTING FIG (3):

VS_1	VS_2	THEORETICAL Ix	PRACTICAL Ix

VIVA QUESTIONS:

1) What are the Statements of superposition theorem?

2) What is a linear network?

3) Where the above theorems are used practically?

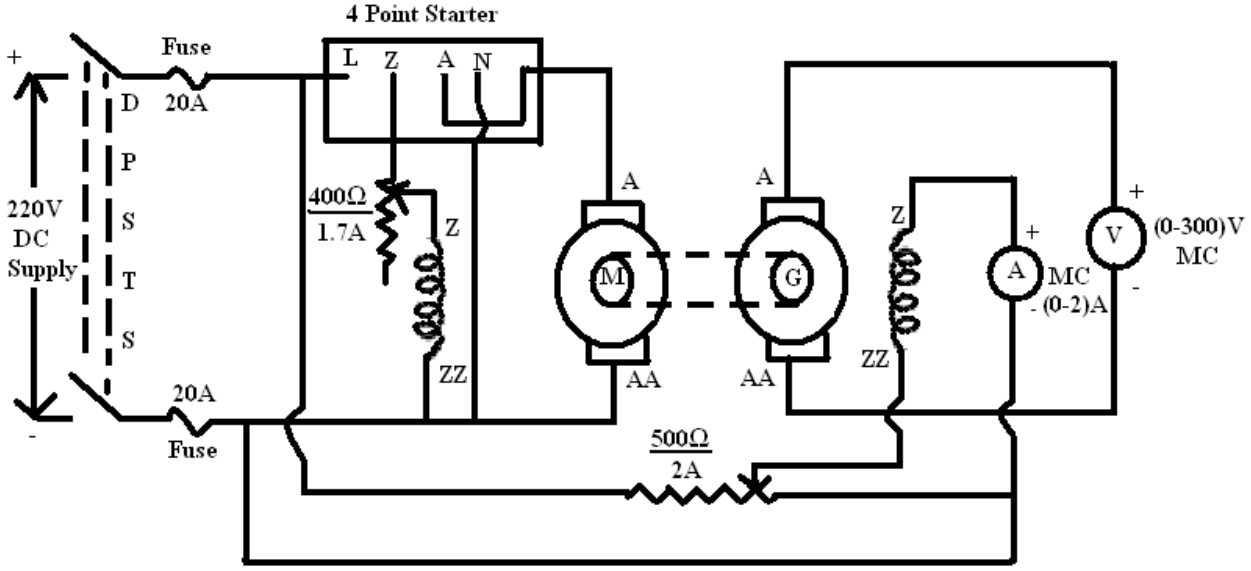
4) What are the practical applications of the above theorems?

5) What is a bilateral network? Give examples.

6) What are the limitations of above theorems?

Result:

Circuit Diagram:



EXP.NO: **DATE**

OPEN CIRCUIT CHARACTERISTICS OF A D.C GENERATOR

Aim:

To find critical field resistance of a separately excited D.C generator from its open circuit characteristics.

Apparatus:

S. No.	Name of the Equipment	Range	Type	Quantity
1	Voltmeter	(0-300)V	MC	1
2	Ammeter	(0-2)A	MC	1
3	Rheostat	400Ω/1.7A	Wire Wound	1
		500Ω/2A	Wire Wound	1
4	Tachometer	(0-9999)rpm	Digital	1
5	Connecting Wires	-	-	Required Some

Name Plate Details:

Precautions:

1. Motor field rheostat must be kept in minimum resistance position.
2. Potential Divider must be kept in maximum resistance position.
3. Starter arm must be in OFF position.

Procedure:

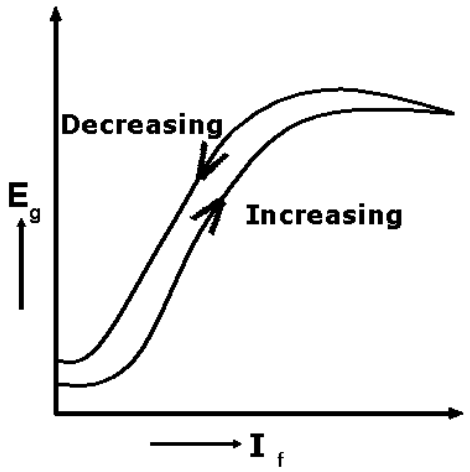
1. Connect the circuit as shown in circuit diagram.
2. Observing the precautions close the DPST Switch and switch ON 220V D.C supply.
3. Start the Motor Generator set with the help of starter.
4. Adjust the speed of the Motor Generator Set to rated speed value by adjusting motor field rheostat.
5. Increase the excitation of the generator in steps by adjusting the potential divider and note down the corresponding voltmeter and ammeter readings.
6. Take the readings up to a value little higher than the rated voltage of the generator.
7. Again decrease the excitation in the same steps till field current is zero by adjusting the potential divider noting down the corresponding voltmeter and ammeter readings.
8. Observing the precautions switch OFF the supply.

Tabular Column:

S. No.	I_f (A)	E_g (V) Increasing	E_g (V) Decreasing

1			
2			
3			
4			
5			
6			
7			
8			

Model Graph:



VIVA VOICE QUESTIONS:

1) Why the magnetization curve is a non linear curve?

2) What is critical Speed and Critical Resistance?

3) What are conditions to failure the self excitation?

4) What are the different methods of excitations?

5) Magnetization curves are also known as?

6) What are the characteristics of a dc generator?

7) What is Residual magnetism?

8) What is meant by magnetic saturation?

9) What is meant by the field flashing method?

10) What is meant by the residual voltage?

11) Why saturation curve for DC generator does not start with zero?

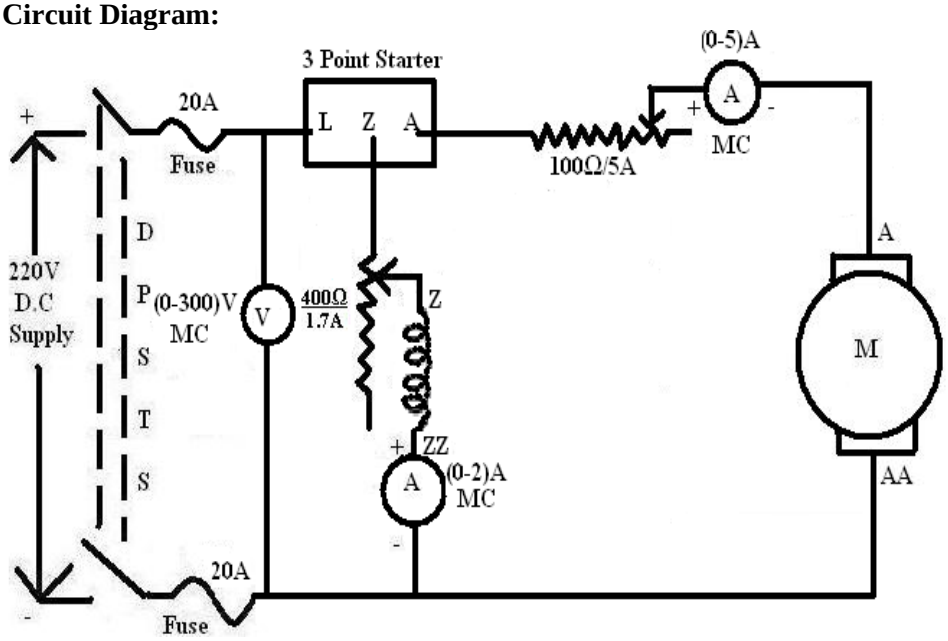
12) What is Open Circuit Characteristics of DC generator?

13) What are the different types of DC generators?

14) What are the characteristics of DC generators?

Result:

Circuit Diagram:



EXP.NO. **DATE**

SPEED CONTROL OF A D.C SHUNT MOTOR

Aim:

To obtain the speed characteristics of D.C Shunt Motor by

1. Armature Controlled Method.
2. Field Controlled Method.

Apparatus:

S. No.	Name of the Equipment	Range	Type	Quantity
1	Voltmeter	(0-300)V	MC	1
2	Ammeter	(0-2)A	MC	1
		(0-5)A	MC	1
3	Rheostat	400Ω/1.7A	Wire Wound	1
		100 Ω/5A	Wire Wound	1
4	Tachometer	(0-9999)rpm	Digital	1
5	Connecting Wires	-	-	Required Some

Name Plate Details:-

Precautions:

1. Field rheostat must be kept in minimum resistance position.
2. Armature rheostat must be kept in maximum resistance position.
3. Starter arm must be in OFF position.

Procedure:

Armature Controlled Method:

1. Connect the circuit as shown in circuit diagram.
2. Observing the precautions switch ON 220V D.C supply.
3. Start the motor with the help of starter.
4. By adjusting the field rheostat set the field current to a constant value.
5. By adjusting the armature rheostat for an armature voltage note down the speed and voltmeter readings.
6. Repeat step 5 for another constant field current.

Field Controlled Method:

1. By adjusting the armature rheostat set the voltage to a constant value.
2. By adjusting the field rheostat for a field current note down the speed and armature current readings.
3. Repeat the above step for another constant armature voltage.

Tabular Columns:

Armature Controlled Method:

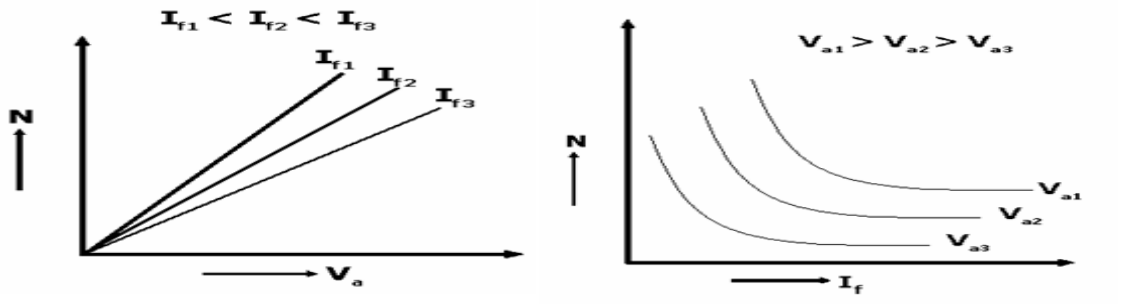
Field Current=0.8A		Field Current=0.6A	
V_a (V)	Speed (rpm)	V_a (V)	Speed (rpm)

Field Controlled Method:

Armature Voltage=160V		Armature Voltage=200V	
I_f (A)	Speed (rpm)	I_f (A)	Speed (rpm)

Model Graphs:

Armature Controlled Method **Field Controlled Method**



VIVA VOICE:

1) What is speed equation of DC shunt motor?

2) What is the no load speed of DC shunt motor?

3) What are the various speed control techniques of a dc motor?

4) Why DC shunt motor is called Constant speed motor?

5) What happens when the field of dc shunt motor gets open circuited during running condition?

6) Why field rheostat is kept minimum position at starting condition?

7) Which method we can obtain speed of motor is above its rated speed?

8) Which method we can obtain speed of motor is below its rated speed?

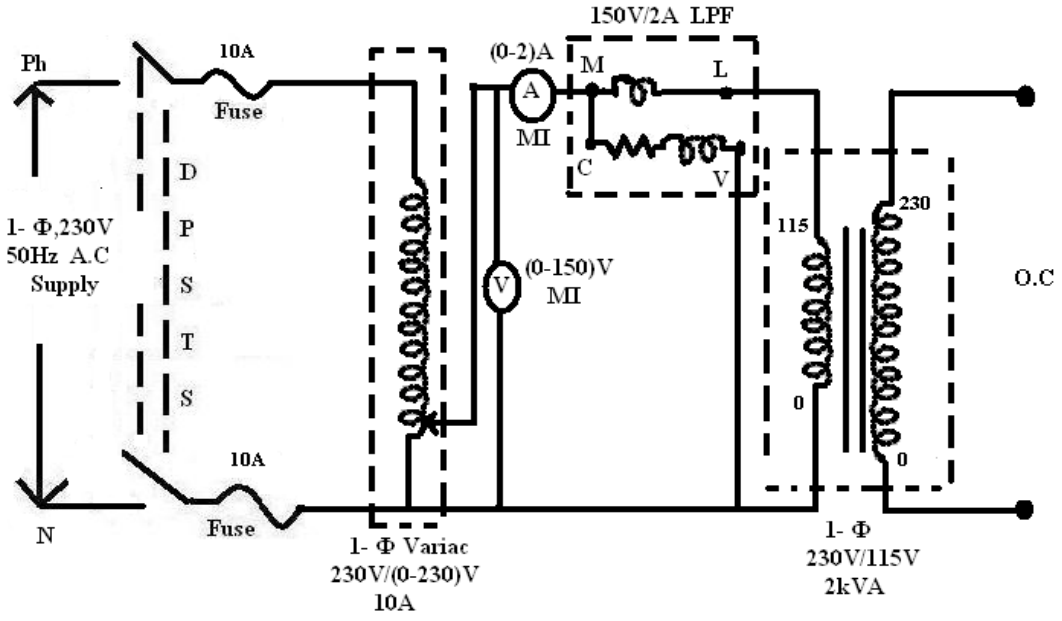
9) What versus us can draw speed curve field controlled method?

10) What versus us can draw speed curve armature controlled method?

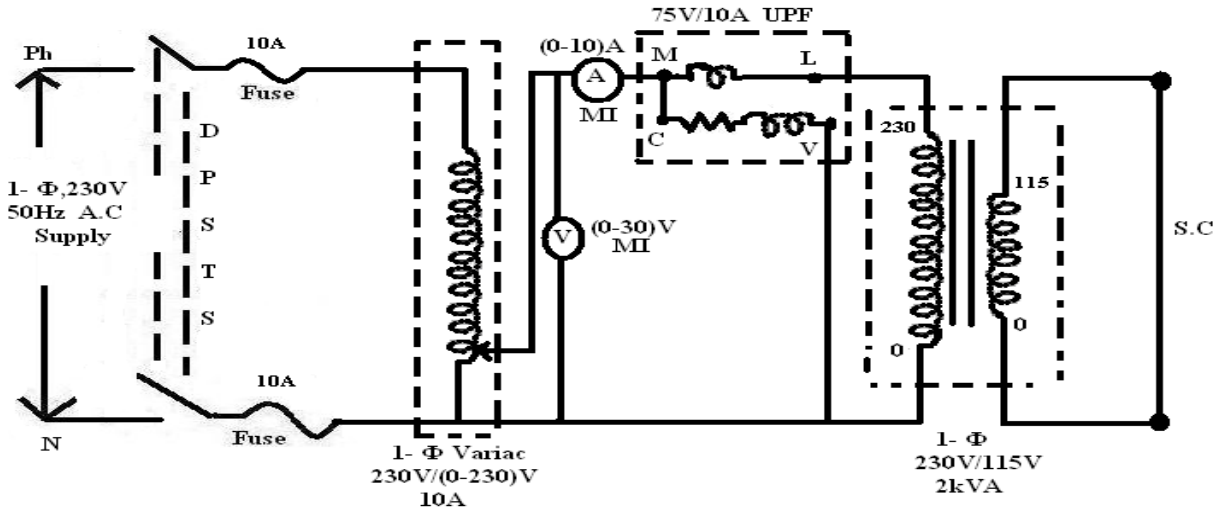
RESULT:

Circuit Diagram:

O.C Test:



S.C Test:



Exp. No.: **Date:**

O.C & S.C TESTS ON 1-Ø TRANSFORMER

Aim:

a) To determine the efficiency and regulation of 1- Ø transformer by conducting no-load and S.C Test.

b) To draw the equivalent circuit of 1- Ø transformer referred to L.V side as well as H.V side.

Apparatus:

S. No.	Name of the Equipment	Range	Type	Quantity
1	1- Ø Variac	230V/(0-270)V, 10A	-	1
2	1- Ø Transformer	115V/230V, 2kVA	Core	1
3	Ammeter	(0-10)A	MI	1
		(0-2)A	MI	1
4	Voltmeter	(0-150)V	MI	1
		(0-30)V	MI	1
5	Wattmeter	150V/2A	LPF	1
		75V/10A	UPF	1
6	Connecting Wires	-	-	Required Some

Name plate Details:-

Precautions:

1. Connections should be made tight.
2. 1- Ø Variac should be in minimum position.

Procedure:

O.C Test :

1. Connect the circuit as shown in circuit diagram for O.C test.
2. Observing the precautions switch ON 1- Ø A.C supply and by using the 1-Φ variac apply the rated voltage of the primary of the transformer.
3. Note down all the meter readings. Here wattmeter reading gives iron loss.
4. Observing the precautions switch OFF the supply.

S.C Test :

1. Connect the circuit as shown in circuit diagram for S.C test.
2. Observing the precautions switch ON 1- Ø A.C supply and by using the 1-Φ variac apply the rated current to the transformer. (Rated power of the transformer/Voltage of primary of transformer)
3. Note down all the meter readings, here wattmeter reading gives full-load copper loss.
4. Observing the precautions switch OFF the supply.

Tabular Columns:

O.C Test:

V_o (V)	I_o (A)	W_o = W X M.F (W)

S.C Test:

V_{SC} (V)	I_{SC} (A)	W_{SC} = W X M.F (W)

Efficiencies at different loads and power factor:

cosθ = 0.6				cosθ = 0.8			
Cu Loss (W)	Output power (W)	Input power (W)	Efficiency (%η)	Cu Loss (W)	Output (W)	Input (W)	Efficiency (%η)

Lagging Power Factor		Leading Power Factor	
Power Factor	% Regulation	Power Factor	% Regulation

Model Calculations:

Let the transformer be the step-down transformer (O.C Test)

Primary is H.V side and secondary is L.V side

$R_o=V_1/I_w$ (Ω) where $I_w=I_o\cos\Phi_o$

$X_o=V_1/I_\mu$ (Ω) where $I_w=I_o\cos\Phi_o$

$R_{o1}=W_{SC}/I_{SC}^2$ (Ω)

$Z_{O1}=V_{SC}/I_{SC}$

$X_{o1}=\sqrt{(Z_{O1}^2 - R_{o1}^2)}$

$R_{o2}=K^2 R_{o1}$

$X_{o2}=K^2 X_{o1}$

where,

$K=V_2/V_1$=Transformation Ratio

Calculations to find efficiency:

For example, at $1/4^{th}$ full load,

Copper Losses=W_{SC} x $(1/4)^2$ (w)

where, W_{SC}=Full Load Copper Losses

Constant Losses=W_o (W)

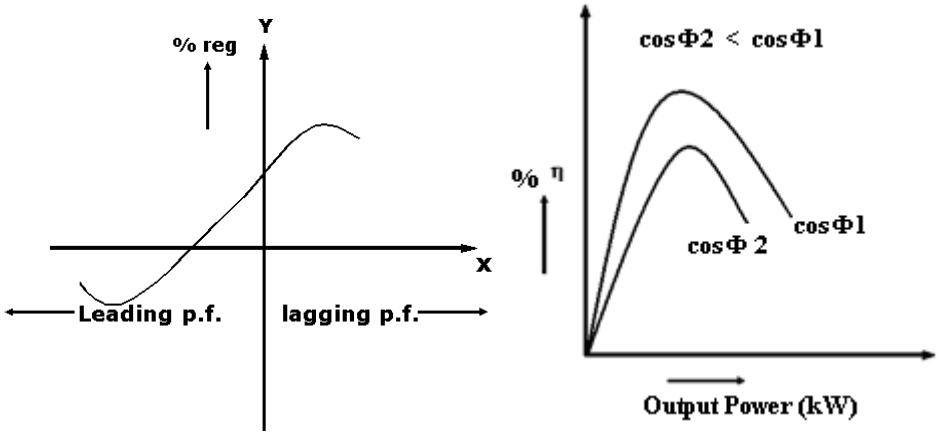
Output=(1/4) X VA X cosΦ (cosΦ may be assumed)

Input=Output + Copper Loss + Constant Loss

Efficiency (%η) = (Output/Input) X 100

Theoretical calculations:

MODEL GRAPHS:

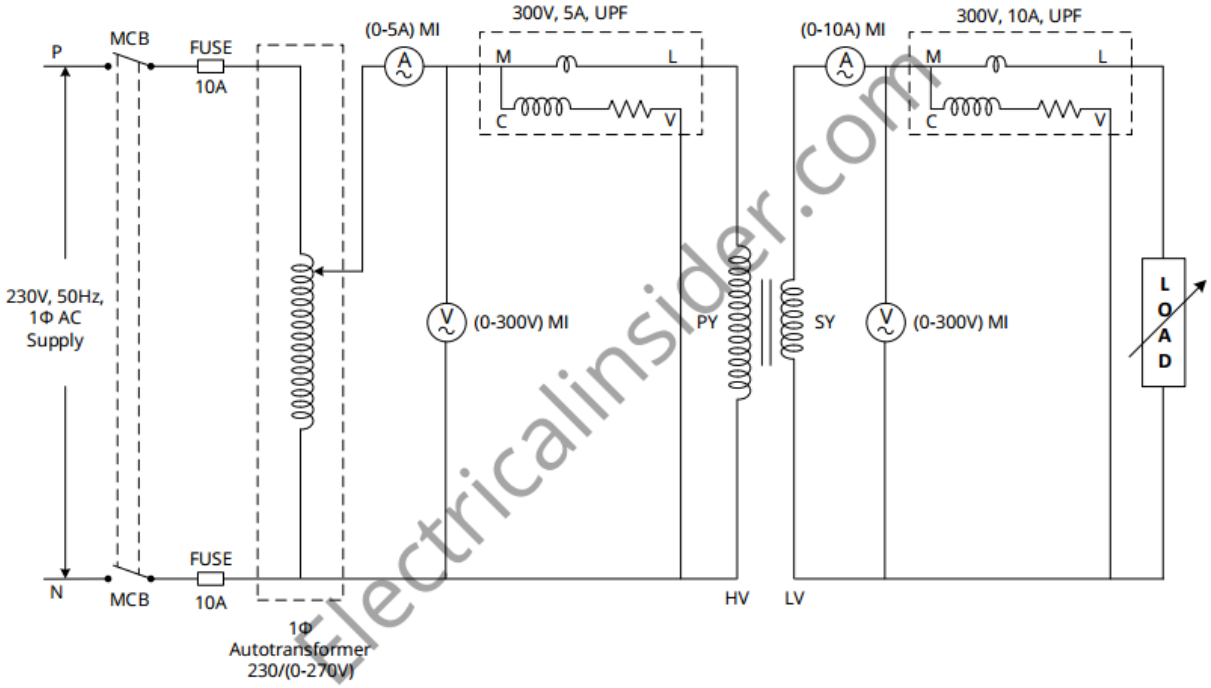


Viva Voce Questions:

1. Define transformer.
2. Distinguish the statically induced EMF and dynamically induced EMF.
3. Which losses can be determined from the O.C Test and S.C Test.
4. What is the main AIM's to conduct the O.C and S.C tests?
5. Define efficiency and voltage regulation of the transformer.
6. Why the O.C Test is conduct on L.V side.
7. Why the S.C Test is conducted on H.V side.
8. What is the difference between U.P.F and L.P.F wattcmeters?
9. No load power factor angle of transformer is around……
10. For which type of load negative voltage regulation occurs.
11. For which type of load maximum voltage regulation occurs.

Result:

Circuit Diagram:



Exp. No.: **Date:**

LOAD TEST ON 1-Ø TRANSFORMER

Aim:

To conduct Load test on the given 1-Φ Transformer and to plot its performance characteristics.

Apparatus:

S.NO	NAME OF THE APPARATUS	RANGE	TYPE	QUANTITY
1.	Ammeter	(0-5)A	MI	1
		(0-10)A	MI	1
2.	Voltmeter	(0-150)V	MI	1
		(0-300)V	MI	1
3.	Wattmeter	150V, 10A	UPF	1
		300V, 5A	UPF	1
4.	Autotransformer	230V/(0-270V)	-	1
5.	Single Phase Transformer	1 kVA	Dry Type	1
5.	Single Phase Resistive Load	-	-	1
6.	Connecting wires	-	-	As required

Name Plate Details:

Rated kVA	
Rated Primary Voltage	
Rated Secondary Voltage	
Rated Primary Current	
Rated Secondary Current	

Precautions:

1. At the time of starting the test, all the load should be kept off.
2. When loading the transformer, the secondary current should not exceed the rated current.

Procedure:

1. Make connections as per the circuit diagram.
2. Switch on the supply and apply the rated voltage of secondary winding by varying the autotransformer.
3. Note down the ammeter, voltmeter, and wattmeter reading for the no-load condition.
4. Switch on the load and apply the load in steps up to the rated secondary current.
5. Note down the ammeter, voltmeter and wattmeter readings for each step of the
6. Reduce the load and then switch off the supply.
7. Tabulate the readings and perform necessary calculations with the given formula to find efficiency and regulation.

Tabular Column:

Multiplication factor 1 _____

Multiplication factor 2 _____

S.No	Primary Voltage V_1 (Volts)	Primary Current I_1 (Amps)	Input Power (W_1) Watts		Secondary Voltage V_2 (Volts)	Secondary current I_2 (Amps)	Output Power (W_2) Watts		% Efficiency	% Voltage Regulation
			Observed	Actual			Observed	Actual		

Formulae:

Formulae for finding efficiency and regulation

The following formulas can be used to find the efficiency and regulation of a single phase transformer.

$$\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} \times 100$$

$$\text{Regulation} = \frac{V_{SO} - V_S}{V_{SO}} \times 100$$

Where

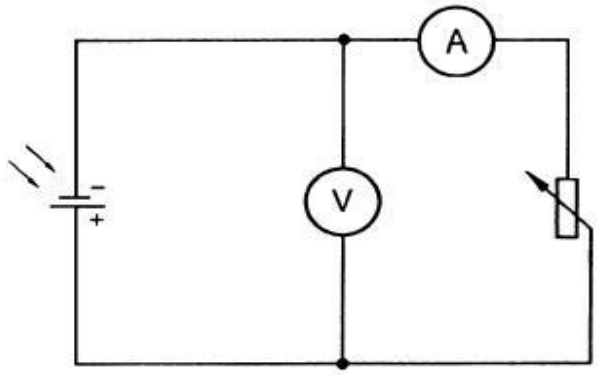
V_{SO} – Secondary terminal voltage at no-load

V_S – Secondary terminal voltage on load

Theoretical Calculations:

Result:

CIRCUIT DIAGRAM:



EXP.NO: **DATE:**

I-V CHARACTERISTICS OF SOLAR PV CELL

AIM: Find the current and voltage response under illumination depending on the magnitude of the variable resistance.

APPARATUS:

1- Source
2- Variable resistance
3- Slid board
4- Voltmeters

PROCEDURE:

1. In this measurement we want to record with high accuracy the voltage versus current dependence on our device.

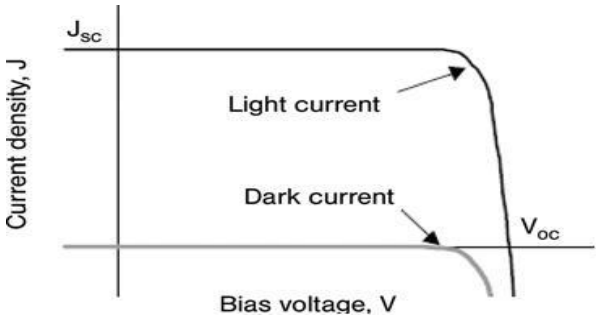
2. While the previous measurement allowed us to see the response of the device to different colors of light we did not get any accurate information as to the magnitude of the response. 3. It's important when reporting the performance of a solar cell to report the efficiency of the response to a solar light source we will now allow bright white light to excite the solar cell .

4.we will record the current and voltage response under this illumination depending on the magnitude of variable resistance.

TABULAR COLUMN:

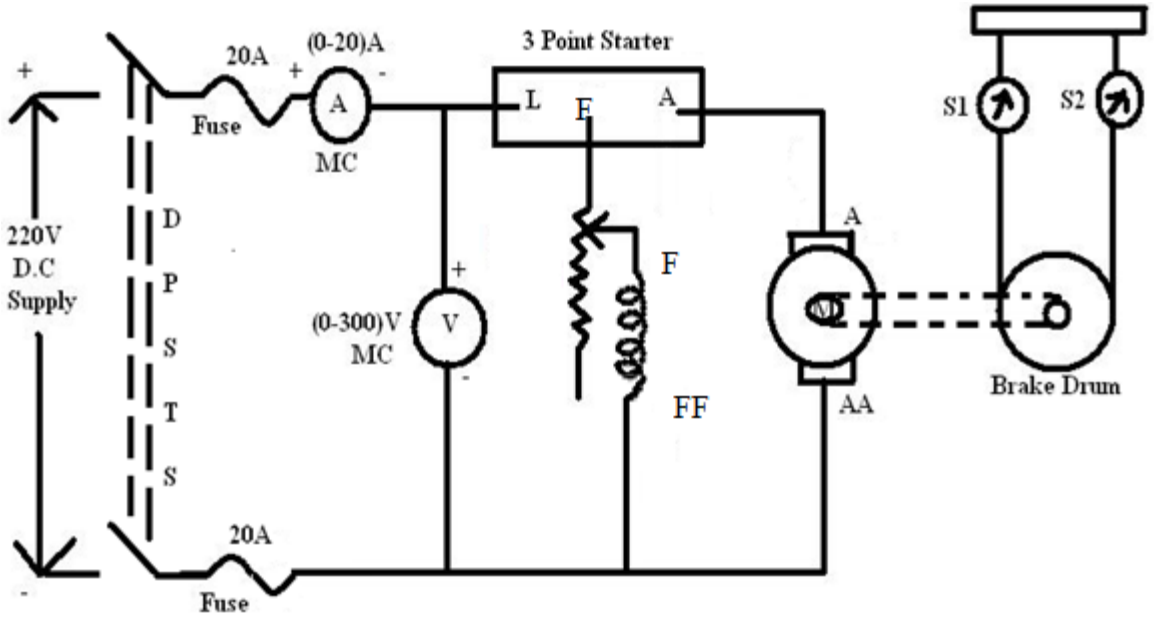
S.NO	VARIABLE RESISTANCE	VOLATGE	CURRENT	POWER

MODEL GRAPH:



RESULT:

Circuit Diagram:



Exp. No.: **Date:**

BRAKE TEST ON D.C SHUNT MOTOR

Aim:

To obtain the performance characteristics of D.C Shunt Motor by direct loading.

Apparatus:

S. No.	Name of the Equipment	Range	Type	Quantity
1	Voltmeter	(0-300)V	MC	1
2	Ammeter	(0-20)A	MC	1
3	Rheostat	360Ω/1.2A	Wire Wound	1
4	Tachometer	(0-9999)rpm	Digital	1
5	Connecting Wires	-	-	Required Some

Name plate details:

Precautions:

1. Motor field rheostat must be kept in minimum resistance position.
2. Starter arm must be in OFF position.

Procedure:

1. Connect the circuit as shown in circuit diagram.
2. Observing the precautions switch ON 220V D.C supply.
3. Start the motor with the help of the starter.
4. By adjusting the motor field rheostat bring the motor to its rated speed.
5. Now load the motor in steps to its full load and note down all the meter readings.
6. Observing the precautions switch OFF the supply.

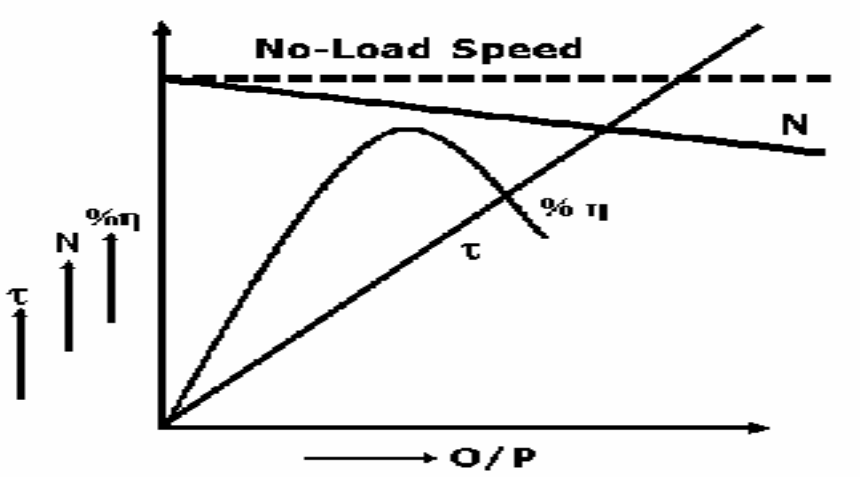
Tabular Column:

S. No.	Supply voltage V_L (V)	Line current I_L (A)	Speed N (rpm)	Spring Balance Reading			Torque (N-m)	Input power (kW)	Output Power (kW)	Efficiency ŋ (%)
				S_1	S_2	S_1-S_2				
1										
2										
3										
4										
5										
6										
7										
8										

Formulae:

Torque = 9.81 X (S_1-S_2) X R N-m
Input = V_L I_L kW
Output = 2∏NT/60 kW
Efficiency = ŋ % = (Output/Input) X 100

Model Graph:



Theoretical calculations:

VIVA VOICE QUESTIONS:

1) What is the principle operation of DC motor?

2) What is the Range of Shunt field Resistance?

3) What is no load current of Dc shunt motor?

4) How the Direction of a motor can be reversed?

5) What is Back EMF or counter EMF?

6) Why the Shunt motor is called a constant speed motor?

7) What are the applications of DC shunt motor?

8) What is purpose of starter?

9) What meant by the DPDTS?

10) What is the output power the dc motor?

11) What is speed regulation of DC motor?

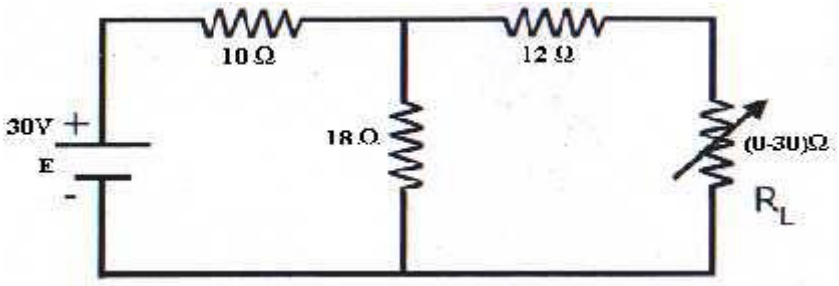
12) Explain principle of operation of DC motor?

13) Why shunt motor field winding has more no of turns?

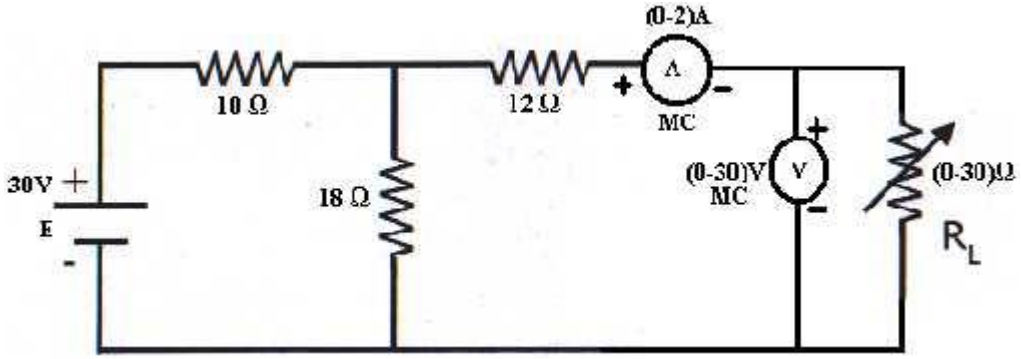
14) What happens when DC motor is connected across AC supply?

Result:

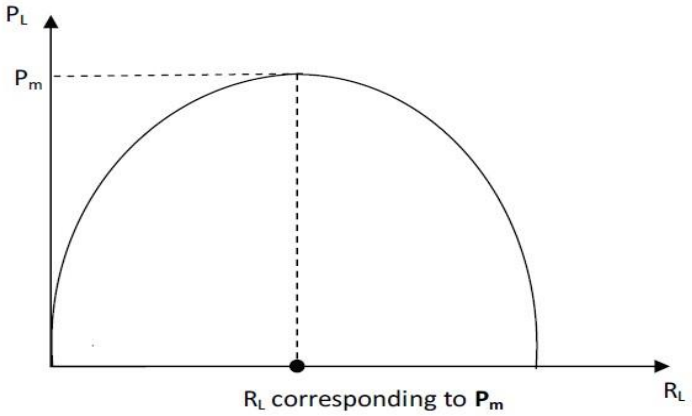
Circuit Diagram:



Practical Circuits:



MODEL GRAPH



EXP.NO: **DATE:**

MAXIMUM POWER TRANSFER THEOREM

AIM: To verify maximum power transfer theorem theoretically and practically.

APPARATUS:

S.No.	Name of the equipment	Range	Type	Quantity
1.	RPS	(0-30)V	..	1
2	Bread Board	..	..	1
3	Resistors			
4	Ammeter	(0-500)mA	MC	1
5	Voltmeter	(0-30)V	MC	1
6	DRB	(0-1)M ohm	..	1
7	Connecting Wires	..	..	..

Statement for maximum power transfer theorem:

It states that the maximum power is transferred from the source to the load, when the load resistance is equal to the source resistance.

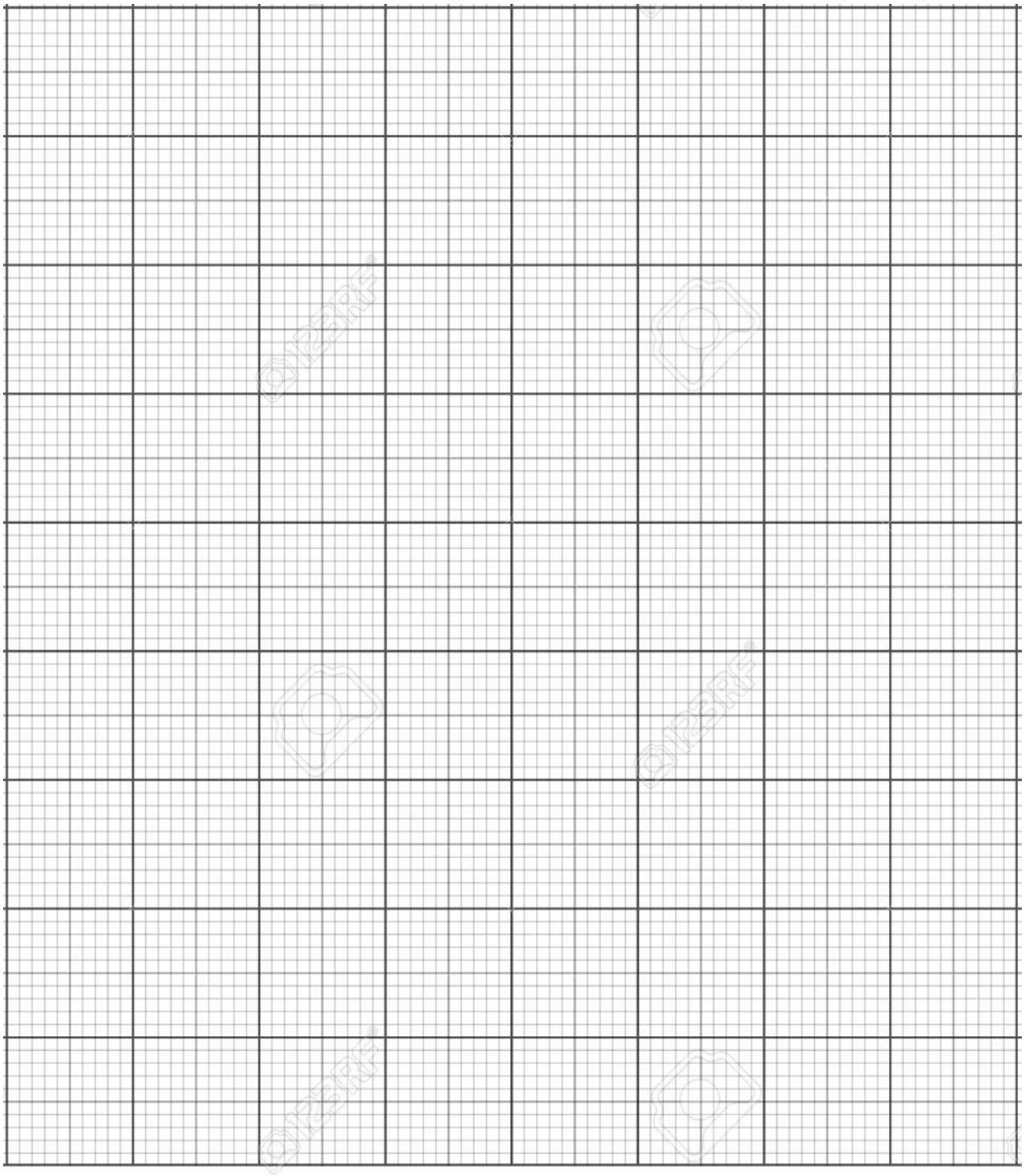
PROCEDURE:

1. Make the connections as shown in fig (1).
2. By varying RL in steps, note down the reading of ammeter IL in each step.
3. Connect the circuit as shown in fig (2), measure the effective resistance R_{th}.with the help of digital multi meter.
4. Calculate power delivered to load PL in each step.
5. Draw a graph PL Vs RL and find the RL corresponding to maximum power from it.
6. Verify that RL corresponding to maximum power from the graph is equal to the R_{th}(which is nothing but source resistance RS).

Tabular Column

S.No.	V_S (V)	V_L (V)	I_L (A)	$R_L = \frac{V_L}{I_L}$ (Ω)	$P = V_L I_L$ (W)

Theoretical Calculations:



Result:

VIVA QUESTIONS:-

1) What is the Statement of Maximum Power Transfer theorem?

2) What is a non linear network?

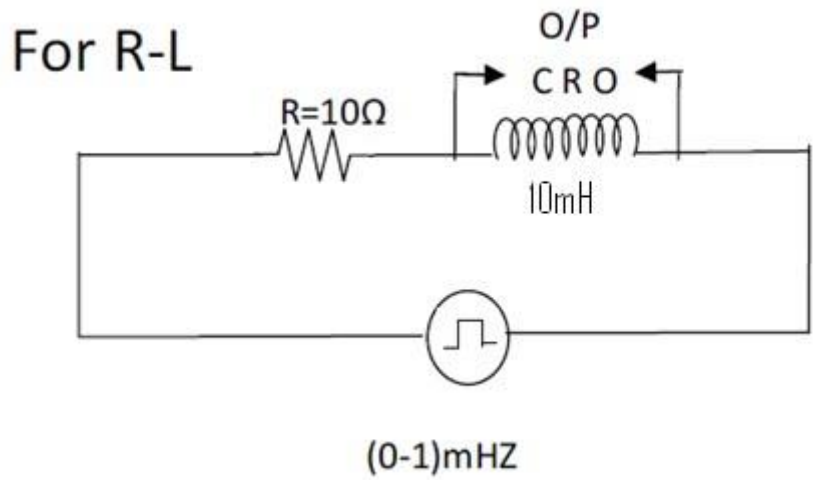
3) What is a unilateral network?

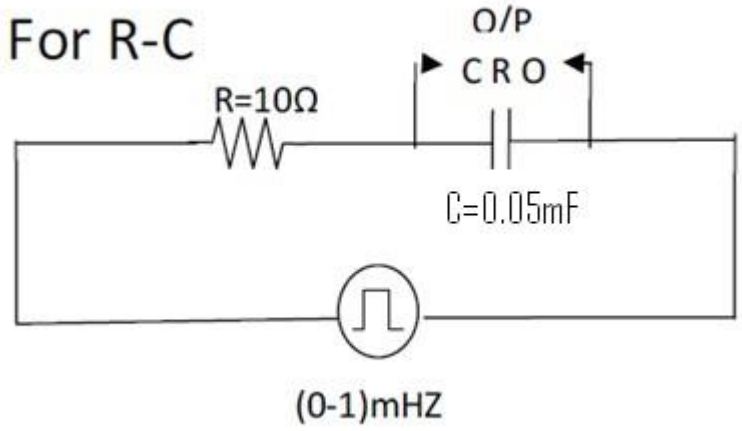
4) What are the applications of the above theorem?

5) What are the advantages & disadvantages of the above theorem?

6) State the maximum power transfer theorem for AC network?

Circuit Diagram:





EXP.NO: **DATE:**

ANALYSIS OF RL & RC CIRCUITS FOR PULSE EXCITATION

AIM:- To draw the time response of first order R-L & R-C Networks for periodic non sinusoidal functions and determination of time constant.

APPARATUS:

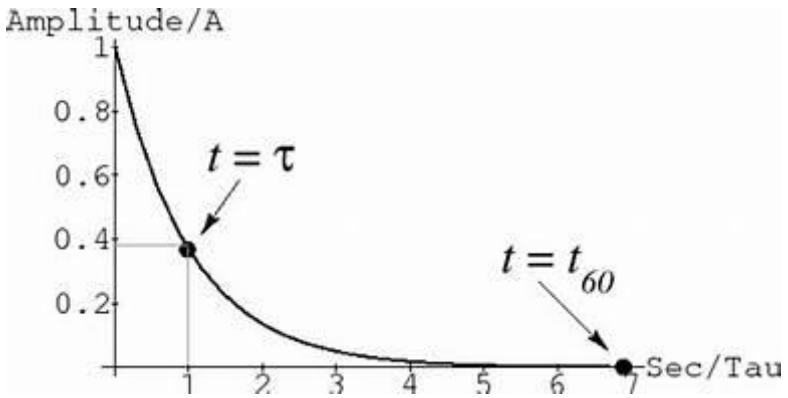
S.No.	Name of the equipment	Range	Type	Quantity
1.	Function Generator	(0-1)MHz	..	1
2	Bread Board	..	..	1
3	DRB	..	..	1
4	DLB	..	..	1
5	DCB	..	..	1
6	CRO	..	..	1
7	Connecting Wires	..	..	..

PROCEDURE:-

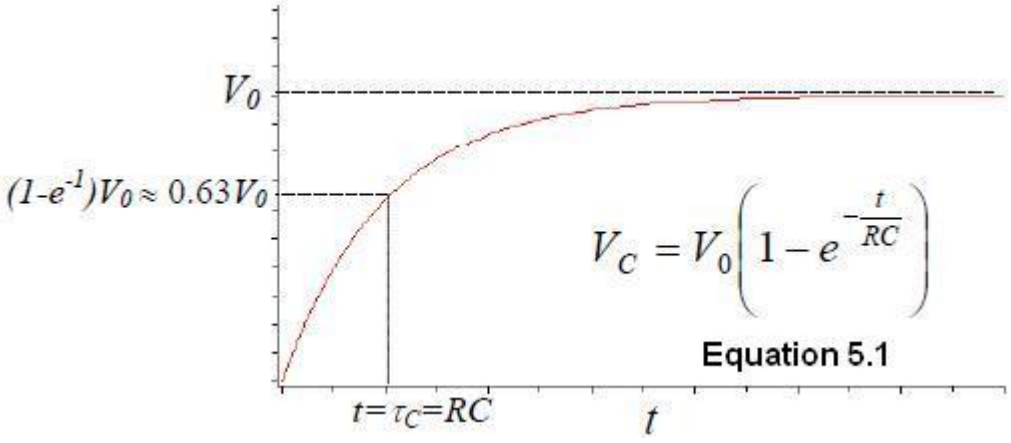
1. Make connections as per the circuit diagram.
2. Give 2V Peak to peak square wave supply through function generator with suitable frequency.
3. Take out put across inductor in RL Circuit, across capacitor in RC Circuits.
4. Calculate the time constant from CRO.
5. For deferent values of T and V Calculate corresponding (L/R) Values.
6. Compare the time constant theoretically and practically.

Model Waveform:

(a) For RL circuit:



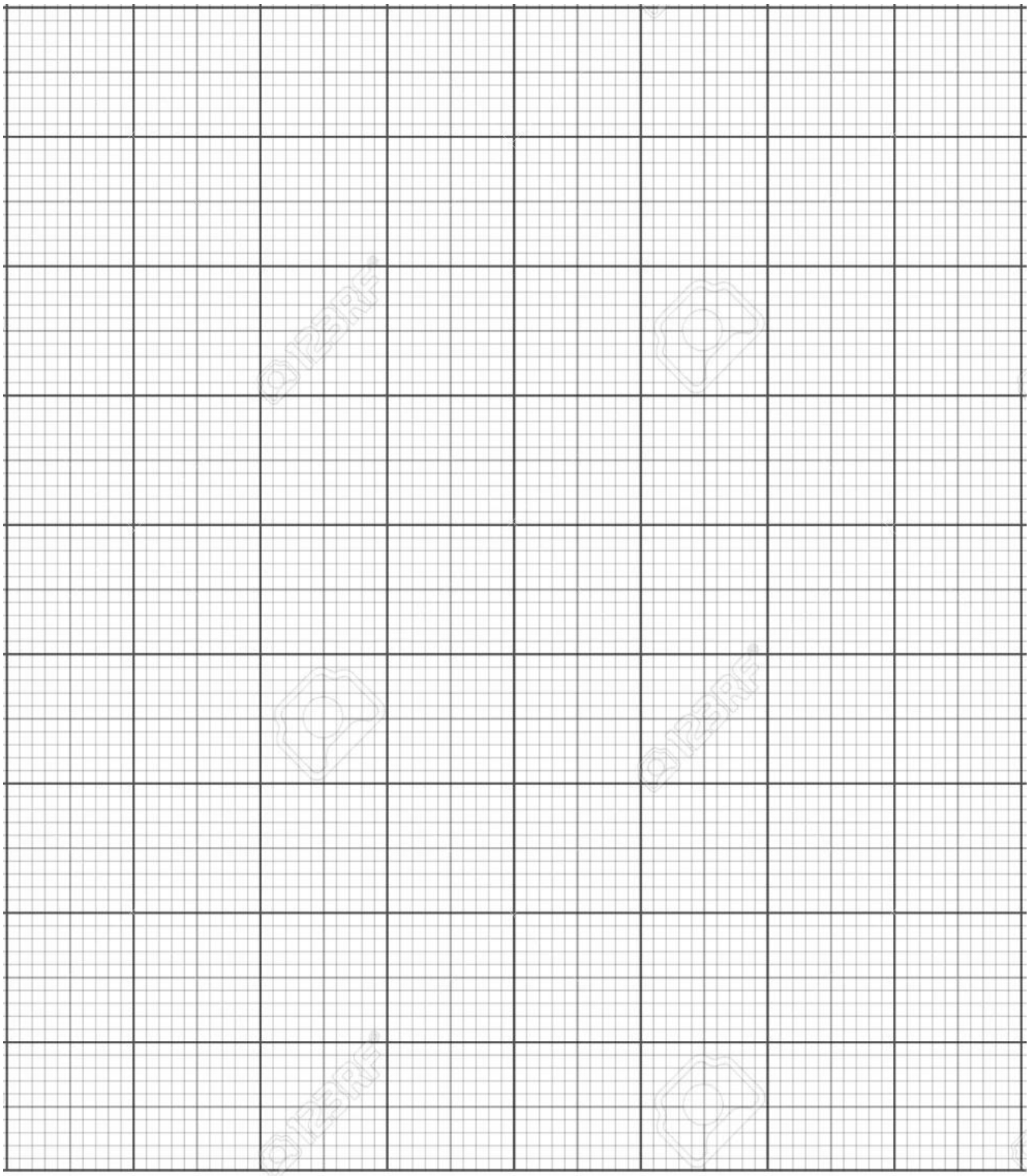
(b) For RC circuit:



OBSERVATIONS:-

Type of circuit	Voltage	Time period	Time constant Practical	Time constant theoretical

Theoretical Calculations:



Result:

VIVA QUESTIONS:-

1) Define impedance?

2) Define suseptance?

3) What is the Impedance of series RL circuit?

4) What is the Impedance of series RC circuit?

5) What is the Time constant of series RL circuit?

6) What is the Time constant of series RC circuit?

7) What happen if DC supply applied to inductor?

8) What happen if DC supply applied to capacitor?