DIGITAL LOGIC DESIGN LAB MANUAL

Department of Electronics & Communication Engineering

VEMU INSTITUTE OF TECHNOLOGY::P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

(Approved by AICTE, New Delhi & Affiliated to JNTUA, Anantapuramu)

DIGITAL LOGIC DESIGN LAB MANUAL

Name:____

H.T.No:____

Year/Semester:____

Department of Electronics & Communication Engineering

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VEMU Institute of Technology
Dept. of Electronics and Communication Engineering

Vision of the institute

To be one of the premier institutes for professional education producing dynamic and vibrant force of technocrats with competent skills, innovative ideas and leadership qualities to serve the society with ethical and benevolent approach.

Mission of the institute

Mission_1: To create a learning environment with state-of-the art infrastructure, well equipped laboratories, research facilities and qualified senior faculty to impart high quality technical education.
Mission_2: To facilitate the learners to inculcate competent research skills and innovative ideas by Industry-Institute Interaction.
Mission_3: To develop hard work, honesty, leadership qualities and sense of direction in learners by providing value based education.

Vision of the department

To develop as a center of excellence in the Electronics and Communication Engineering field and produce graduates with Technical Skills, Competency, Quality, and Professional Ethics to meet the challenges of the Industry and evolving Society.

Mission of the department

Mission_1: To enrich Technical Skills of students through Effective Teaching and Learning practices to exchange ideas and dissemination of knowledge.

Mission_2: To enable students to develop skill sets through adequate facilities, training on core and multidisciplinary technologies and Competency Enhancement Programs.

Mission_3: To provide training, instill creative thinking and research attitude to the students through Industry-Institute Interaction along with Professional Ethics and values.

Programme Educational Objectives (PEOs)

PEO 1: To prepare the graduates to be able to plan, analyze and provide innovative ideas to investigate complex engineering problems of industry in the field of Electronics and Communication Engineering using contemporary design and simulation tools.

PEO-2: To provide students with solid fundamentals in core and multidisciplinary domain for successful implementation of engineering products and also to pursue higher studies.

PEO-3: To inculcate learners with professional and ethical attitude, effective communication skills, teamwork skills, and an ability to relate engineering issues to broader social context at work place

Programme Outcomes(Pos)

PO_1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO_2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO_3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO_4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO_5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO_6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO_7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO_8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO_9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO_10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO_11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO_12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Programme Specific Outcome(PSOs)

PSO_1	**Higher Education :** Qualify in competitive examination for pursuing higher education by applying the fundamental concepts of Electronics and Communication Engineering domains such as Analog & Digital Electronics, Signal Processing, Communication & Networking, Embeded Systems, VLSI Design and Control systems etc.,
PSO_2	**Employment**: Get employed in allied industries through their proficiency in program specific domain knowledge, Specalized software packages and Computer programming or became an entrepreneur.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

II B.Tech. II-Sem (ECE)

(20A04303P) DIGITAL LOGIC DESIGN LABORATORY

COURSE OUTCOMES(COS)

CO1	Understand the pin configuration of various digital ICs used in the lab
CO2	Conduct the experiment and verify the properties of various logic circuits.
CO3	Analyze the sequential and combinational circuits.
CO4	Design of any sequential/combinational circuit using Hardware

PART A:

LIST OF EXPERIMENTS:

1. Verification of truth tables of the following Logic gates
   Two input (i) OR (ii) AND (iii) NOR (iv) NAND (v) Exclusive-OR (vi) Exclusive-NOR
2. Design a simple combinational circuit with four variables and obtain minimal expression and verify the truth table using Digital Trainer Kit.
3. Verification of functional table of 3 to 8-line Decoder /De-multiplexer.
4. 4variable logic function verification using 8 to1 multiplexer.
5. Design full adder circuit and verify its functional table.
6. Verification of functional tables of (i) JK Edge triggered Flip–Flop (ii) JK Master Slav Flip–Flop (iii) D Flip-Flop
7. Design a four-bit ring counter using D Flip–Flops/JK Flip Flop and verify output
8. Design a four bit Johnson’s counter using D Flip-Flops/JK Flip Flops and verify output
9. Verify the operation of 4-bit Universal Shift Register for different Modes of operation.
10. Draw the circuit diagram of MOD-8 ripple counter and construct a circuit using T-Flip-Flops and Test It with a low frequency clock and sketch the output waveforms.
11. Design MOD–8 synchronous counter using T Flip-Flop and verify the result and sketch the output waveforms.
12. (a) Draw the circuit diagram of a single bit comparator and test the output
    (b) Construct 7 Segment Display Circuit Using Decoder and7 Segment LED and test it.

(20A04303P) DIGITAL LOGIC DESIGN II B.Tech-II SEM

LIST OF EXPERIMENTS TO BE CONDUCTED

HARDWARE EXPERIMENTS

1. Logic Gates.
2. Design of combinational circuits with four variables.
3. 3 to 8-line Decoder /De-multiplexer.
4. 8 to1 multiplexer.
5. Full adder.
6. Functional tables of (i) JK Edge triggered Flip–Flop (ii) JK Master Slav Flip–Flop (iii) D Flip-Flop.
7. Four-bit ring counter using D Flip–Flops/JK Flip Flop.
8. Four bit Johnson's counter using D Flip-Flops/JK Flip Flops.
9. 4-bit Universal Shift Register.
10. MOD-8 ripple counter using T-Flip-Flops.
11. MOD–8 synchronous counter using T Flip-Flop.

12a. single bit comparator

12b. 7 Segment Display Circuit Using Decoder and7 Segment LED

ADDITIONAL EXPERIMENTS:

1. BCD Adder Circuit.
2. 74154 De-Multiplexer using LEDs for outputs.

CONTENTS

DOS & DONTS IN LABORATORY

DO's

1. Students should be punctual and regular to the laboratory.
2. Students should come to the lab in-time with proper dress code.
3. Students should maintain discipline all the time and obey the instructions.
4. Students should carry observation and record completed in all aspects.
5. Students should be at their concerned experiment table, unnecessary moment is restricted.
6. Students should follow the indent procedure to receive and deposit the components from lab technician.
7. While doing the experiments any failure/malfunction must be reported to the faculty.
8. Students should check the connections of circuit properly before switch ON the power supply.
9. Students should verify the reading with the help of the lab instructor after completion of experiment.
10. Students must endure that all switches are in the lab OFF position, all the connections are removed.
11. At the end of practical class the apparatus should be returned to the lab technician and take back the indent slip.
12. After completing your lab session SHUTDOWN the systems, TURNOFF the power switches and arrange the chairs properly.
13. Each experiment should be written in the record note book only after getting signature from the lab in charge in the observation notebook.

DON'Ts

1. Don't eat and drink in the laboratory.
2. Don't touch electric wires.
3. Don't turn ON the circuit unless it is completed.
4. Avoid making loose connections.
5. Don't leave the lab without permission.
6. Don't bring mobiles into laboratory.
7. Do not open any irrelevant sites on computer.
8. Don't use a flash drive on computers.

SCHEME OF EVALUATION

S.No	Program	Date	Marks Awarded				Total 30(M)
			Record (10M)	Obs. (10M)	Viva (5M)	Attd. (5M)	
1	Logic Gates.						
2	Design of combinational circuits with four variables.						
3	3 to 8-line Decoder /De-multiplexer.						
4	8 to1 multiplexer.						
5	Full adder.						
6	Functional tables of (i) JK Edge triggered Flip–Flop (ii) JK Master Slav Flip–Flop (iii) D Flip-Flop.						
7	Four-bit ring counter using D Flip–Flops/JK Flip Flop.						
8	Four bit Johnson's counter using D Flip-Flops/JK Flip Flops.						
9	4-bit Universal Shift Register.						
10	MOD-8 ripple counter using T-Flip-Flops.						
11	MOD–8 synchronous counter using T Flip-Flop.						
12	A. single bit comparator B.7 Segment Display Circuit Using Decoder and7 Segment LED						
ADDITIONAL EXPERIMENTS							
1	BCD Adder Circuit.						
2	74154 De-Multiplexer using LEDs for outputs.						

Signature of Lab In-charge

INTRODUCTION

Digital IC Trainer KIT Operation (Model No: 9002):

Specification : Digital IC Trainer KIT Operation (Model No: 9002) Specification : Digital IC Trainer Kit Model No. 9002 is available with 10 nos. of TTL compatible logic level inputs, TTL logic selectable by a toggle switch, Logic HIGH and logic LOW are displayed by LED, 10 nos of Logic Output indictors, Four crystal generated clock output of 1KHz, 100Hz, 10Hz and 1Hz. Facility for single pulse generation by a push button switch, Logic probe to check logic LOW, logic HIGH and pulse, Four seven segment displays with BCD inputs, Sockets onboard to fix the IC`s : 16pin-4nos. Built-in Power supply : 5V, 1Amp, +12V, 250mA

How to use the IC Trainer Kit? Connect the 230 volts AC power supply and switch ‘ON’ the Toggle switch ‘ON’ the left side of the Top Panel, LED will glow. Digital IC Trainer Kit is ready for use. Select the TTL IC to be used for the experiment. Insert the IC properly in the breadboard/ZIF socket (lock the ZIF by moving lever upwards), Know the biasing voltage required for different families of IC’s and connect power supply voltage and ground terminals to the respective pins of the IC. Inputs such as logic clock, of different frequency, monopulse, logic levels, BCD inputs, can be selected from the patch panel.

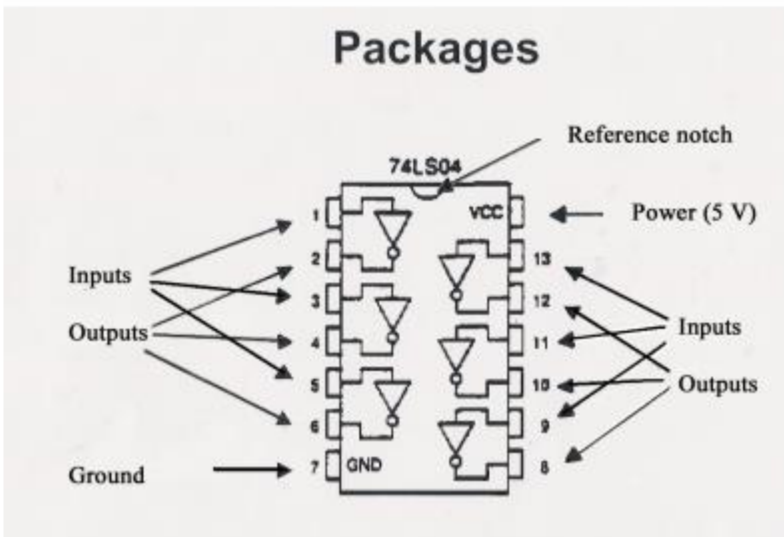
Outputs such as LED indicator, seven segment digital display can be selected depending upon the requirement. Connect the pin connection of IC using wires as per the logic diagram, after verifying connection switch on the supply of IC Trainer Kit and verify the operation the circuit with the help of truth table.

Guide to Assembling your Circuits.

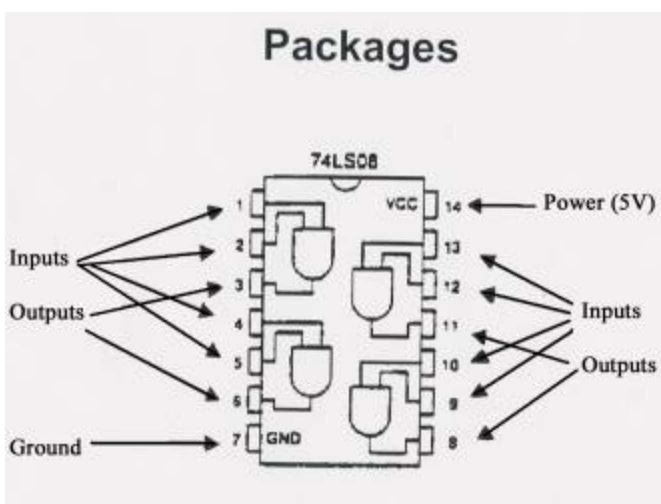
In this section we describe the use of the breadboard and give basic hints about the wiring process needed to power up and interconnect your circuits. Assembling circuits on your breadboard is a fast and easy process once you get used to it. To assemble your circuit first select the chips that you need, insert them in the breadboard, wire up the power and ground connections as described in the next section and next wire the logic elements according to the circuit connections that you obtained from the design process. Before you insert a chip into the breadboard, make sure it is properly oriented (see Figures), and that when you press it down the pins of the chip actually enter the holes and do not bend underneath the chip package. When wiring, be careful to hit the right hole needed in the connection, because this is one of the most common mistakes found to cause an error in your projects.

The chips or packages that will be used to build the experiments belong to the TTL logic family, and they are referred as the 74LSXX family, where the XX is a number that indicates the specific kind of gate or function. The main characteristics for some typical logic gates packages are shown in Figures

TTL Packages Description:



Inverter (NOT) gate pin distribution



AND gate pin distribution

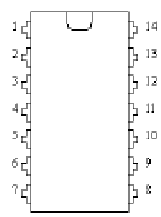
Logic Gates

Digital logic devices are the circuits that electronically perform logic operations on binary variables. binary information is represented by high and low voltage levels, which the device processes electronically. The devices that perform the simplest of the logic operations (such as AND, OR, NAND,etc.) are called gates. For example, an AND gate electronically computes the AND of the voltage encoded binary signals appearing at its inputs and presents the voltage encoded result at its output.

The digital logic circuits used in this laboratory are contained in integrated circuit (IC) packages, with generally 14 or 16 pins for electrical connections. Each IC is labeled (usually with an 74LSxx number) to identify the logic it performs. The logic diagrams and pin connections for these IC's are described in the TTL Data Book by Texas Instruments1.

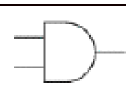
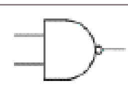
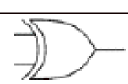
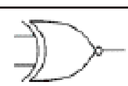
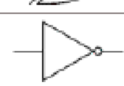
The transistor-transistor logic(TTL) IC's used in this laboratory require a 5.0 volt power supply for operation. TTL inputs require a voltage greater than 2 volts to represent a binary 1 and a voltage less than 0.8 volts to represent a binary 0.

Pin numbering is standard on IC's. Figure 1-1 illustrates the pin numbering for a 14-pin dual in-line package (DIP). With the IC oriented as shown, the numbering starts at the top left and proceeds counterclockwise around the chip:



To construct circuits with IC's, a circuit board that allows easy connections to IC pins should be used. The circuit board contains rows of solder less tie points, a 5-volt power supply, a common circuit point (ground), toggle switches for input, and LEDs (light emitting diodes) for output.

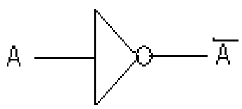
LOGIC GATES AND THEIR PROPERTIES

Name	Symbol	Description
AND gate		Output is 1 only if all the inputs are 1. AND gates can have two, three, or more inputs.
NAND gate		"NOT-AND gate"--opposite of AND gate--output is 1 only if all the inputs are NOT 1. Output is only 0 when all the inputs are 1. NAND gates can have more than two inputs.
OR gate		Output is 1 if either of the inputs are 1. Output is only 0 if both of the inputs are 0. OR gates can have more than two inputs.
NOR gate		"NOT-OR gate"--opposite of OR gate--output is only 1 if both of the inputs are 0. If either of the inputs, or both the inputs, are 1, then the output is 0. NOR gates can have more than two inputs.
EX-OR gate		"Exclusive-OR gate"--output is only 1 if either of the inputs are 1, but 0 when both the inputs are 0 or when both the inputs are 1.
EX-NOR gate		"Exclusive-NOR gate"--opposite of EX-OR gate--output is only 1 when both the inputs are 0 or both the inputs are 1. Output is 0 when either of the inputs is 1.
NOT gate		Also known as INVERTER gate.

LOGIC DIAGRAMS:

NOT GATE

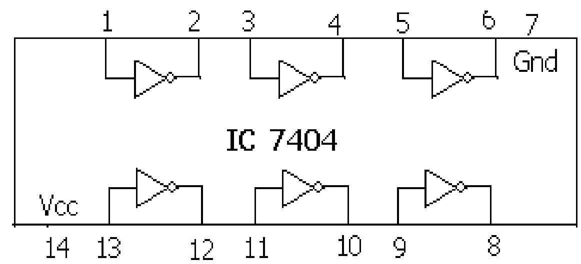
SYMBOL



TRUTH TABLE

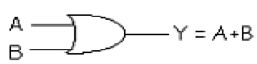
Dec	I/P (A)	O/P $(\overline{A})$
0	0	1
1	1	0

IC 7404



OR GATE

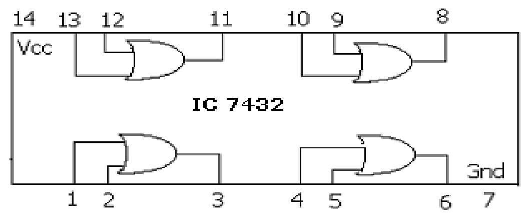
SYMBOL



TRUTH TABLE

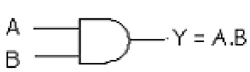
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	1

IC 7432



AND GATE

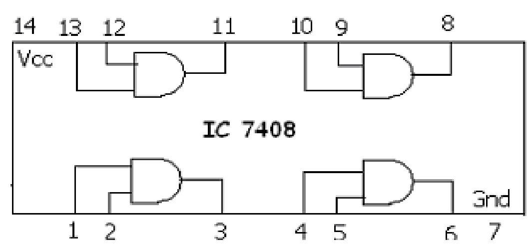
SYMBOL



TRUTH TABLE

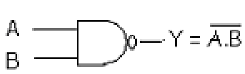
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	0
2	1	0	0
3	1	1	1

IC 7408



NAND GATE

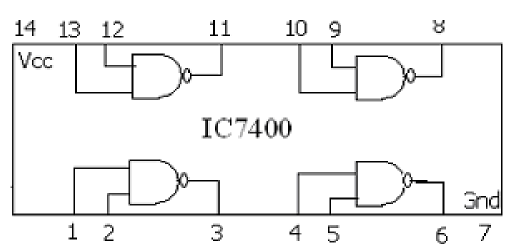
SYMBOL



TRUTH TABLE

Dec Eq	Inputs		Output
	A	B	Y
0	0	0	1
1	0	1	1
2	1	0	1
3	1	1	0

IC 7400



EXP.NO:01 **DATE:**

LOGIC GATES

AIM: Verification of Truth Table for AND, OR, NOT, NAND, NOR and EX-OR gates.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	74LS08,74LS32,74LS04 74LS00,74LS02,74LS86, 74LS266	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

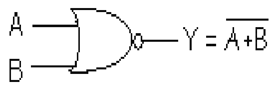
The basic logic gates are the building blocks of more complex logic circuits. These logic gates perform the basic Boolean functions, such as AND, OR, NAND, NOR, Inversion, Exclusive-OR, Exclusive-NOR. Fig. below shows the circuit symbol, Boolean function, and truth. It is seen from the Fig that each gate has one or two binary inputs, A and B, and one binary output, C. The small circle on the output of the circuit symbols designates the logic complement. The AND, OR, NAND, and NOR gates can be extended to have more than two inputs. A gate can be extended to have multiple inputs if the binary operation it represents is commutative and associative.

PROCEDURE:

1. Do the Connections as per symbol and indent marked on PCB.
2. Give the logic input to the gate under test as per symbol from INPUT
3. SWITCHES section.
4. Connect output of gate under test to any of the led from OUTPUT LED section
5. Observe the output on LEDS from OUTPUT SECTION and verify the truth table.

NOR GATE

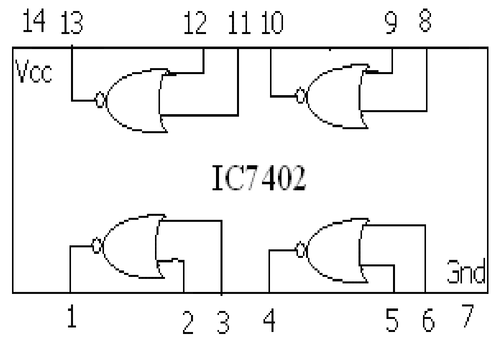
SYMBOL



TRUTH TABLE

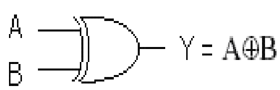
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	1
1	0	1	0
2	1	0	0
3	1	1	0

IC7402



EX-OR GATE

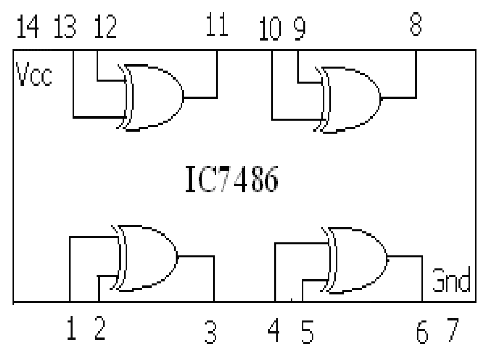
SYMBOL



TRUTH TABLE

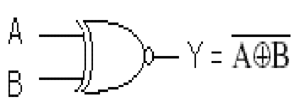
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

IC- 7486



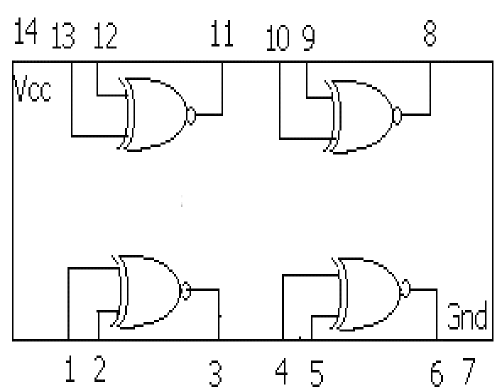
EX-NOR GATE

SYMBOL



TRUTH TABLE

Dec Eq	Inputs		Output
	A	B	Y
0	0	0	1
1	0	1	0
2	1	0	0
3	1	1	1



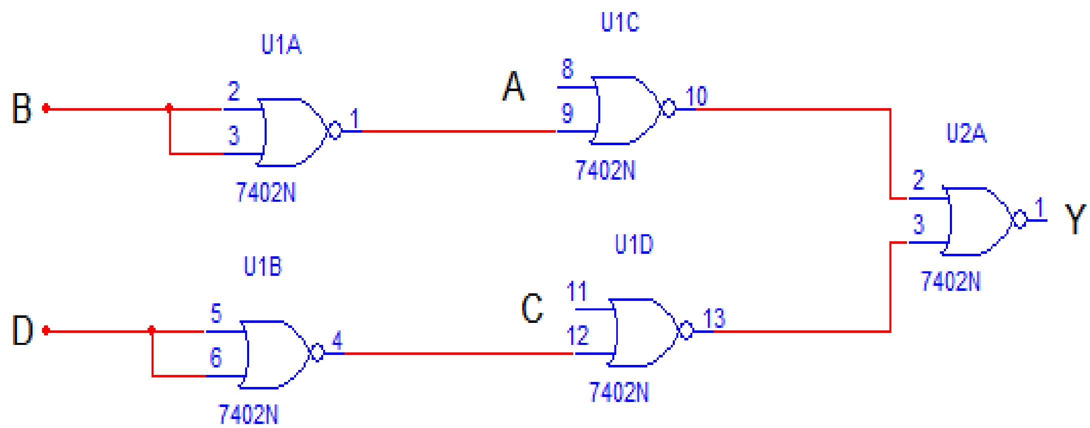
RESULT:

CONCLUSION:

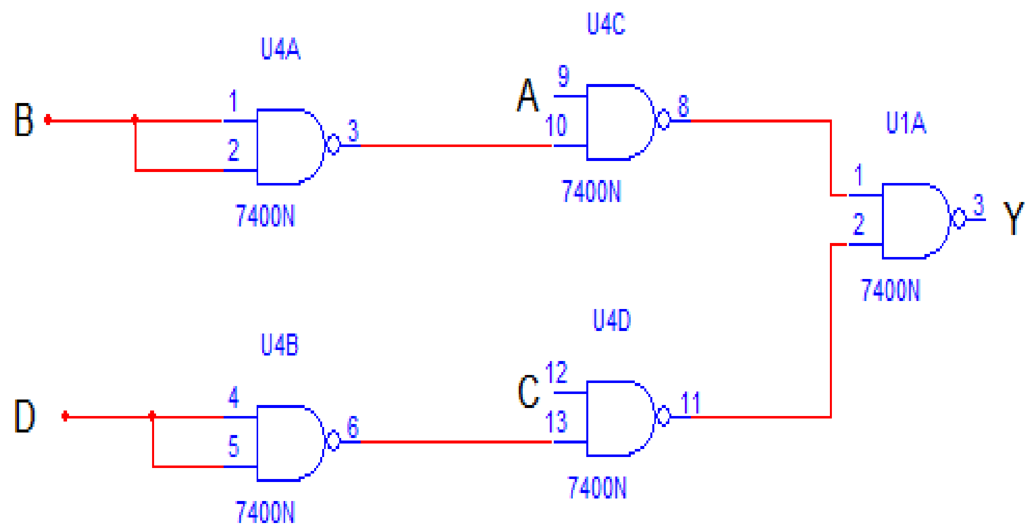
VIVA QUESTIONS:

1. Why NAND & NOR gates are called universal gates?
2. Realize the EX – OR gates using minimum number of NAND gates?
3. Give the truth table for EX-NOR and realize using NAND gates?
4. What is the principle of logic gates?
5. Which is the most commonly used logic family?

REALIZATION USING NOR GATES:



REALIZATION USING NAND GATES:



EXP NO:02 **DATE:**

COMBINATIONAL CIRCUIT

AIM:-To implement and verification of four variables logic functional truth table using basic gates and universal gates.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	74LS08,74LS32,74LS04, 74LS00,74LS02	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

Canonical Forms (Normal Forms): Any Boolean function can be written in Disjunctive normal form (sum of min-terms) or conjunctive normal form (product of maxterms). A Boolean function can be represented by a Karnaugh map in which each cell corresponds to a minterm. The cells are arranged in such a way that any two immediately adjacent cells correspond to two minterms of distance 1. There is more than one way to construct a map with this property.

PROCEDURE:

1. Do the connection as per block diagram shown below and switch ON the power supply
2. Provide the input data via the input switches and observe the output on output LEDs Verify the Truth Table

Karnaugh Maps

For a function of two variables, say, f(x, y),

	x'	x
y'	f(0,0)	f(1,0)
y	f(0,1)	f(1,1)

For a function of three variables, say, f(x, y, z)

	x'y'	x'y	xy	xy'
z'	f(0,0,0)	f(0,1,0)	f(1,1,0)	f(1,0,0)
z	f(0,0,1)	f(0,1,1)	f(1,1,1)	f(1,0,1)

For a function of four variables: f(w, x, y, z)

For the given Truth, Table,realize a logical circuit using NOR and NAND gates

	w'x'	w'x	wx	wx'
y'z'	0	4	12	8
y'z	1	5	13	9
yz	3	7	15	11
yz'	2	6	14	10

Realization of Boolean expression:

1) $Y= \bar{A}\bar{B}C\bar{D}+\bar{A}BC\bar{D}+ABC\bar{D}+A\bar{B}C\bar{D}+A\bar{B}\bar{C}\bar{D}+A\bar{B}\bar{C}D+A\bar{B}CD$

AB

			1
			1
			1
1	1	1	1

After simplifying using K-Map method we get $Y = A\bar{B} + C\bar{D}$

TRUTH TABLES:

NOR gates

Inputs				Output
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

NAND gates

TRUTH TABLE

INPUTS				OUTPUT
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What are the different methods to obtain minimal expression?

2. What is a Min term and Max term?

3. State the difference between SOP and POS?

4. How do you realize a given function using multiplexer?

5. What is a multiplexer?

EXP. NO:03 **DATE:**

DE-MULTIPLEXER

AIM:-Verification of functional table of De-multiplexer.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	74LS138	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

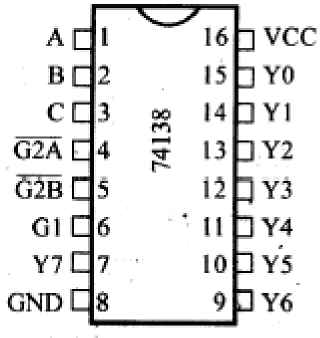
THEORY DECODER:

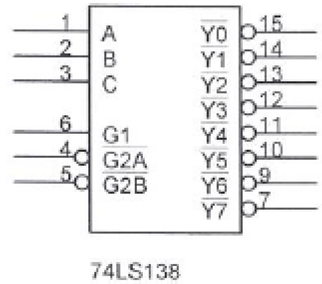
A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-2^n, binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. In case of decoding all combinations of three bits eight (2^3=8) decoding gates are required. This type of decoder is called 3-8 decoder because 3 inputs and 8 outputs. For any input combination decoder outputs are 1.

Procedure:

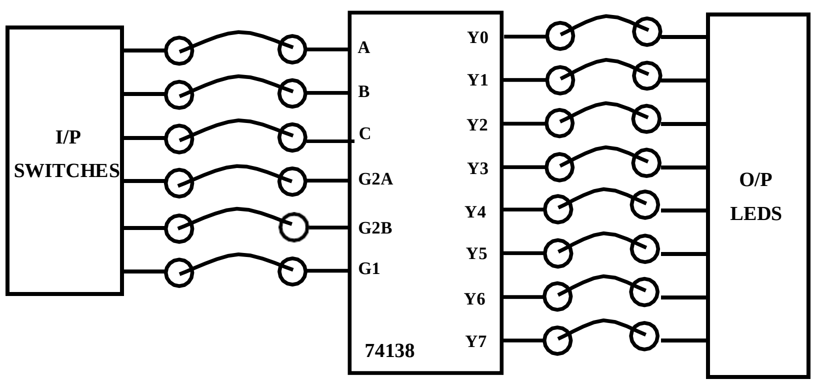
1. The truth table and a design of 3:8 decoder are given.
2. Realize this circuit on your board by using logic circuit.
3. Connect threeinputs x,y,z to the switches & eight outputs vice-versa.
4. Connect the functions outputs to LEDs.
5. Verify input/output relation (Truth table) of this converter.

Pin Description **IC74138 Circuit connection**





BLOCK DIAGRAM 3:8 DEMUX:



TRUTH TABLE FOR DEMUX:

DM74LS138

Inputs					Outputs							
Enable		Select										
G1	G2 (Note 1)	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

NOTE1: G2=G2A and G2B

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer.

In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND +9gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

PROCEDURE:

1. Do the connection as per block diagram shown below and switch ON the power supply.
2. Apply proper logic inputs o the Demultiplexer and observe the output on LEDs.
3. Verify the function table of Demultiplexer.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vcc and ground should be applied carefully at the specified pin only.

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What do you understand by decoder?

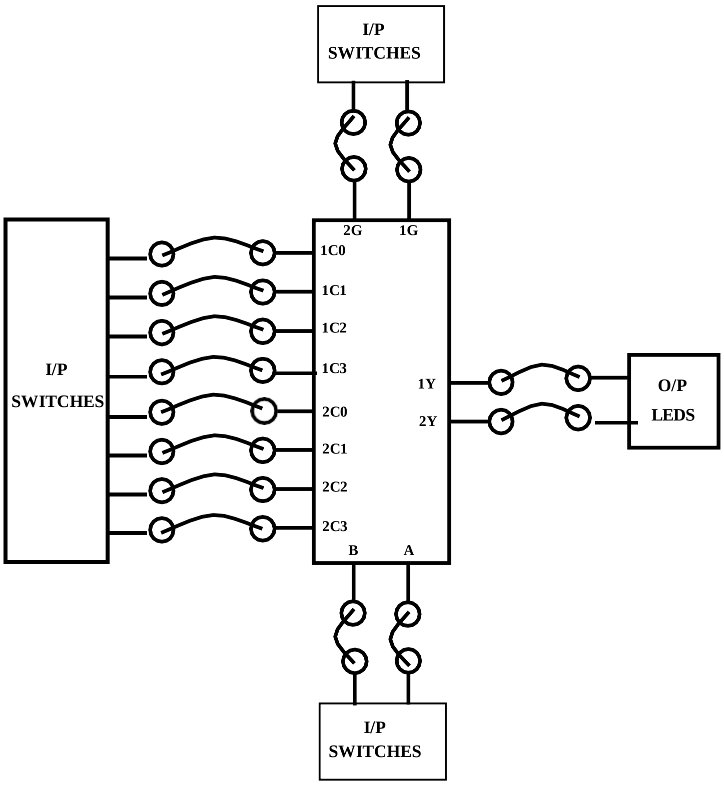
2. What is demultiplexer?

3. What do you understand by encoder?

4. What is the main difference between decoder and demultiplexer?

5. Why Binary is different from Gray code?

BLOCK DIAGRAM OF 8:1 MUX :



FUNCTION TABLE

Select I/p		STROBE		DATA INPUTS				OUTPIT	
B	**A**	**2G**	**1G**	**1C3**	**1C2**	**1C1**	**1C0**	**2Y**	**1Y**
X	X	H	H	X	X	X	X	L	L
CASE 1									
L	L	H	L	L	L	L	**H**	L	**H**
L	H	H	L	L	L	**L**	H	L	**L**
H	L	H	L	L	**H**	L	L	L	**H**
H	H	H	L	**H**	L	L	L	L	**H**
CASE 2									
B	**A**	**2G**	**1G**	**2C3**	**2C2**	**2C1**	**2C0**	**2Y**	**1Y**
L	L	L	H	H	H	H	**L**	**L**	L
L	H	L	H	H	H	**H**	L	**H**	L
H	L	L	H	L	**H**	L	L	**H**	L
H	H	L	H	**L**	L	L	L	**L**	L

X = don’t care condition.

EXP NO:04 **DATE:**

8:1 MULTIPLEXER

AIM: To verify the Functional Table using 8:1multiplexer.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC 74153	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

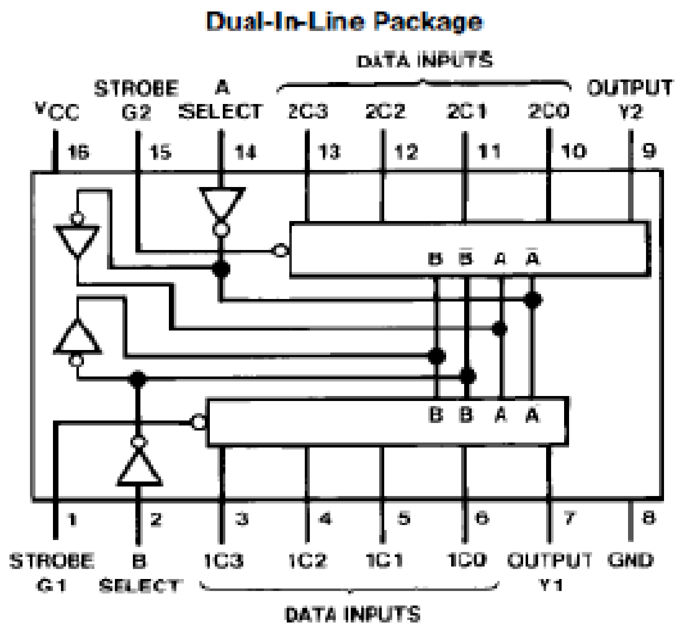
THEORY:

The Multiplexers or data selector is a logic circuit that selects one out of several inputs to a single output. The input selected is controlled by a set of select lines. For selecting one output line from n-input lines, a set of m-select lines is required. The relationship between the number of input lines and the select lines is given by $2^m = n$.

PROCEDURE:

1. Do the connection as per block diagram shown below and switch ON the power supply.
2. Apply proper logic inputs o the Multiplexer and observe the output on LEDs.
3. Verify the function table of multiplexer in both the cases.

Internal Block Diagram OF 74153:



RESULT :

CONCLUSION:

VIVA QUESTIONS:

1. What is a multiplexer?

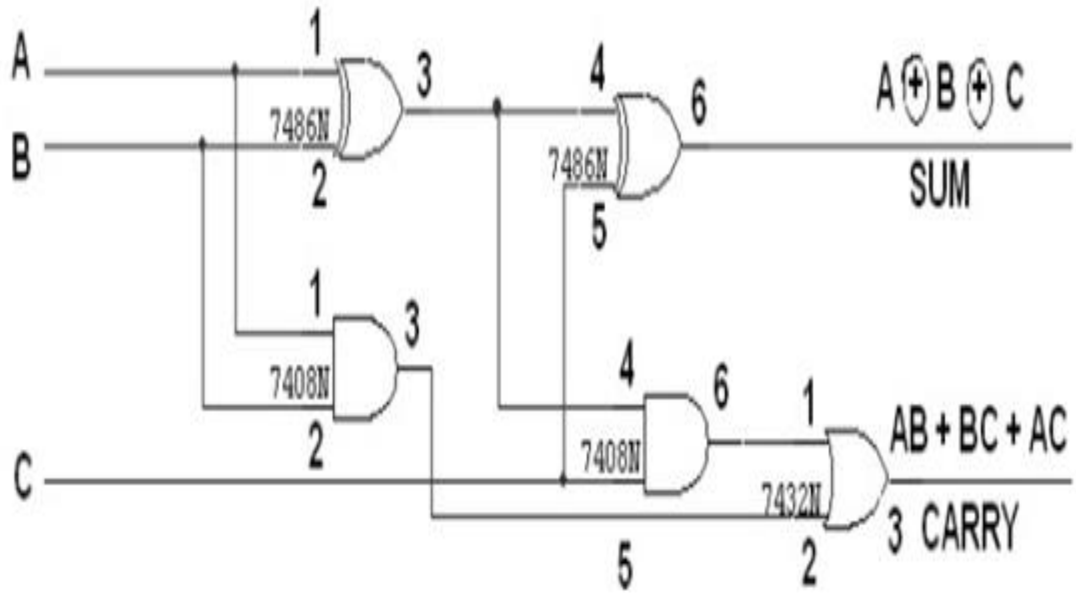
2. What are the applications of multiplexer and de-multiplexer?

3. What is a de-multiplexer?

4. In 2n to 1 multiplexer how many selection lines are there?

5. Implement an 8:1 mux using 4:1 muxes?

BLOCK DIAGRAM OF FULLADDER:



TRUTH TABLE

X	Y	Z	Sum (S)	Carry (C)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Exp No:05 **Date:**

FULL ADDER

AIM: To verify the truth tables of Full Adder.

APPARATUS REQUIRED:

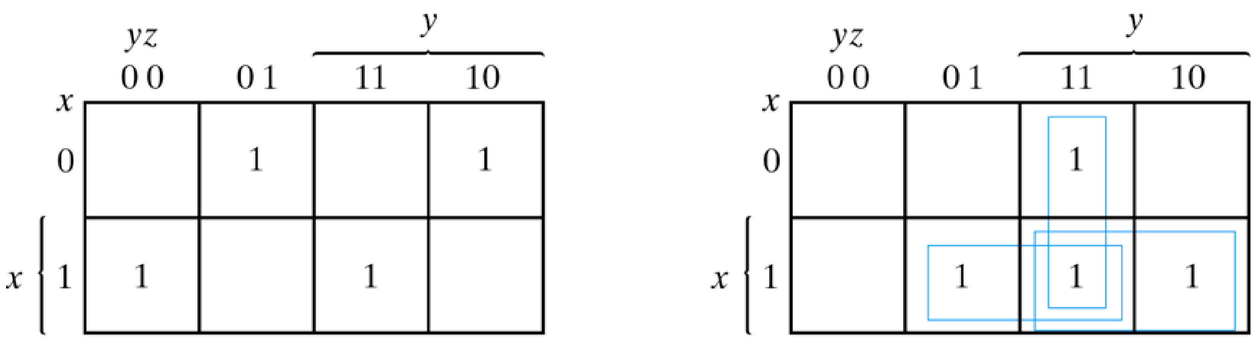
S.NO	APPARATUS	RANGE	QUANTITY
1	IC's	74LS08, 74LS32, 74LS04, 74LS00, 74LS02, 74LS86	1
2	Patch Chords		REQUIRED
3	Fixed Power Supply	(0-5V)	1
4	Digital IC Trainer Kit		1

THEORY:

Full adder

A Full adder is a combinational circuit that performs addition of three input bits. Half adder has inputs X, Y, Z and outputs sum (S) and carry(C).

The simplified Boolean expressions are

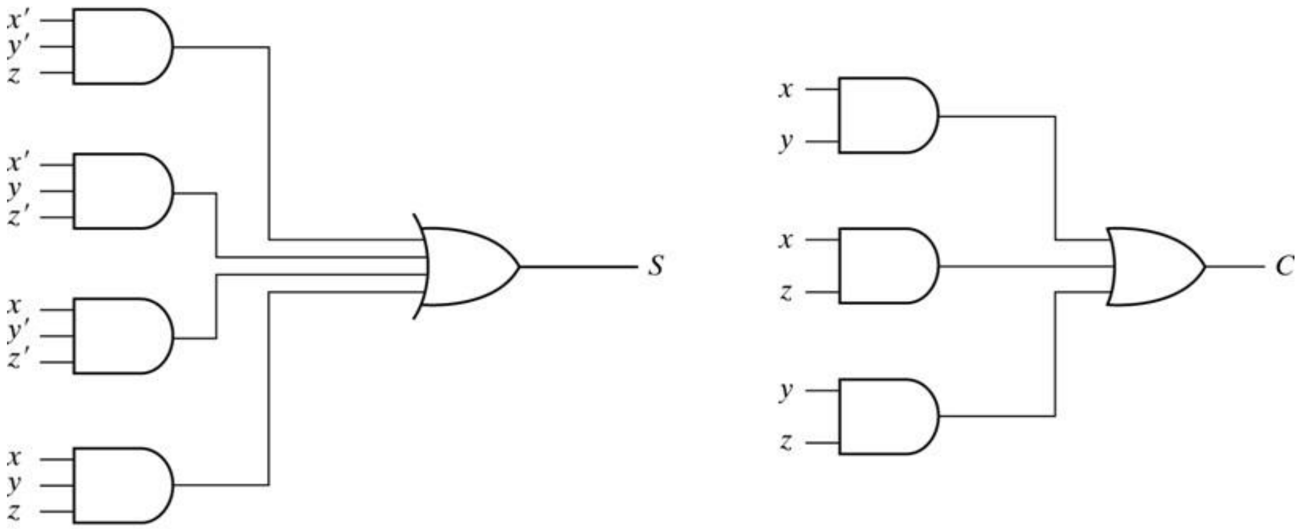


$$S = x'y'z + x'yz' + xy'z' + xyz$$

$$\begin{aligned} C &= xy + xz + yz \\ &= xy + xy'z + x'yz \end{aligned}$$

Maps for Full Adder

The logic circuit to implement is as shown below



Implementation of Full Adder in Sum of Products

FULL ADDER USING TWO HALF ADDERS AND OR GATE

A full adder can also be implemented using two half adders and one OR gate as shown in fig.The sum output from second half adder is

S=x EXOR y EXOR z S=x’y’z’+x’yz’+xy’z’+xyz

C=xy+yz+xz

PROCEDURE:

1. Connect A, B and C I/P of Full adder to switches from input switches section.
2. Connect SUM & CARRY O/P of Full Adder to LEDs from O/P LED section.
3. Switch ON the power supply of the Kit.
4. Provide proper inputs to Full adder using switches as per truth table of Full adder shown above.
5. Observe the O/P of Full Adder on LEDs.
6. Verify the functionality of Full Adder as per truth table & Note it down.

RESULT:

CONCLUSION

VIVA QUESTIONS:

1. What is use of Full adder?

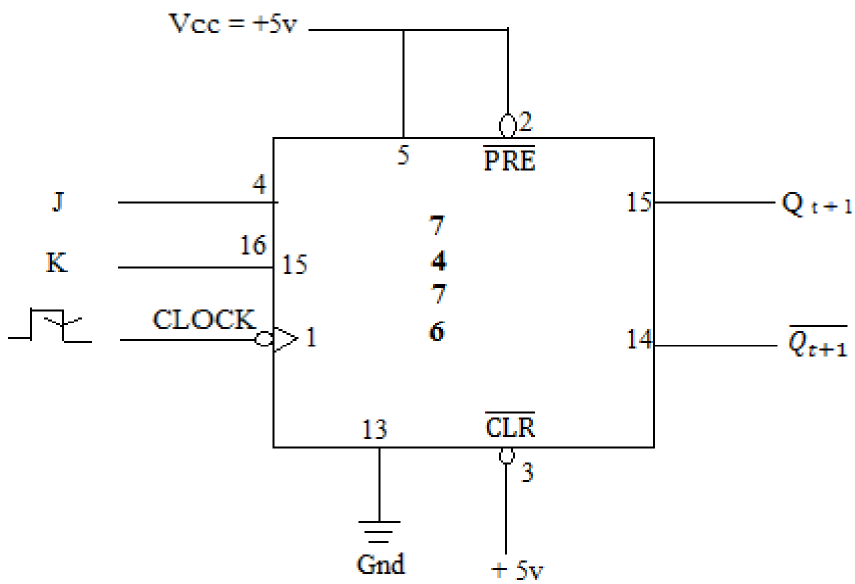
2. What is difference between the half and full adder?

3. How many half adders required to make a full adder?

4. In full adder how many types of gates are required?

5. Draw full adder circuit?

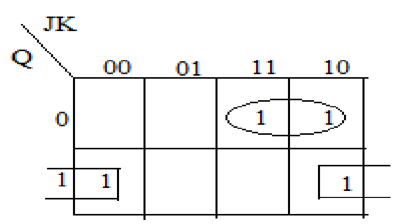
BLOCK DIAGRAM OF JK FLIP -FLOP:



Where

Q ⟶ Present State

Q_{t+1} ⟶ Next State



Characteristic eqn $Q_{t+1} = J Q + K Q$

i) Implementation of JK Flip-FlopDesign:

IC – 74LS76: Dual –ve edge triggered JK Flip-Flop

Inputs			Outputs
Q	J	K	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Truth Table of JK Flip – Flop

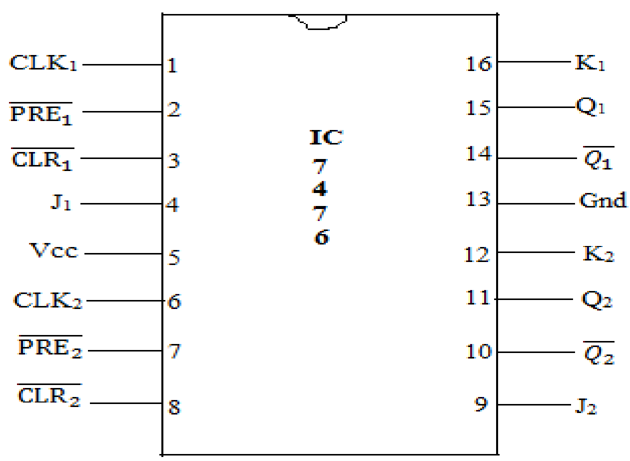


Fig: Pin diagram of 7476

Exp No: 06 **Date:**

JK & D FLIP-FLOP

AIM: Verification of functional tables of (i) JK Edge triggered Flip–Flop (ii) JK Master Slav Flip–Flop (iii) D Flip-Flop

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC 7476,74107,7474	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

Basically Flip-Flops are the bistable multivibrators that stores logic 1 and logic 0.Shift registers, memory, and counters are built by using Flip – Flops. Any complex sequential machines are build using Flip – Flops. Sequential circuit (machine) output depends on the present state and input applied at that instant.

Mealy Machine is one whose output depends on both the present state and the input. Moore machines one whose output depends only on the present state of the sequential circuit. Note that the truth table of J – K Flip – Flop is same as the Master – Slave.

J – K Flip Flop and they must be remain same because IC – 7476is –ve edge trigged flip – flop and we know that race around condition is eliminated by edge triggered flip – flop. Another way of eliminating race around condition is by using Master – Slave J –K Flip – Flop. When J = K = 1 (logic HIGH), J – K Flip – Flop changes output many times for single clock pulse, it is Smaller than width of the clock pulse.

ii) Master Slave JK Flip – Flop:

IC – 74107: Dual – Master – Slave JK Flip-Flop

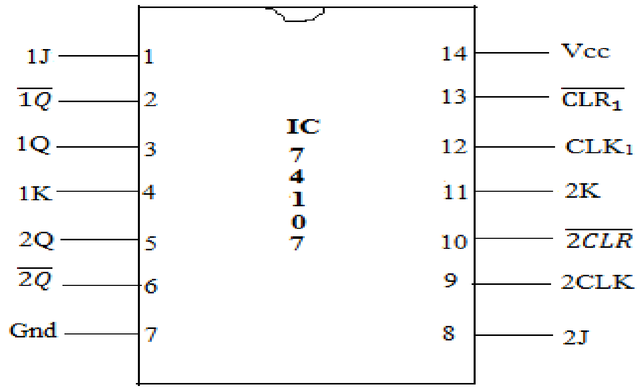
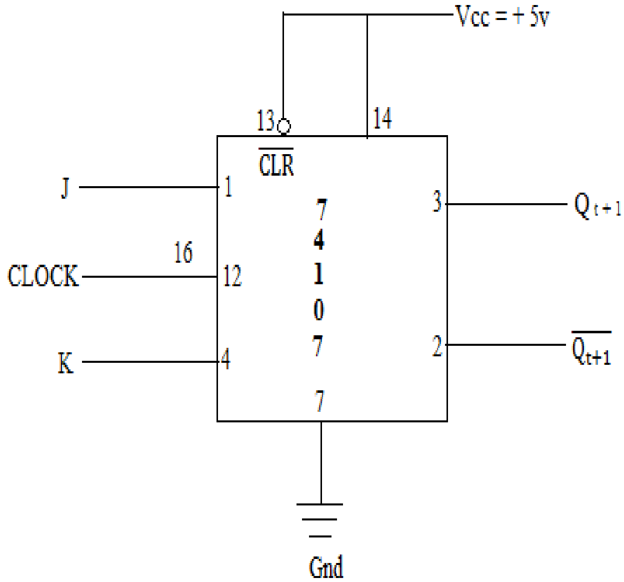


FIG: PIN DIAGRAM

BLOCK IMPLEMENTATION:



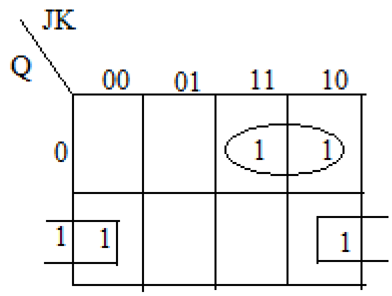
Truth Table of Master – Slave – JK Flip – Flop:

Where

Q ⟶ Present State

Q_{t+1} ⟶ Next State

Inputs			Outputs
Q	J	K	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



Characteristic eqn $Q_{t+1} = J\ Q + K\ Q$

PROCEDURE:

JK FLIP_FLOP:

1. Connect PR to **PRESET**, CR to **CLEAR** and J and K terminals to the logic input switches.
2. Connect CLK of JK flip-flop to Clock terminal.
3. Connect Q and /Q terminals to LED indicators in O/P section.
4. Set the PR, CR, CLK, J and K Signals by means of the switches as per the truth table of JK flip-flop given above and verify the Q and /Q outputs by changing possible input condition.

MASTER SLAVE J-K FLIP-FLOP:

1. Do the connection for MS JK Flip-Flop as shown in Fig.7(c) above.
2. Connect PR to **PRESET**, CR to **CLEAR** of both the flip-flops and J and K terminals of master flip-flop to the logic input switches.
3. Connect CLK of master JK flip-flop to Clock terminal.
4. Connect Q and /Q terminals of slave flip-flop to LED indicators in O/P LED section. Also connect Q & /Q terminals of master flip-flop to the LEDs in O/P LED section.
5. Set the PR, CR, clk, J and K Signals by means of the switches as per the truth table of MS JK flip-flop given above and verify the Q and /Q outputs.

D FLIP-FLOP:

1. Connect PR to **PRESET**, CR to **CLEAR** and D terminals to the logic input switch.
2. Connect the CLK of D Flip-Flop to CLOCK terminal.
3. Connect Q and /Q terminals to LED indicators in O/P LED section.
4. Set the PR, CR, CLK and D Signals by means of the switches as per the truth table of D flip-flop given above and verify the Q and /Q outputs.

iii) D Flip – Flop:

IC – 7474: Dual + ve edge triggered D Flip-Flop:

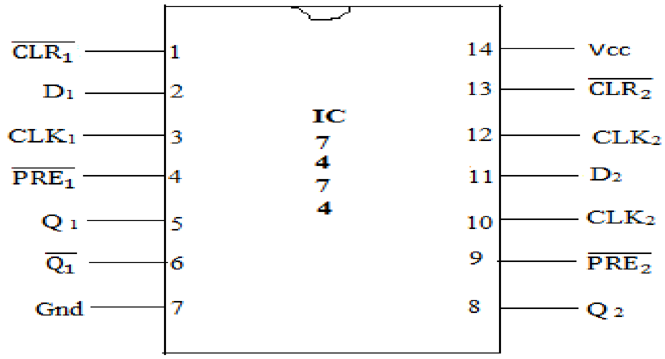
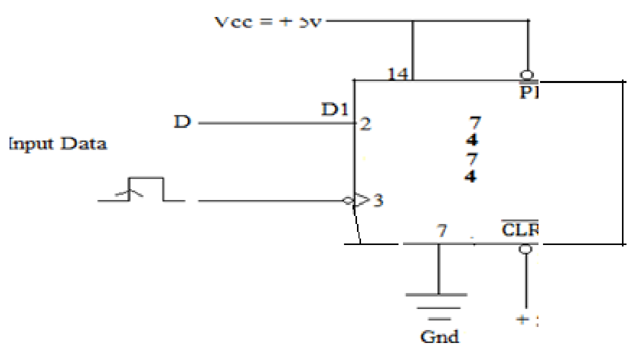


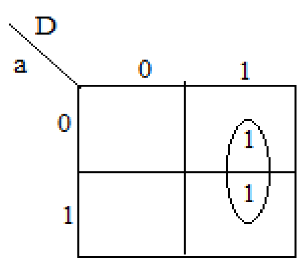
FIG: PIN DIAGRAM

BLOCK IMPLEMENTATION:



Truth Table of D Flip – Flop:

Inputs		Outputs
Q	J	Q_{t+1}
0	0	0
0	1	1
1	0	0
1	1	1



Where

Q $\longrightarrow$ Present State

D $\longrightarrow$ Data Input

Q_{t+1} $\longrightarrow$ Next State

Characteristic eqn $Q_{t+1} = D$

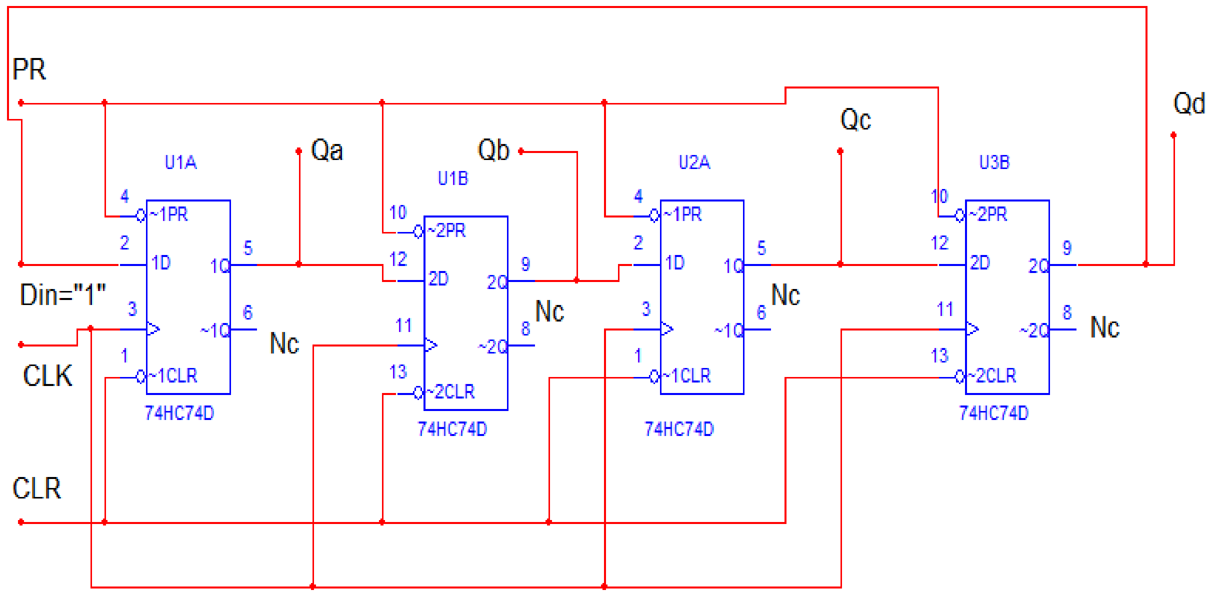
RESULT:

CONCLUSION:

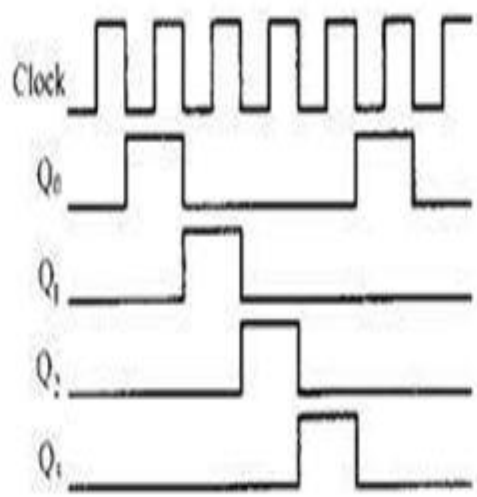
VIVA QUESTIONS:

1. What is flip-flop?
2. How many types of flip-flop are used?
3. What are the characteristic equation for T flip-flop?
4. What is full form of T flip-flop?
5. Which Gates are used in SR flip flops to a JK flip-flop?

<u>BLOCK DIAGRAM OF RING COUNTERS Using D Flip-Flop</u>:



Waveforms for ring counter



Clk	Q_0	Q_1	Q_2	Q_3
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

Exp No:07 **Date:**

RING COUNTER

AIM: Design a four-bit ring counter using D Flip–Flop.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC 7474	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

Ring counter and Johnson counters are basically shift registers.

Ring counter:

It is made by connecting Q&Q‟ output of one JK FF to J&K input of next FF respectively. The output of final FF is connected to the input of first FF. To start the counterthe first FF is set by using preset facility and the remaining FF are reset input. When the clock arrives the set condition continues to shift around the ring ,

As it can be seen from the truth table there are four unique output stages for this counter. The modulus value of a ring counter is *n*, where *n* is the number of flip flops. Ring counter iscalled divided by N counter where N is the number of FF

PROCEDURE:

1. Set up the ring counter and set clear Q outputs using PRESET and apply monopulse.
2. Note down the state of the ring counter on the truth table for successive clock 0.

RESULT:

COCLUSION:

VIVA QUESTIONS:

1. What do you mean by Counter?

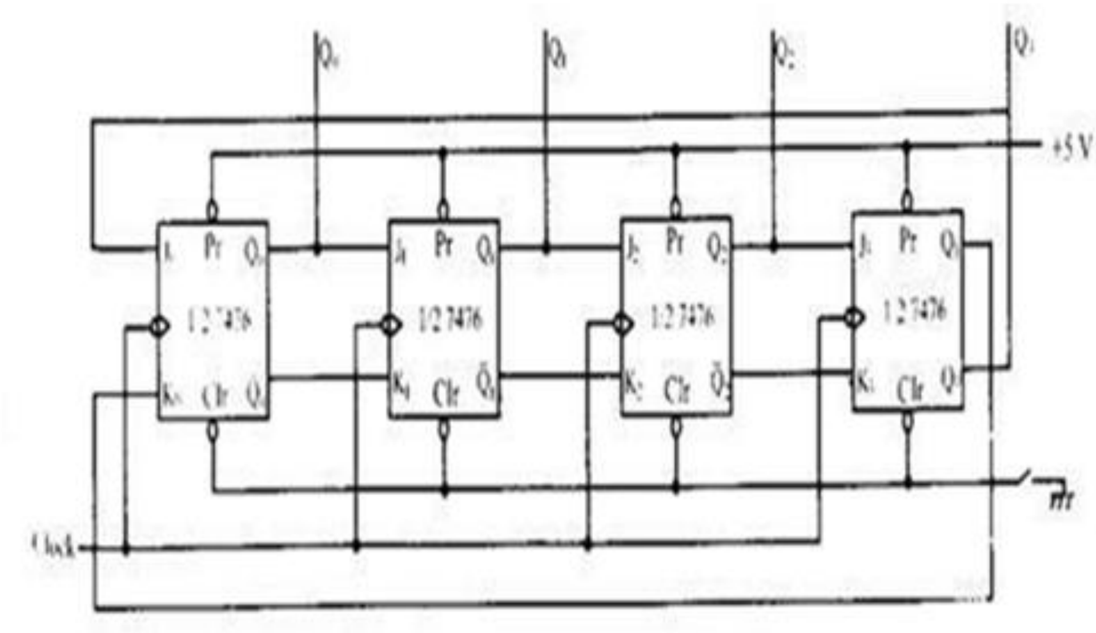
2. What is the ring counter?

3. What are the types of Counters? Explain each

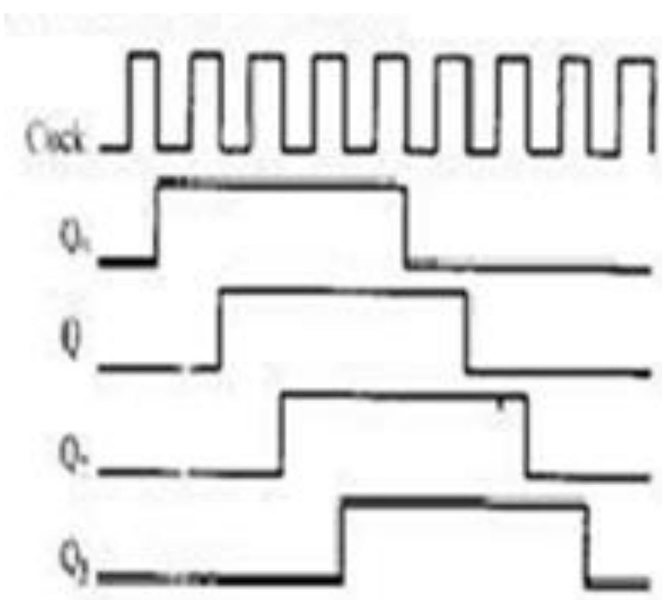
4. Why asynchronous counters are called as ripple counters?

5. What are the applications of asynchronous counters?

BLOCK DIAGRAM OF JOHNSON COUNTER Using Flip-Flop:



MODEL WAVEFORM:



Clk	Q_0 Q_1 Q_2 Q_3
0	0 0 0 0
1	1 0 0 0
2	1 1 0 0
3	1 1 1 0
4	1 1 1 1
5	0 1 1 1
6	0 0 1 1
7	0 0 0 1

Exp No:08 **Date:**

JOHNSON'S COUNTER

AIM: Design a four bit Johnson's counter using JK Flip-Flops

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC 7476	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

Ring counter and Johnson counters are basically shift registers

Johnson counter (Twisted ring counter)

The modulus value of a ring counter can be doubled by making a small change in the ring counter circuit. The Q‟ and Q of the last FFS are connected to the J and K input of the first FFrespectively. This is the Johnson counter.

Initially the FFs are reset. After first clock pulse FF0 is set and the remaining FFs are reset. After the eight clock pulse all the FFS are reset. There are eight different conditions creating a mode 8 Johnson counter. Johnson counter is called a twisted ring counter or divide by 2N counter.

PROCEDURE:

1. Set up the Johnson counter and set clear Q outputs using PRESET and apply mono pulse.
2. Note down the state of the Johnson counter on the truth table for successive clock 0.

RESULT:

COCLUSION:

VIVA QUESTIONS:

1. What is the Johnson counter?

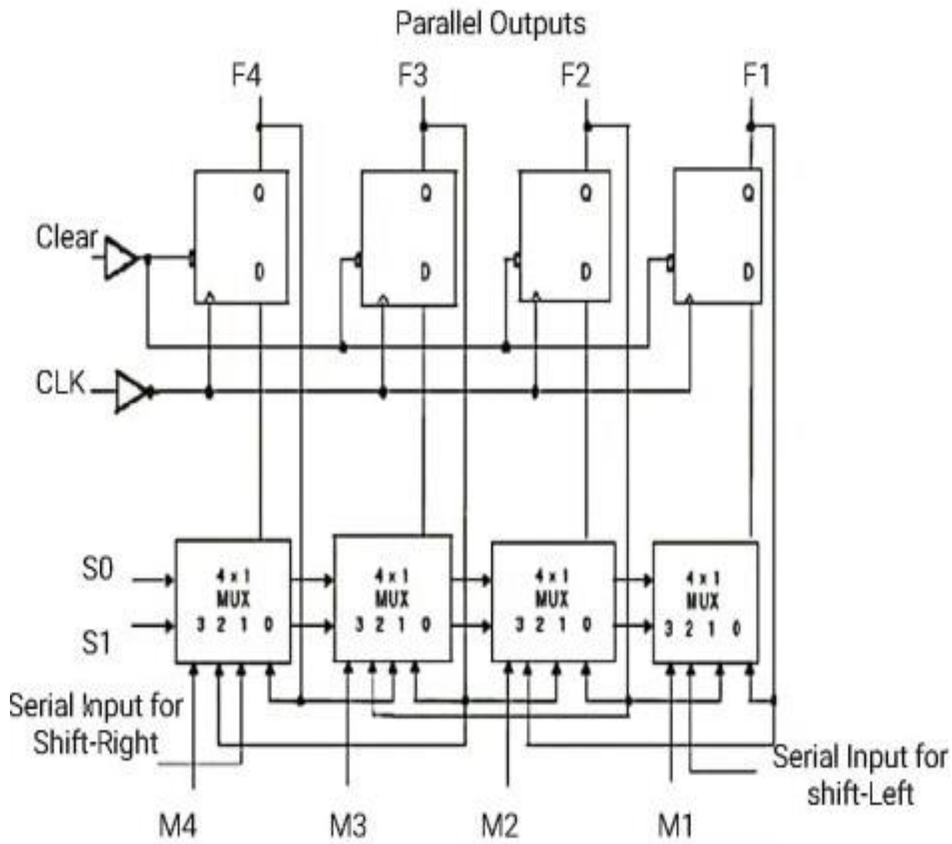
2. What is the difference between the counting sequence of an up counter and a down counter?

3. What down you mean by down counter?

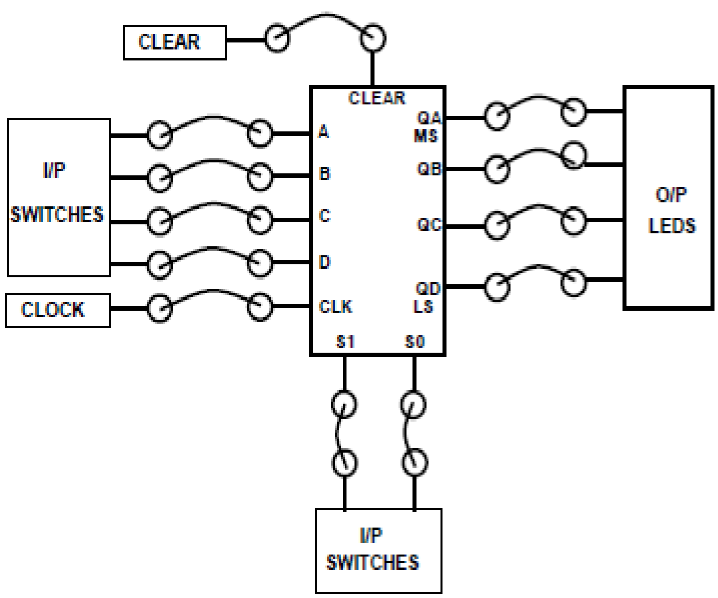
4. What is the advantage of Ripple counter over Synchronous Counter?

5. What are the applications of the counters?

BLOCK DIAGRAM OF USR:



A) PIPO mode:



Exp No:09 **Date:**

UNIVERSAL SHIFT REGISTER

AIM: To study the following applications of the Universal shift register using IC 74194.

a. Left Shift Register

b. PIPO mode

c. Right Shift Register

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC74LS194	1
2	Digital IC Trainer Kit		
3	Patch card		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

Shift registers are the sequential logic circuits that can store the data temporarily and provides the data transfer towards its output device for every clock pulse. These are capable of transferring/shifting the data either towards the right or left in serial and parallel modes. Based on the mode of input/output operations, shift registers can be used as a serial-in-parallel-out shift register, serial-in-serial-out shift register, parallel-in-parallel-out shift register, parallel-in-parallel-out shift register. Based on shifting the data, there are universal shift registers and bidirectional shift registers. Here is a complete description of the universal shift register.

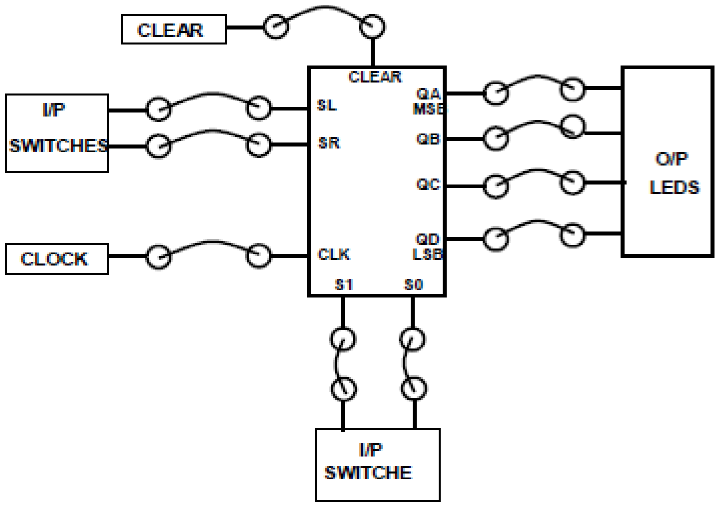
What is a Universal Shift Register?

Definition: A register that can store the data and /shifts the data towards the right and left along with the parallel load capability is known as a universal shift register. It can be used to perform input/output operations in both serial and parallel modes. Unidirectional shift registers and bidirectional shift registers are combined together to get the design of the universal shift register. It is also known as a parallel-in-parallel-out shift register or shift register with the parallel load.

Universal shift registers are capable of performing 3 operations as listed below.

- **Parallel load operation** – stores the data in parallel as well as the data in parallel
- **Shift left operation** – stores the data and transfers the data shifting towards left in the serial path
- **Shift right operation** – stores the data and transfers the data by shifting towards right in the serial path.

PIN DIAGRAM OF RIGHT SHIFT REGISTER



TRUTH TABLE RIGHT SHIFT REGISTER

SR	CLOCK	Q_A	Q_B	Q_C	Q_D	O/P
1	0	0	0	0	0	0
2	1	1	0	0	0	8
3	2	1	1	0	0	12
4	3	1	1	1	0	14
5	4	1	1	1	1	15

LEFT SHIFT REGISTER

SR	CLOCK	$Q_{A(MSB)}$	Q_B	Q_C	Q_D	O/P in DEC
1	0	0	0	0	0	0
2	1	1	0	0	1	1
3	2	1	0	1	1	3
4	3	1	1	1	1	7
5	4	1	1	1	1	15

PROCEDURE:

PIPO

- Set ABCD = 1010 using logic switches. Set S1 = S0 = ‘1’ or Logic HIGH, connect Clear of Shift reg. to CLEAR terminal.
- Connect outputs Q_A to Q_D of reg. to LED indicators.
- Switch on the power supply. All Led indicators are in OFF positions.
- Now give clock signal to Shift register by CLOCK terminal, as soon as clock is reached to Reg. led indicators will show 1010, which is the input we have set for register.
- Now change the data at input side using I/P switches & press clock switch, LED indication now displays the new data. It means this shift register works as parallel in parallel out under clock signal control.

RIGHT SHIT REGISTER

- Do the connection as per block diagram shown below,
- Set S1 = ‘0’, S0 = ‘1’, SL = X, SR = ‘1’. Connect Clear of Shift Reg. to CLEAR terminal.
- Connect outputs Q_A to Q_D of reg. to LED indicators.
- Switch on the power supply. All Led indicators are in OFF positions.
- Now give clock signal to Shift register by CLOCK terminal and observe the LED
- From the above function table we can conclude that this register work as right shift register as it shifts ‘1’ towards right by one position at every clock pulse.
- To start the counting again or to reset the register press CLEAR.

LEFT SHIT REGISTER

- Do the connection as per Right Shift register.
- Set S1 = ‘1’, S0 = ‘0’, SL = ‘1’ and SR = X. Connect Clear of Shift Register to CLEAR terminal.
- Connect outputs QA to QD of reg. to LED indicators.
- Switch on the power supply. All Led indicators are in OFF positions.
- Now give clock signal to Shift register by CLOCK terminal and observe the LED indication.
- From the above function table we can conclude that this register work as Left shift register as it shifts ‘1’ towards left by one position at every clock pulse.
- To start the counting again or to reset the register press CLEAR.

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What do you mean by shift register?

2. Explain the operation of a left shift register & a right shift register?

3. What is the difference between a register and shift register?

4. What is meant by universal shift register?

5. Explain the various modes in which the data can be entered or taken out from a register?

BLOCK DIAGRAM:

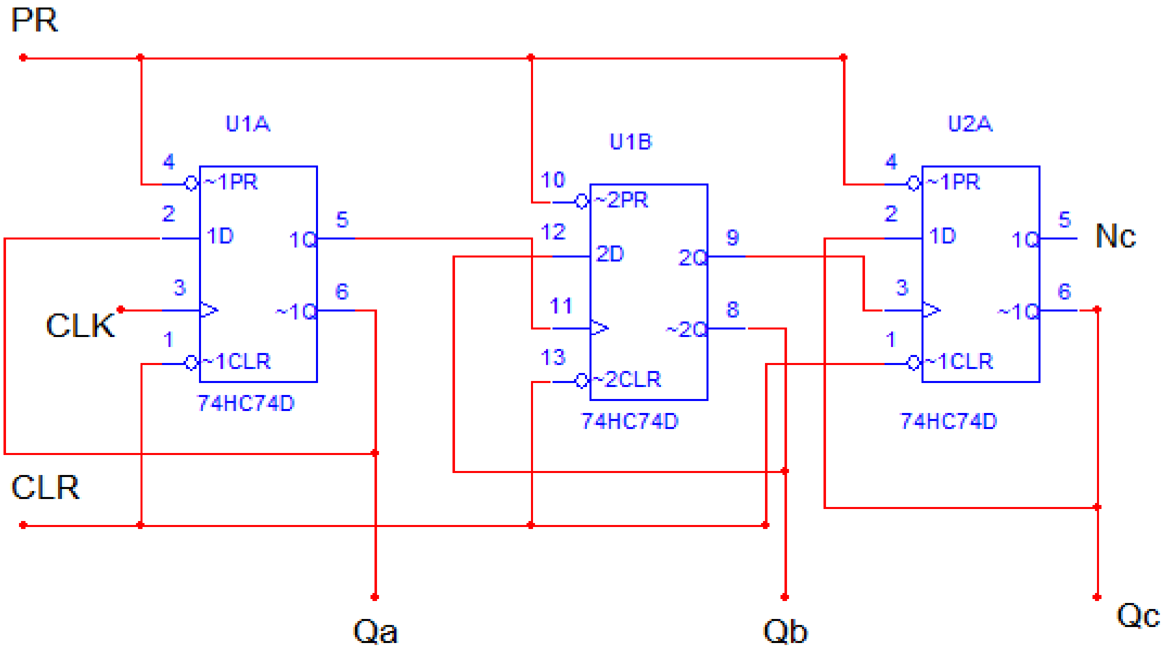


FIG: 3- BIT ASYNCHRONOUS UP COUNTER

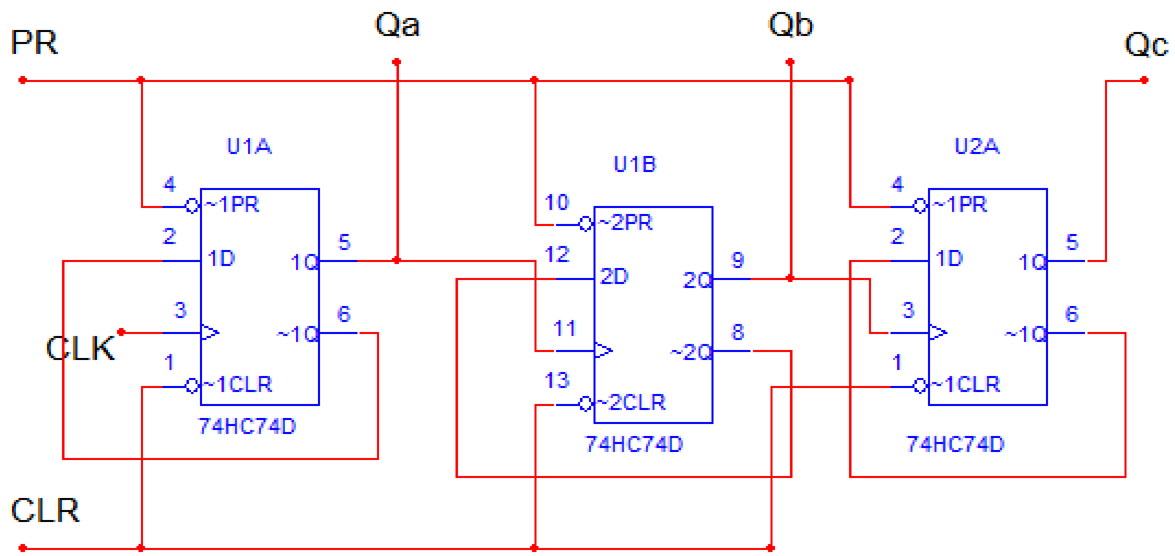


FIG: 3- BIT ASYNCHRONOUS DOWN COUNTER

Exp No:10 **Date:**

MOD-8 RIPPLE COUNTER

AIM: Draw the circuit diagram of MOD-8 ripple counter and construct a circuit using T-Flip-Flops and Test It with a low frequency clock and sketch the output waveforms.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC 7474	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

Asynchronous counter:

A digital counter is a set of flip flop. An Asynchronous counter uses T flip flop to perform a counting function. The actual hardware used is usually J-K flip-flop connected to logic 1.
In ripple counter, the first flip-flop is clocked by the external clock pulse & then each successive flip-flop is clocked by the Q or /Q‘ output the previous flip-flop. Therefore in an asynchronous counter the flip-flop are not clocked simultaneously.

1. **Up Counter:**

Fig shows 3 bit Asynchronous Up Counter. Here Flip-flop A act as a MSB Flip-flop and Flip-flop C can act as a LSB Flip-flop. Clock pulse is connected to the Clock of flip-flop C. Output of Flip-flop C (Qc) is connected to clock of next flip-flop(i.e. Flip-flop B) and so on. As soon as clock pulse changes output is going to -change(at the negative edge of clock pulse) as a Up count sequence. For 3 bit Up counter Truth table is as shown below.

2. **Down Counter:**

Fig shows 3 bit Asynchronous Down Counter. Here Flip-flop a act as a MSB Flip-flop and Flip-flop C can act as a LSB Flip-flop. Clock pulse is connected to the Clock of flip-flop C. Output of Flip-flop C (Qc‘) is connected to clock of next flip- flop (i.e. Flip-flop B) and so on. As soon as clock pulse changes output is going to change(at the negative edge of clock pulse) as a down count sequence. For 3 bit down counter Truth table is as shown below.

Truth Table:

Up Counter

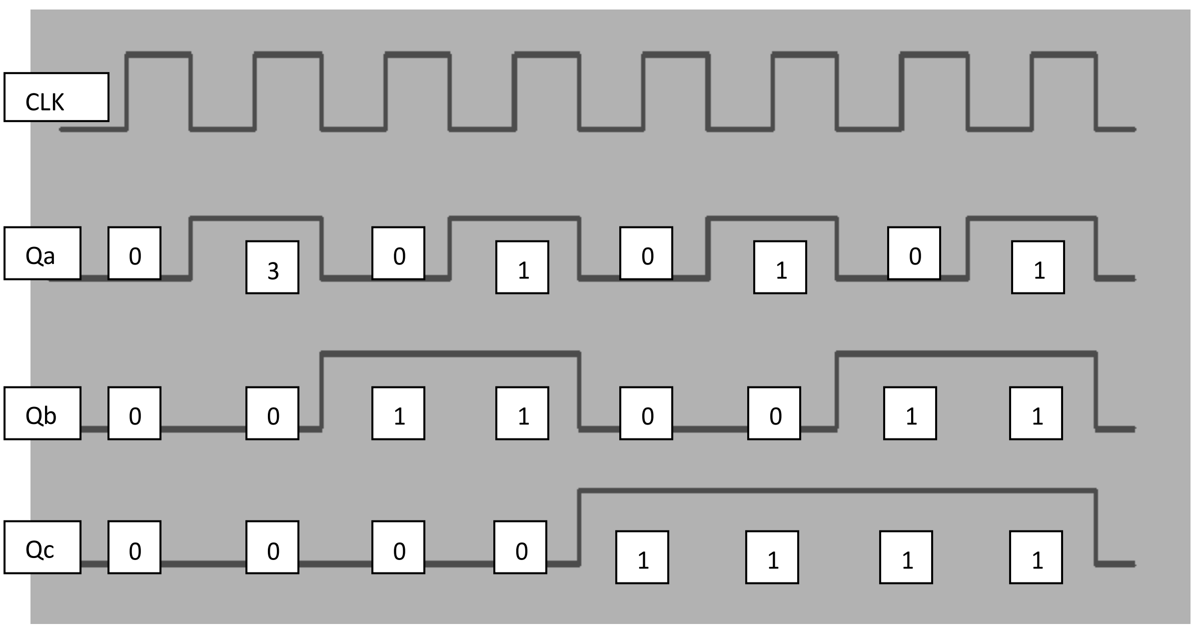
Counter States	F/F Output		
	Q_A	Q_B	Q_C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Down Counter

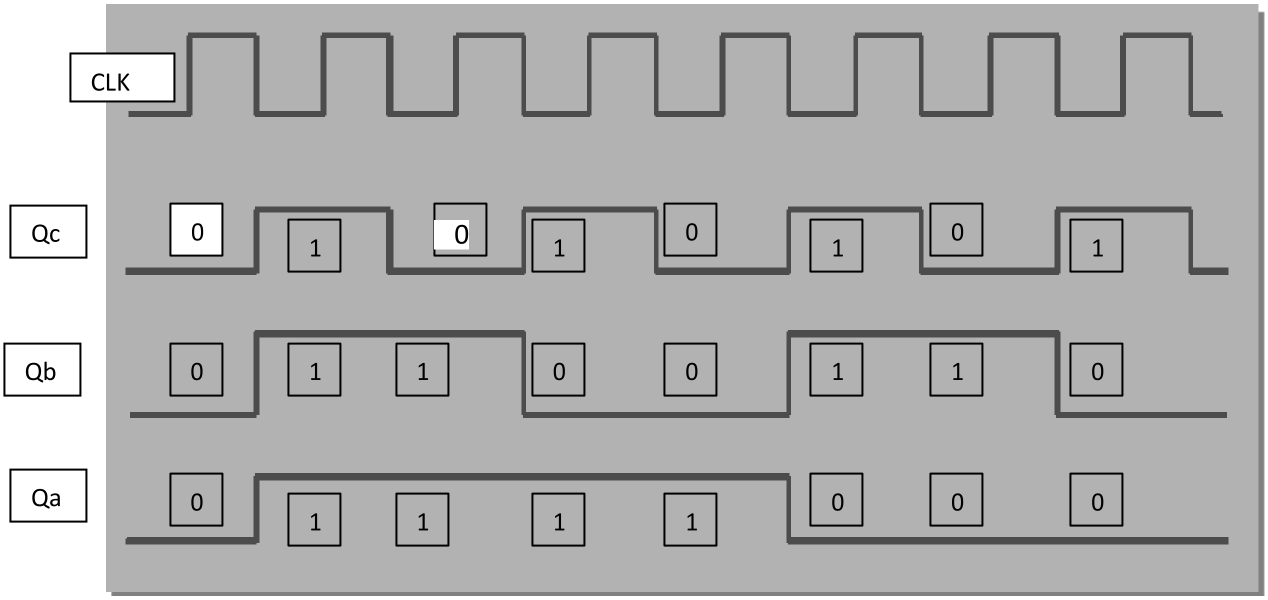
Counter States	F/F Output		
	Q_A	Q_B	Q_C
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	1
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

TIMING DIAGRAM:

1. **3 Bit Asynchronous Up Counter**



2. **3 Bit Asynchronous Down Counter:**



PROCEDURE:

1. Assemble the different counters as shown in above diagrams using JK flip-flop and verify its functionality by referring its function table.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The Vcc and ground should be applied carefully at the specified pin only.

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What do you understand by counter?
2. What is asynchronous counter?
3. What is synchronous counter?
4. Which flip flop is used in asynchronous counter?
5. Which flip flop is used in synchronous counter?

BLOCK DIAGRAM OF MOD-8 COUNTER:

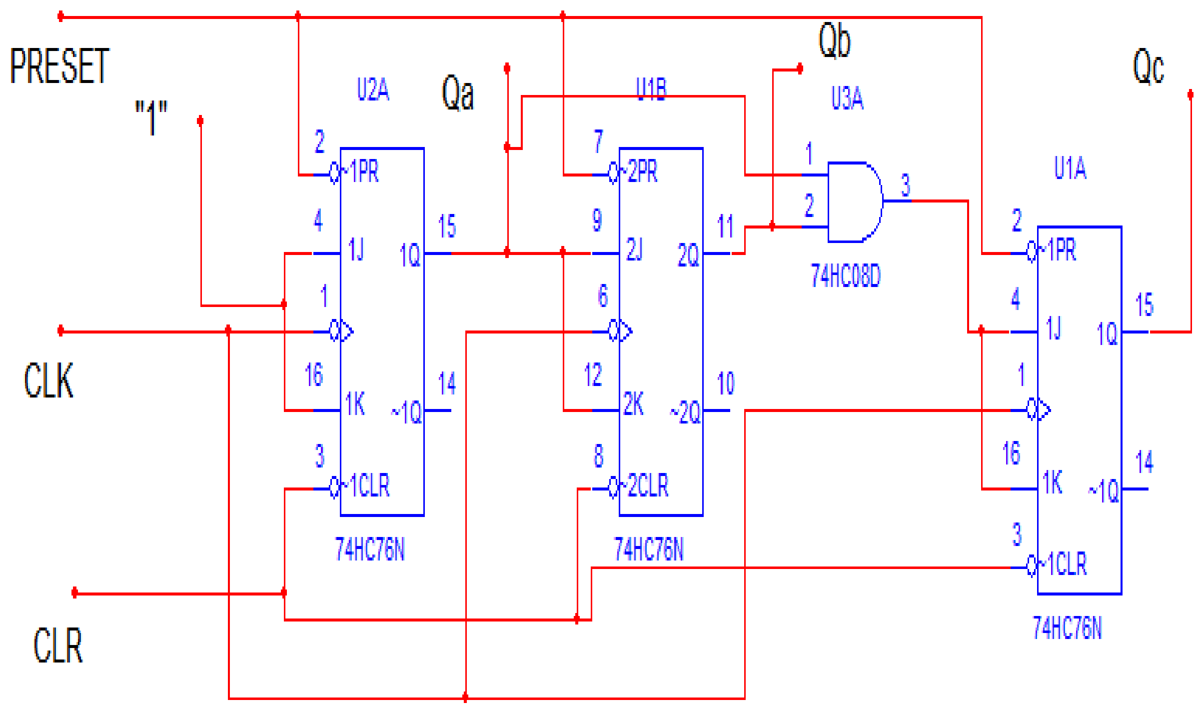


FIG: 3 BIT SYNCHRONOUS COUNTER

TRUTH TABLE:

Q_C	Q_B	Q_A
0	0	0
0	0	1
0	1	0
0	1	1
1	*0*	*0*
1	*0*	*1*
1	*1*	*0*
1	*1*	*1*
0	*0*	*0*

Exp No:11 **Date:**

MOD–8 SYNCHRONOUS COUNTER

AIM: To Design MOD–8 synchronous counter using T Flip-Flop.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC 7476	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

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THEORY:

A counter in which each flip-flop is triggered by the output goes to previous flip-flop. As all the flip-flops do not change states simultaneously in asynchronous counter, spike occur at the output. To avoid this, strobe pulse is required. Because of the propagation delay the operating speed of asynchronous counter is low. This problem can be solved by triggering all the flip-flops in synchronous with the clock signal and such counters are called synchronous counters.

PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

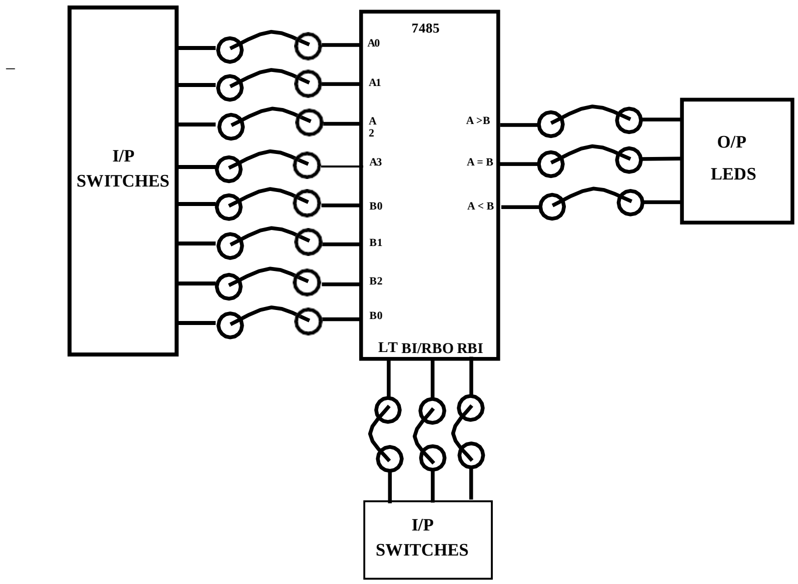
RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What are synchronous counters?
2. What are the advantages of synchronous counters?
3. What is an excitation table?
4. Write the excitation table for D, T FF?
5. Design mod-5 synchronous counter using T FF?

BLOCK DIAGRAM OF 1-BIT COMPARATOR:



TRUTH TABLE:

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

Exp No: 12(a) **Date:**

COMPARATOR

AIM: Draw the circuit diagram of a single bit comparator and test the output.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	7485	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

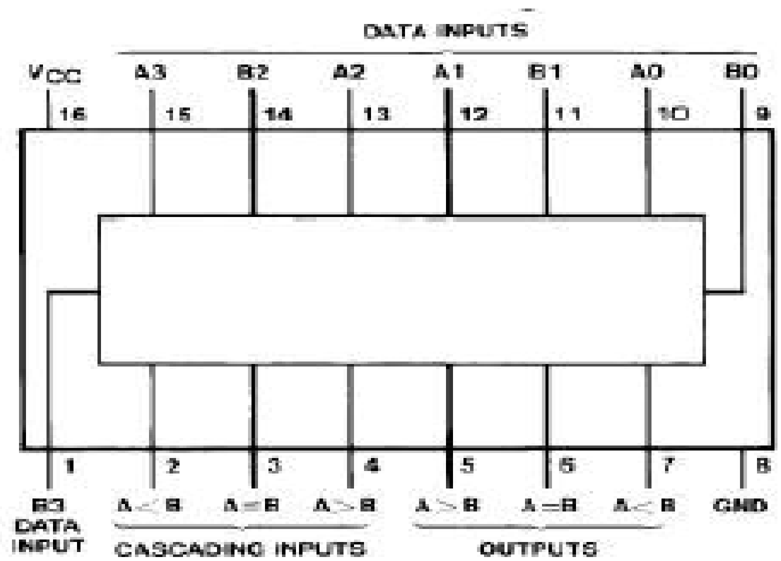
THEORY:

Magnitude Comparator is a logical circuit, which compares two signals A and B andgenerates three logical outputs, whether A > B, A = B, or A < B. IC 7485 is a high speed 4-bit Magnitude comparator , which compares two 4-bit words . The A = B Inputmust be held high for proper compare operation.

PROCEDURE:

1. Do the connection as per block diagram shown below and switch ON the power supply.
2. Give step by step inputs to A & B of comparator starting from MSB (A3 and B3).
3. Initially just observe the comparison between inputs A & B inputs and ignore the cascading inputs.
4. Once all possible combinations for A & B inputs are over then apply cascading inputs as per function table. Observe the outputs of comparator and verify it with function table.
5. Cascading inputs are used to increase the input line capacity of comparator.

Pin Diagram of 7485:



RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What is a comparator?

2. What are the applications of comparator?

3. Derive the Boolean expressions of one bit comparator and two bit comparators.

4. How do you realize a higher magnitude comparator using lower bit comparator

5. Design a 2 bit comparator using a single Logic gates?

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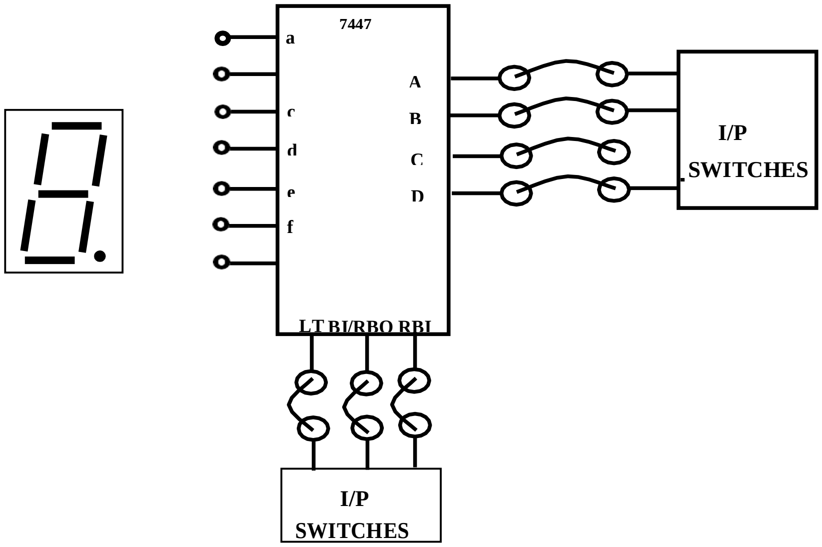
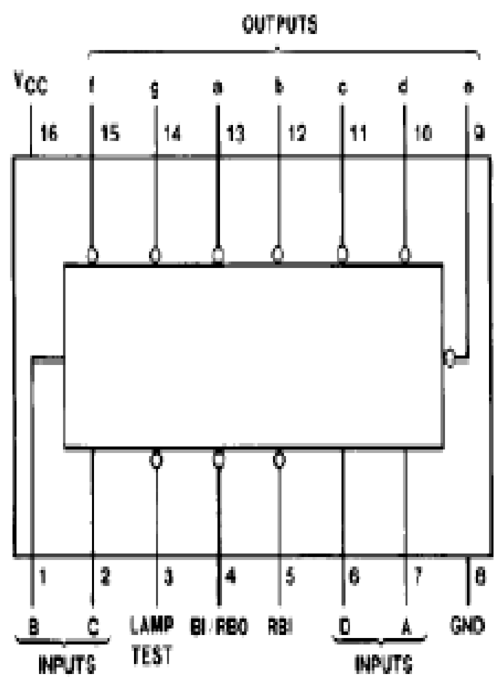
BLOCK DIAGRAM OF SEVEN SEGMENT DIAGRAM:



TRUTH TABLE:

Decimal or Function	Inputs						BI/RBO (Note 1)	Outputs							
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	NOTE 2
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	NOTE 3
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	NOTE 4
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	NOTE 5

PIN FIAGRAM:



Exp No:12(b) **Date:**

7 SEGMENT DISPLAY

AIM: Construct 7 Segment Display Circuit Using Decoder and7 Segment LED and test it.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	7447	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

The functions of LT, RBI, RBO and BI are given below. LT This is called the LAMP TEST terminal and is used for segment testing. If it is connected to logic '0' level, all the segements of the display connected to the decoder will be ON. For normal decoding operation, this terminal is to be connected to logic '1' level. RBI For normal decoding operation, this is connected to logic '1' level. If it is connected to logic '0', the segment outputs will generate the data for normal 7-segment decoding, for all BCD inputs except Zero. Whenever the BCD inputs correspond to Zero, the 7-segment display switches off. This is used for zero blanking in multi-digit displays. BI If it is connected to logic '0' level, the display is switched-off irrespective of the BCD inputs. This is used for conserving the power in multiplexed displays. RBO This output is used for cascading purposes and is connected to the RBI terminal of the succeeding stage.

PROCEDURE:

1. Do the connection as per block diagram shown below and switch on the power supply.
2. For normal operation set LT = '1' RBI = '1' and BI/RBO = '1'. Apply input to the IC from I/P switches as per the function table and observe the output on seven segment display
3. You can give output of onboard Decade counter (7490) as input to seven segment decoder. Observe the output on Display. It displays from 0 to 9 digits.
4. You can also give output of onboard Binary counter (74191) as input to seven segment decoder. Observe the output on Display. It displays digits as shown in the function table for 0 to 15.

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What are the applications of seven segment display?

2. Can you use the segments outputs of 7448 decoder directly to drive a 7-Segment LED? If not suggest a suitable interface?

3. Describe the operation performed by the decoder?

4. What is the function of RBI input?

5. What is the difference between common anode & common cathode display?

ADVANCED EXPERIMENTS

BLOCK DIAGRAM OF BCD ADDEER

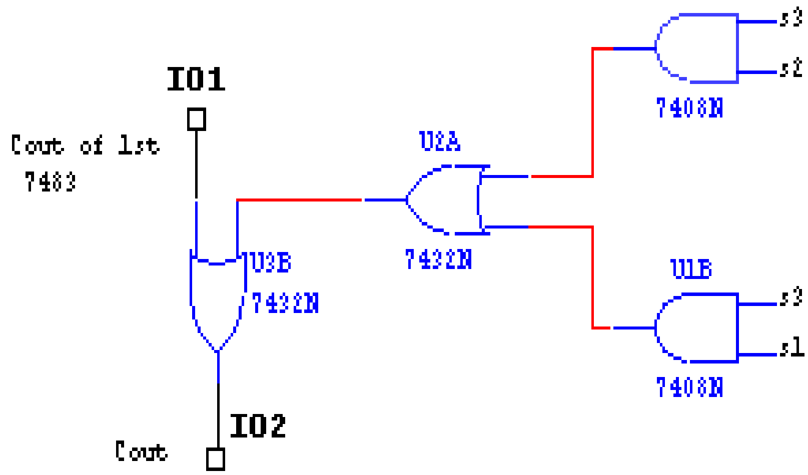


TABLE OF BCD ADDER:

INPUT								OUTPUT				
1st Operand				2nd Operand				MSD	LSD			
A3 (MSB)	A2	A1	A0 (LSB)	B3 (MSB)	B2	B1	B0 (LSB)	Cout	S3 (MSB)	S2	S1	S0 (LSB)

EXP. NO:13 **Date:**

BCD ADDER

AIM: Design BCD Adder Circuit and Test the Same using Relevant IC.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	7483,7432,7408	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

Carry Save Adder:

A carry save adder is just a set of one bit full adder, without any carry chaining. Therefore n-bit CSA receivers three n-bit operands, namely A(n-1),A(0) and CIN(n-1)CIN(0) and generate two n-bit result values, sum(n-1)-----------sum(0) and count(n-1)count(0).

Carry Propagation Adder:

The parallel adder is ripple carry type in which the carry output of each full adder stage is connected to the carry input of the next highest order stage.
Therefore, the sum and carry outputs of any stage cannot be produced until the carry occurs. This leads to a time delay in addition process.
This is known as Carry Propagation Delay.

BCD Adder:

It is a circuit that adds two BCD digits & produces a sum of digits also in BCD.

Rules for BCD addition:

1. Add two numbers using rules of Binary addition.

2. If the 4 bit sum is greater than 9 or if carry is generated then the sum is invalid. To correct the sum add 0110 i.e. (6)10 to sum. If carry is generated from this addition add it to next higher order BCD digit.

3. If the 4 bit sum is less than 9 or equal to 9 then sum is in proper form.

TruthTable:-

For design of combinational circuit for BCD adder to check invalid BCD

INPUT				OUTPUT
S3	**S2**	**S1**	**S0**	**Y**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

K-map:-

For reduced Boolean expressions of output

S3S2 \ S1S0	00	10	11	01
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

Y= $S_3S_2+S_3S_1$

- ✓ **CASE I: Sum <= 9 & carry = 0.**

Add BCD digits 3 & 4

1. 0 0 1 1

+ 0 1 0 0

----

0 1 1 1

Answer is valid BCD number = **(7) BCD** & so 0110 is not added.

CASE II: Sum > 9 & carry = 0.

Add BCD digits 6 & 5

1. 0 1 1 0

+ 0 1 0 1

----

1 0 1 1

Invalid BCD (since sum > 9) so 0110 is to be added

2. 1 0 1 1

+ 0 1 1 0

----

1 0 0 0 1

(1 1)BCD

Valid BCD result = (11) BCD

CASE III: Sum < = 9 & carry = 1.

Add BCD digits 9 & 9

1. 1 0 0 1

+ 1 0 0 1

----

1 0 0 1 0

Invalid BCD (since Carry = 1) so 0110 is to be added

2. 1 0 0 10

+ 0 1 1 0

----

1 1 0 0 0

(1 8)BCD

Valid BCD result = **(18) BCD**

Design of BCD adder:

1. 4 bit binary adder is used for initial addition. i.e. binary addition of two 4 bit numbers.(with Cin = 0),
2. Logic circuit to sense if sum exceeds 9 or carry = 1, this digital circuit will produce highoutput otherwise its output will be zero.
3. One more 4-bit adder to add (0110)2 in the sum is greater than 9 or carry is 1.

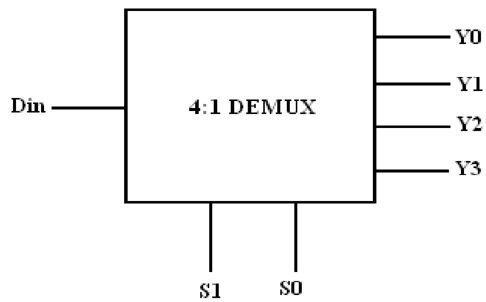
RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What is the need of code converters?
2. What is BCD Adder?
3. What is invalid BCD?
4. What are weighted codes and non-weighted codes?
5. What are applications of Gray code?

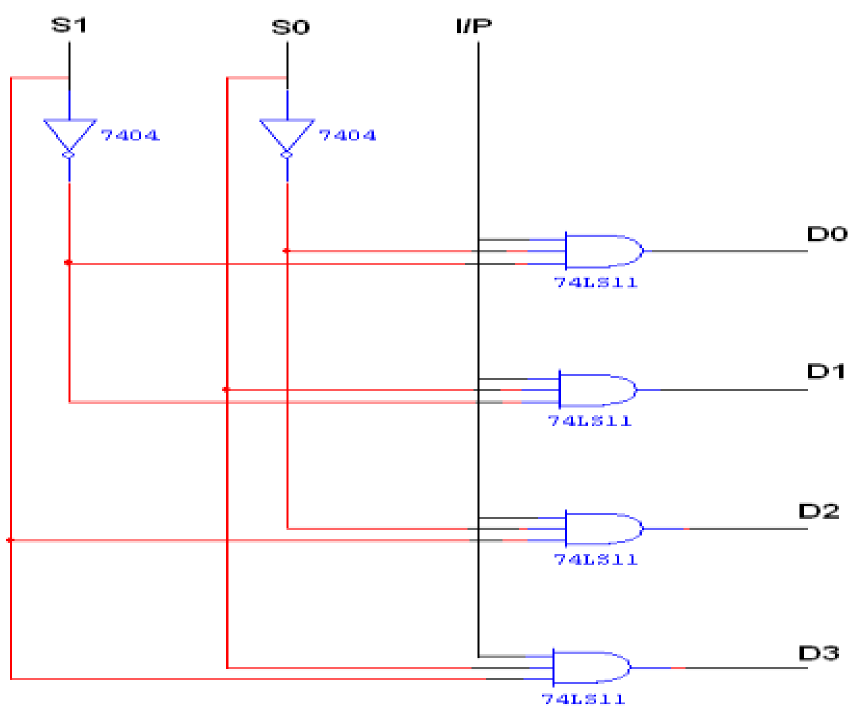
BLOCK DIAGRAM OF 4:1DE-MULTIPLEXER:



TRUTH TABLE

Select Inputs		Data Outputs			
S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	D_{in}	0	0	0
0	1	0	D_{in}	0	0
1	0	0	0	D_{in}	0
1	1	0	0	0	D_{in}

CIRCUIT DIAGRAM:



Exp No:14 **Date:**

4:1DE-MULTIPLEXER

AIM: - Verification of the truth table of the 4:1De-Multiplexer.

APPARATUS REQUIRED: -

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	7404,7411	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

A Demultiplexer performs the reverse operation of a Multiplexer. It accepts a single input and distributes it over several outputs. The SELECT input code determines to which output the data input will be transmitted. The Demultiplexer becomes enabled when the strobe signal is active LOW.

This circuit can also be used as binary-to-decimal decoder with binary inputs applied at the select input lines and the output will be obtained on the corresponding line. These devices are available as 2-line-to-4-line decoder, 3-line-to- 8-line decoder, 4-line-to-16-line decoder. The output of these devices is active LOW. Also there is an active low enable/data input terminal available. Figure below shows the block diagram of a Demultiplexer.

In this diagram the inputs and outputs are indicated by means of broad arrows to indicate that there may be one or more lines. Depending upon the digital code applied at the SELECT inputs, one data is transmitted to the single output channel out of many. The pin out of a 16:1 Demultiplexer IC 74154 is shown above. The output of this circuit is active low. This is a 24-pin DIP.

PROCEDURE: -

1) Assemble the circuit on bread board, as per above Pin diagram.
2) Give the logical inputs and check for the proper output, as per the truth table.

PRECAUTIONS:

- All connections should be made neat and tight.
- Digital lab kits and ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- Never touch live and naked wires

RESULT:

CONCLUSION:

VIVAQUESTIONS:

1. Why is a demultiplexer called data distributor?

2. How does a demux works?

3. Which IC is used for demux?

4. What is difference between MUX and DEMUX?

5. Can decoder be used as demux?