

LINEAR AND DIGITAL IC APPLICATIONS LAB MANUAL



Department of Electronics & Communication Engineering

VEMU INSTITUTE OF TECHNOLOGY::P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

(Approved by AICTE, New Delhi & Affiliated to JNTUA, Anantapuramu)

LINEAR AND DIGITAL IC APPLICATIONS LAB MANUAL



Name: _____

H.T.No: _____

Year/Semester: _____

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VEMU Institute of Technology
Dept. of Electronics and Communication Engineering

Vision of the institute

To be one of the premier institutes for professional education producing dynamic and vibrant force of technocrats with competent skills, innovative ideas and leadership qualities to serve the society with ethical and benevolent approach.

Mission of the institute

Mission_1: To create a learning environment with state-of-the art infrastructure, well equipped laboratories, research facilities and qualified senior faculty to impart high quality technical education.

Mission_2: To facilitate the learners to inculcate competent research skills and innovative ideas by Industry-Institute Interaction.

Mission_3: To develop hard work, honesty, leadership qualities and sense of direction in learners by providing value based education.

Vision of the department

To develop as a center of excellence in the Electronics and Communication Engineering field and produce graduates with Technical Skills, Competency, Quality, and Professional Ethics to meet the challenges of the Industry and evolving Society.

Mission of the department

Mission_1: To enrich Technical Skills of students through Effective Teaching and Learning practices to exchange ideas and dissemination of knowledge.

Mission_2: To enable students to develop skill sets through adequate facilities, training on core and multidisciplinary technologies and Competency Enhancement Programs.

Mission_3: To provide training, instill creative thinking and research attitude to the students through Industry-Institute Interaction along with Professional Ethics and values.

Programme Educational Objectives (PEOs)

PEO 1: To prepare the graduates to be able to plan, analyze and provide innovative ideas to investigate complex engineering problems of industry in the field of Electronics and Communication Engineering using contemporary design and simulation tools.

PEO-2: To provide students with solid fundamentals in core and multidisciplinary domain for successful implementation of engineering products and also to pursue higher studies.

PEO-3: To inculcate learners with professional and ethical attitude, effective communication skills, teamwork skills, and an ability to relate engineering issues to broader social context at work place

Programme Outcomes(Pos)

PO_1	Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO_2	Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO_3	Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO_4	Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO_5	Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO_6	The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO_7	Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO_8	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO_9	Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO_10	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO_11	Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO_12	Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Programme Specific Outcome(PSOs)

PSO_1	Higher Education : Qualify in competitive examination for pursuing higher education by applying the fundamental concepts of Electronics and Communication Engineering domains such as Analog & Digital Electronics, Signal Processing, Communication & Networking, Embedded Systems, VLSI Design and Control systems etc.,
PSO_2	Employment: Get employed in allied industries through their proficiency in program specific domain knowledge, Specialized software packages and Computer programming or became an entrepreneur.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

II B.Tech. II-Sem (ECE)

(20A04403P) LINEAR AND DIGITAL IC APPLICATIONS LABORATORY

COURSE OUTCOMES (CO_s)

CO. No	Description	Bloom Level
C228.1	Understand the pin configuration of each linear/ digital IC and its functional diagram.	
C228.2	Conduct the experiment and obtain the expected results.	
C228.3	Analyze the given circuit/designed circuit and verify the practical observations with the analyzed results.	
C228.4	Design the circuits for the given specifications using linear and digital ICs.	
C228.5	Acquaintance with lab equipment about the operation and its use.	

LIST OF EXPERIMENTS:

PART – I: Linear IC Experiments

- 1.OP AMP Applications – Adder, Subtractor, Comparators.
- 2.Integrator and Differentiator Circuits using IC 741.
3. Active Filter Applications – LPF, HPF (first order)
4. IC 741 Waveform Generators – Sine, Square wave and Triangular waves.
5. IC 555 Timer – Monostable and Astable Multivibrator Circuits.
6. Schmitt Trigger Circuits – using IC 741
- 7.IC 565 – PLL Applications.
8. Voltage Regulator using IC 723, Three Terminal Voltage Regulators – 7805, 7809, 7912.

PART – II: Digital IC Applications

- 1.3-8 decoder using 74138
2. 4-bit comparator using 7485.
3. 8*1 Multiplexer using 74151 and 2*4 Demultiplexer using 74155.
4. D, JK Flip Flops using 7474, 7483.
5. Decade counter using 7490.
6. UP/DOWN counter using 74163
7. Universal shift registers using 74194/195.
8. RAM (16*4) using 74189 (Read and Write operations).

Note: At least 12 experiments shall be performed.



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Dept. of Electronics and Communication Engineering

(20A04403P) LINEAR AND DIGITAL IC APPLICATIONS LAB

II B.Tech-II SEM

LIST OF EXPERIMENTS TO BE CONDUCTED.

PART – I: Linear IC Experiments

1. OP AMP Applications – Adder, Subtractor, Comparators.
2. Integrator and Differentiator Circuits using IC 741.
3. Active Filter Applications – LPF, HPF (first order)
4. IC 741 Waveform Generators – Sine, Square wave and Triangular waves.
5. IC 555 Timer – Monostable and Astable Multivibrator Circuits.
6. Schmitt Trigger Circuits – using IC 741

PART – II: Digital IC Applications

7. 3-8 decoder using 74138
8. 4-bit comparator using 7485.
9. 8*1 Multiplexer using 74151 and 2*4 Demultiplexer using 74155.
10. D, JK Flip Flops using 7474, 7483.
11. Decade counter using 7490.
12. Universal shift registers using 74194/195.

Additional experiments (Beyond Curriculum)

13. Digital to Analog Convertor
14. Code Convertors (Binary to gray, gray to binary)

CONTENTS

S.NO.	NAME OF THE EXPERIMENT	PAGE NO
1.	OP AMP Applications – Adder, Subtractor, Comparators.	
2.	Integrator and Differentiator Circuits using IC 741.	
3.	Active Filter Applications – LPF, HPF (first order)	
4.	IC 741 Waveform Generators – Sine, Square wave and Triangular waves.	
5.	IC 555 Timer – Monostable and Astable Multivibrator Circuits.	
6.	Schmitt Trigger Circuits – using IC 741	
7.	3-8 decoder using 74138	
8.	4-bit comparator using 7485	
9.	8*1 Multiplexer using 74151 and 2*4 Demultiplexer using 74155.	
10.	D, JK Flip Flops using 7474, 7483.	
11.	Decade counter using 7490	
12.	Universal shift registers using 74194/195.	
Additional experiments (Beyond Curriculum)		
13.	Digital to Analog Convertor	
14.	Code Convertors (Binary to gray ,gray to binary)	

DOS & DONTs IN LABORATORY

DO's

1. Students should be punctual and regular to the laboratory.
2. Students should come to the lab in-time with proper dress code.
3. Students should maintain discipline all the time and obey the instructions.
4. Students should carry observation and record completed in all aspects.
5. Students should be at their concerned experiment table, unnecessary moment is restricted.
6. Students should follow the indent procedure to receive and deposit the components from lab technician.
7. While doing the experiments any failure/malfunction must be reported to the faculty.
8. Students should check the connections of circuit properly before switch ON the power supply.
9. Students should verify the reading with the help of the lab instructor after completion of experiment.
10. Students must ensure that all switches are in the lab OFF position, all the connections are removed.
11. At the end of practical class the apparatus should be returned to the lab technician and take back the indent slip.
12. After completing your lab session SHUTDOWN the systems, TURN OFF the power switches and arrange the chairs properly.
13. Each experiment should be written in the record note book only after getting signature from the lab in charge in the observation notebook.

DON'Ts

1. Don't eat and drink in the laboratory.
2. Don't touch electric wires.
3. Don't turn ON the circuit unless it is completed.
4. Avoid making loose connections.
5. Don't leave the lab without permission.
6. Don't bring mobiles into laboratory.
7. Do not open any irrelevant sites on computer.
8. Don't use a flash drive on computers.

SCHEME OF EVALUATION

S.No	Program	Date	Marks Awarded				Total 30(M)
			Record (10M)	Obs. (10M)	Viva (5M)	Attd. (5M)	
1.							
2.							
3.							
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7.							
8.							
9.							
10.							
11.							
12.							
Additional experiments (Beyond Curriculum)							
13.							
14.							

Signature of Lab In-charge

PART-I

LINEAR IC EXPERIMENTS

STUDY OF OP AMPS - IC 741, IC 555, IC 565, IC 566
FUNCTIONING, PARAMETERS AND SPECIFICATIONS.

AIM: To study the function of OP AMPs - IC 741, IC 555, IC 565, IC 566, along with its functioning parameters and specifications.

IC 741**General Description**

The IC 741 is a high performance monolithic operational amplifier constructed using the planar epitaxial process. High common mode voltage range and absence of latch-up tendencies make the IC 741 ideal for use as voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier and general feedback applications.

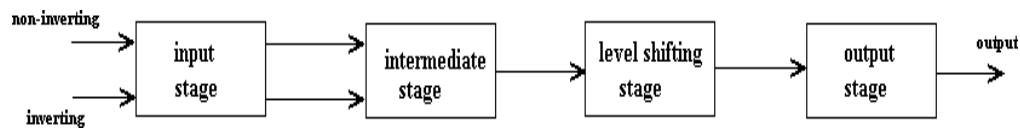
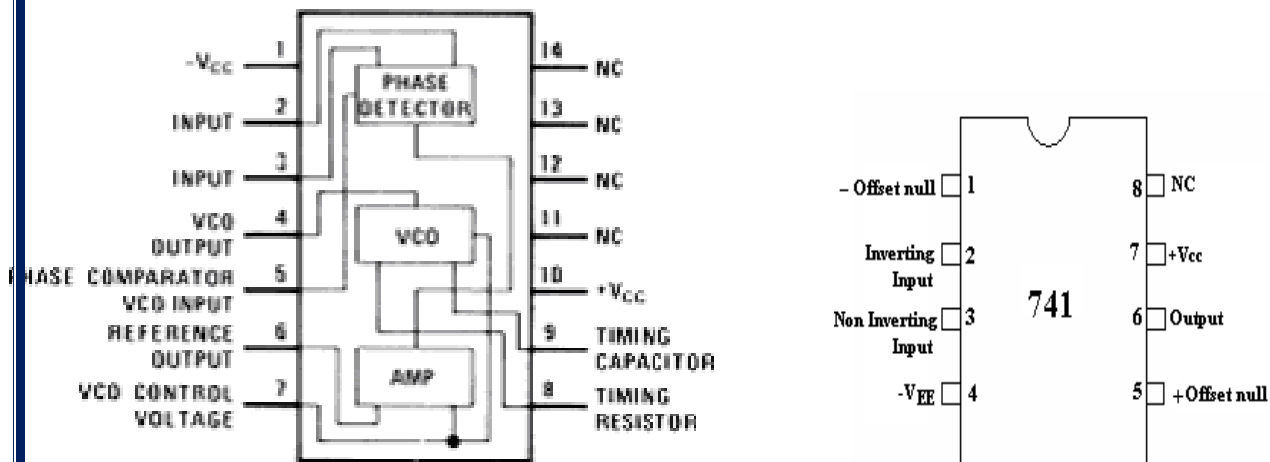
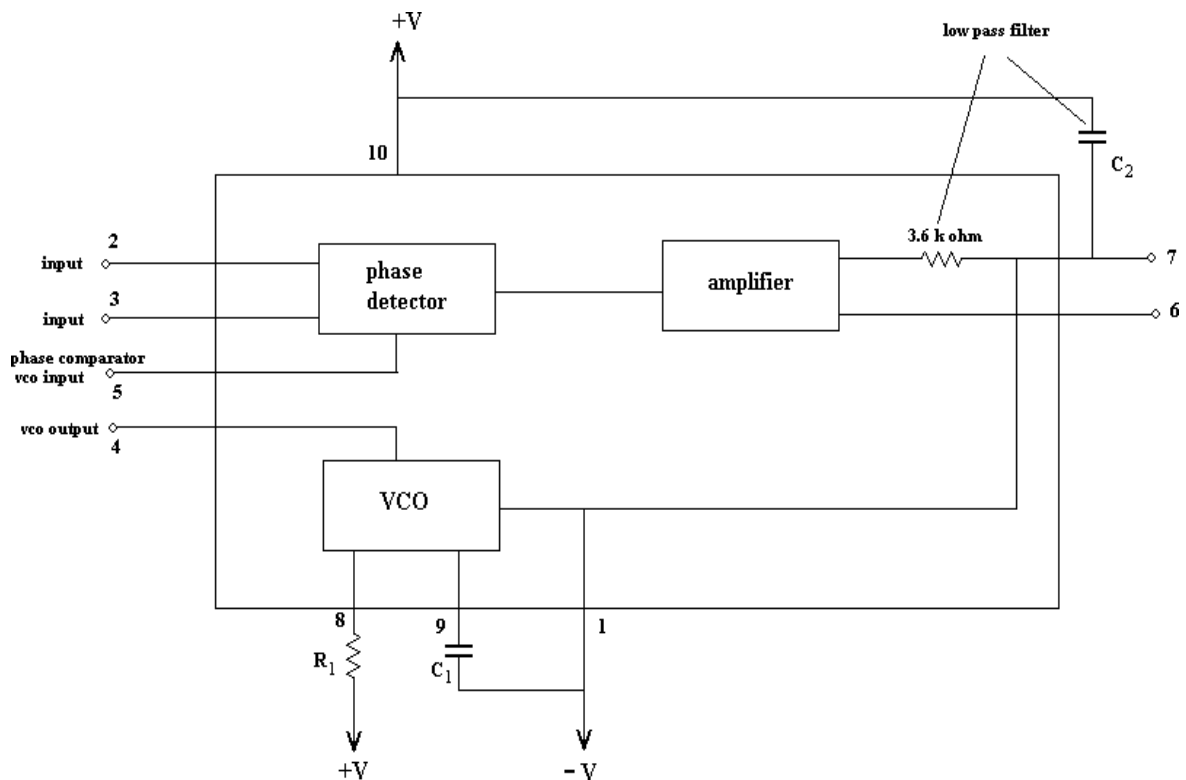
Features

1. No frequency compensation required.
2. Short circuit protection
3. Offset voltage null capability
4. Large common mode and differential voltage ranges
5. Low power consumption
6. No latch-up

Specifications

1. Voltage gain $A = \alpha$ typically 2,00,000
2. I/P resistance $R_L = \alpha \Omega$, practically $2M\Omega$
3. O/P resistance $R = 0$, practically 75Ω
4. Bandwidth = α Hz. It can be operated at any frequency
5. Common mode rejection ratio = α
6. Slew rate = α V/ μ sec
7. When $V_1 = V_2$, $V_D = 0$
8. Input offset voltage ($R_s \leq 10K\Omega$) max 6 mV
9. Input offset current = max 200nA
10. Input bias current : 500nA
11. Input capacitance : typical value 1.4pF
12. Offset voltage adjustment range : ± 15 mV
13. Input voltage range : ± 13 V
14. Supply voltage rejection ratio : 150 μ V/V
15. Output voltage swing: + 13V and - 13V for $R_L > 2K\Omega$
16. Output short-circuit current: 25mA
17. supply current: 28mA
18. Power consumption: 85mW
19. Transient response: rise time= 0.3 μ s

INTERNAL BLOCK DIAGRAM OF OP-AMP

**PIN CONFIGURATION and DIAGRAM:*****BLOCK DIAGRAM OF IC 565:***

Applications

1. AC and DC amplifiers
2. Active filters
3. Oscillators
4. Comparators
5. Regulators

IC 555

General Description

The operation of SE/NE 555 timer directly depends on its internal function. The three equal resistors R_1 , R_2 , R_3 serve internal voltage divider for the source voltage. Thus one-third of the source voltage V_{CC} appears across each resistor. Comparator is basically an Op amp which changes state when one of its inputs exceeds the reference voltage. The reference voltage for the lower comparator is $+1/3 V_{CC}$. If a trigger pulse applied at the negative input of this comparator drops below $+1/3 V_{CC}$, it causes a change in state. The upper comparator is referenced at voltage $+2/3 V_{CC}$.

The output of each comparator is fed to the input terminals of a flip flop. The flip-flop used in the SE/NE 555 timer IC is a bistable multivibrator. This flip flop changes states according to the voltage value of its input. Thus if the voltage at the threshold terminal rises above $+2/3 V_{CC}$, it causes upper comparator to cause flip-flop to change its states. On the other hand, if the trigger voltage falls below $+1/3 V_{CC}$, it causes lower comparator to change its states. Thus the output of the flip flop is controlled by the voltages of the two comparators. A change in state occurs when the threshold voltage rises above $+2/3 V_{CC}$ or when the trigger voltage drops below $+1/3 V_{CC}$.

The output of the flip-flop is used to drive the discharge transistor and the output stage. A high or positive flip-flop output turns on both the discharge transistor and the output stage. The discharge transistor becomes conductive and behaves as a low resistance short circuit to ground. The output stage behaves similarly. When the flip-flop output assumes the low or zero states reverse action takes place i.e., the discharge transistor behaves as an open circuit or positive V_{CC} state. Thus the operational state of the discharge transistor and the output stage depends on the voltage applied to the threshold and the trigger input terminals.

Function of Various Pins

Pin (1) of 555 is the ground terminal; all the voltages are measured with respect to this pin.

Pin (2) of 555 is the trigger terminal, if the voltage at this terminal is held greater than one-third of V_{CC} , the output remains low. A negative going pulse from V_{CC} to less than $V_{CC}/3$ triggers the output goes to High. The amplitude of the pulse should be able to make the comparator (inside the IC) change its state. However the width of the negative going pulse must not be greater than the width of the expected output pulse.

Pin (3) is the output terminal of IC 555. There are 2 possible output states. In the low output state, the output resistance appearing at pin (3) is very low (approximately 10Ω). As a result the output

current will go to zero, if the load is connected from Pin (3) to ground, sink a current I_{Sink} (depending upon load) if the load is connected from Pin (3) to ground, and sinks zero current if the load is connected between +VCC and Pin (3).

Pin (4) is the Reset terminal. When unused it is connected to +Vcc. Whenever the potential of Pin (4) is driven below 0.4V, the output is immediately forced to low state. The reset terminal enables the timer over-ride command signals at Pin (2) of the IC.

Pin (5) is the Control Voltage terminal. This can be used to alter the reference levels at which the time comparators change state. A resistor connected from Pin (5) to ground can do the job. Normally $0.01\mu\text{F}$ capacitor is connected from Pin (5) to ground. This capacitor bypasses supply noise and does not allow it affect the threshold voltages.

Pin (6) is the threshold terminal. In both astable as well as monostable modes, a capacitor is connected from Pin (6) to ground. Pin (6) monitors the voltage across the capacitor when it charges from the supply and forces the already high O/p to Low when the capacitor reaches $+2/3 V_{\text{CC}}$.

Pin (7) is the discharge terminal. It presents an almost open circuit when the output is high and allows the capacitor charge from the supply through an external resistor and presents an almost short circuit when the output is low.

Pin (8) is the +Vcc terminal. 555 can operate at any supply voltage from +3 to +18V.

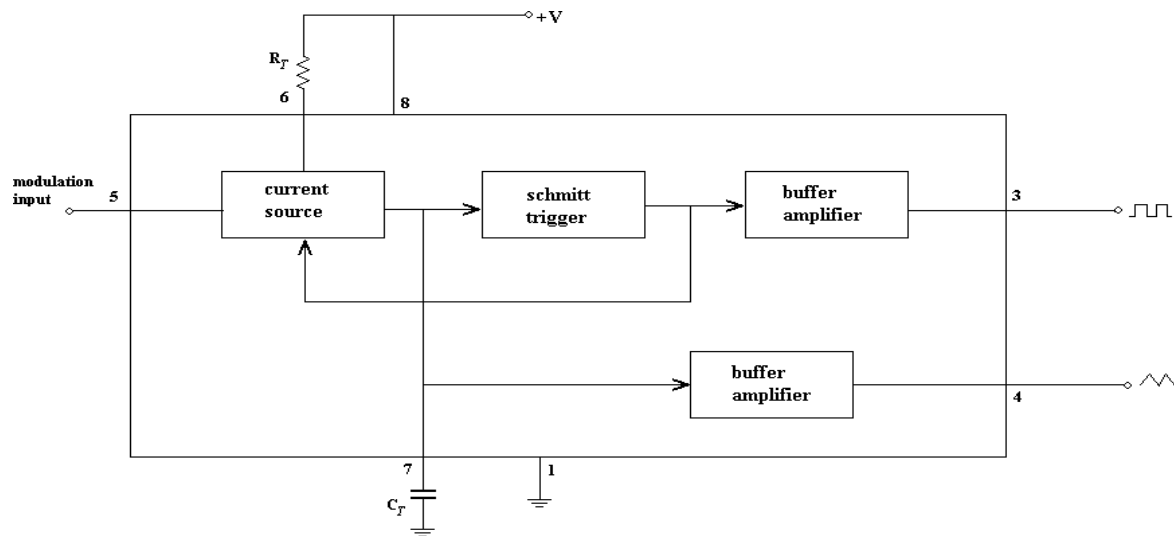
Features

1. The load can be connected to o/p in two ways i.e. between pin 3 & ground 1 or between pin 3 & VCC (supply)
2. 555 can be reset by applying negative pulse, otherwise reset can be connected to +Vcc to avoid false triggering.
3. An external voltage effects threshold and trigger voltages.
4. Timing from micro seconds through hours.
5. Monostable and bistable operation
6. Adjustable duty cycle
7. Output compatible with CMOS, DTL, TTL
8. High current output sink or source 200mA
9. High temperature stability
10. Trigger and reset inputs are logic compatible.

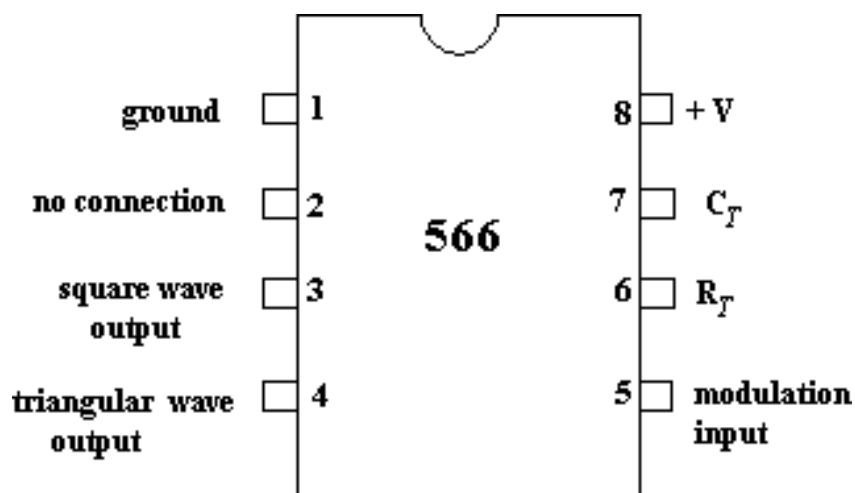
Specifications

1. Operating temperature : SE 555---55oC to 125oC
NE 555-- 0o to 70oC
2. Supply voltage : +5V to +18V
3. Timing : μSec to Hours
4. Sink current : 200mA
5. Temperature stability : 50 PPM/oC change in temp or 0-005% /oC.

BLOCK DIAGRAM OF IC 566



PIN DIAGRAM:



Applications

1. Monostable and Astable Multivibrators
2. dc-ac converters
3. Digital logic probes
4. Waveform generators
5. Analog frequency meters
6. Tachometers
7. Temperature measurement and control
8. Infrared transmitters
9. Regulator & Taxi gas alarms etc.

IC 565**General Description**

The Signetics SE/NE 560 series is monolithic phase locked loops. The SE/NE 560, 561, 562, 564, 565, & 567 differ mainly in operating frequency range, power supply requirements and frequency and bandwidth adjustment ranges. The device is available as 14 Pin DIP package and as 10-pin metal can package. Phase comparator or phase detector compare the frequency of input signal f_s with frequency of VCO output f_o and it generates a signal which is function of difference between the phase of input signal and phase of feedback signal which is basically a d.c voltage mixed with high frequency noise. LPF remove high frequency noise voltage. Output is error voltage. If control voltage of VCO is 0, then frequency is center frequency (f_o) and mode is free running mode. Application of control voltage shifts the output frequency of VCO from f_o to f . On application of error voltage, difference between f_s & f tends to decrease and VCO is said to be locked. While in locked condition, the PLL tracks the changes of frequency of input signal.

Specifications

1. Operating frequency range : 0.001 Hz to 500 KHz
2. Operating voltage range : ± 6 to ± 12 V
3. Inputs level required for tracking: 10mV rms minimum to 3v (p-p)max.
4. Input impedance : 10 K Ω typically
5. Output sink current : 1mA typically
6. Drift in VCO center frequency: 300 PPM/ $^{\circ}$ C typically (f_{out}) with temperature
7. Drif in VCO centre frequency with : 1.5%/V maximum supply voltage
8. Triangle wave amplitude : typically 2.4 VPP at ± 6 V
9. Square wave amplitude : typically 5.4 VPP at ± 6 V
10. Output source current : 10mA typically
11. Bandwidth adjustment range : $<\pm 1$ to $>\pm 60\%$

Center frequency $f_{out} = 1.2/4R1C1$ Hz = free running frequency

$FL = \pm 8 f_{out}/V$ Hz

$V = (+V) - (-V)$

$f_c = \pm 1/2$

Applications

1. Frequency multiplier
2. Frequency shift keying (FSK) demodulator
3. FM detector

IC 566**General Description**

The NE/SE 566 Function Generator is a voltage controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage with exceptional linearity.

Maximum operating Voltage --- 26V

Input voltage --- 3V (P-P)

Storage Temperature --- -65°C to + 150°C

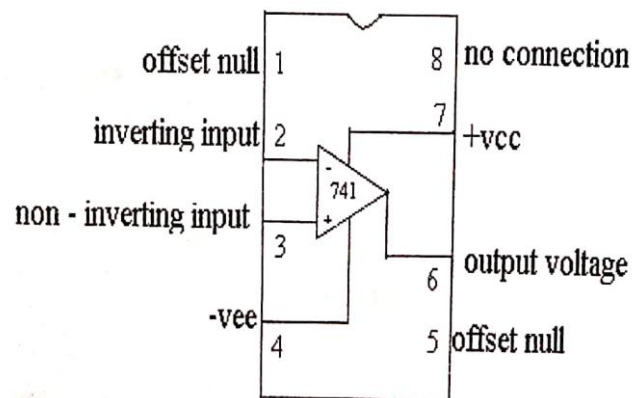
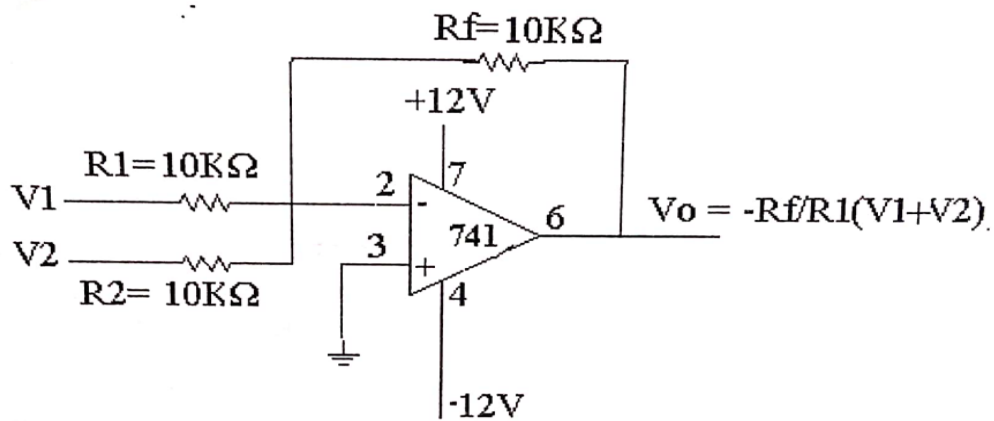
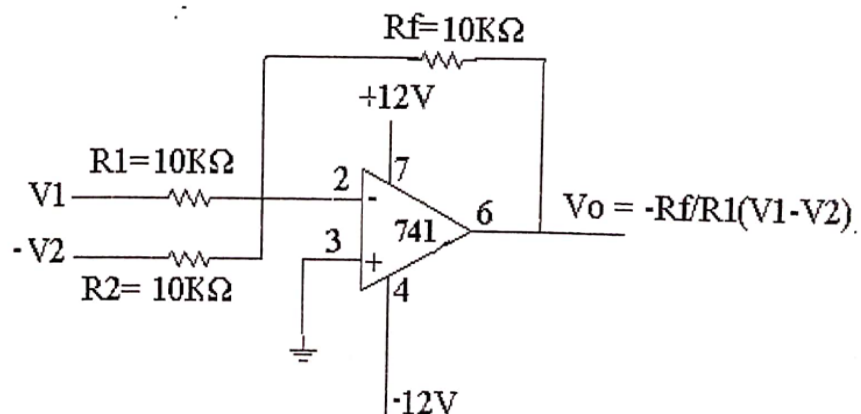
Operating temperature --- 0°C to +70°C for NE 566

-55°C to +125°C for SE 566

Power dissipation --- 300mW

Applications

1. Tone generators.
2. Frequency shift keying
3. FM Modulators
4. clock generators
5. signal generators
6. Function generator

PIN DIAGRAM-IC741**ADDER:****SUBTRACTOR:**

Exp. No:**Date:****ADDER, SUBTRACTOR&COMPARATOR**

AIM: To Study the amplifications of IC 741 an op-amp such as an adder, subtractor and comparator circuits.

APPARATUS:

S.No	Name of the Item	Range	Quantity
1	IC	741	1
2	Resistors	10 k Ω	3
		1k Ω	2
3	RPS	(0-30)v	1
4	FPS	+/- 12v	1
5	Multimeter		1
6	Bread Board		1
7	Connecting wires		1

PROCEDURE:

1. Circuit was connected as shown in figure.
2. Fixed power supply of +12v at pin7 and -12v at pin4 was applied.
3. Differential inputs were applied and measured the corresponding output voltage.
4. Output values are compared with theoretical value.

PRECAUTIONS:

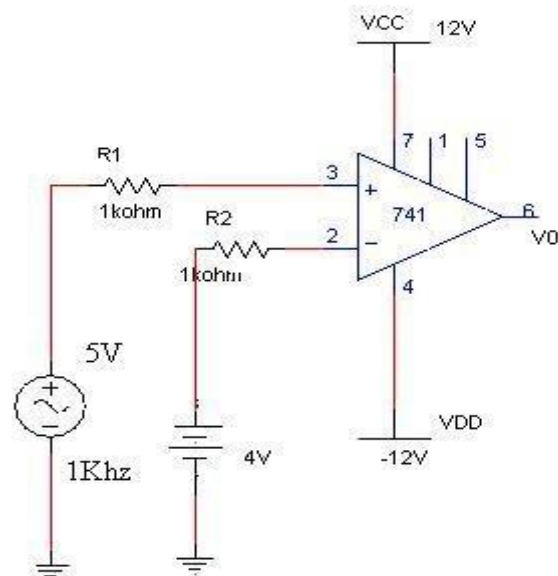
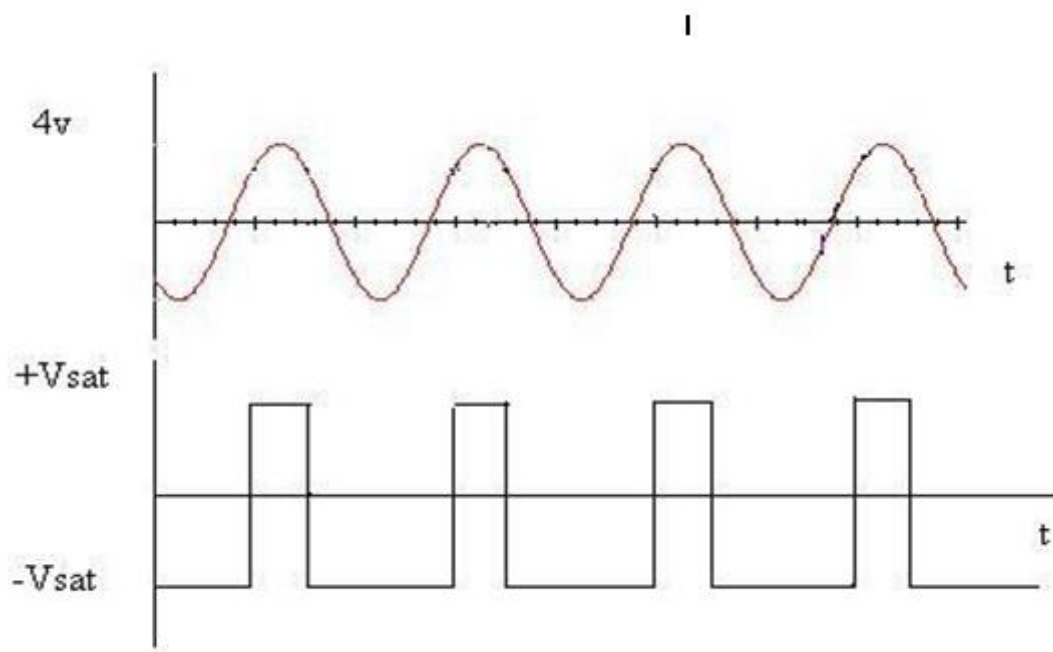
1. Make null adjustment before applying the input signal.
2. Maintain proper Fpss levels.

Applications of adder and sub tractor:

1. Digital signal processing
2. Communication

Applications of comparator:

1. Zero crossing detector
2. Level detector
3. Time marker generator
4. Window detector

COMPARATOR:**EXPECTED WAVEFORMS FOR COMPARATOR:**

TABULAR COLUMN:**ADDER**

S.No	V1(volts)	V2(volts)	Practical voltage(v)	Theoretical voltage(v)

SUBTRACTOR:

S.No	V1(volts)	V2(volts)	Practical voltage(v)	Theoretical voltage(v)

COMPARATOR:

S.No	V1(volts)	V2(volts)	Practical voltage(v)	Theoretical voltage(v)

RESULT:

CONCLUSION:

VIVA QUESTIONS:

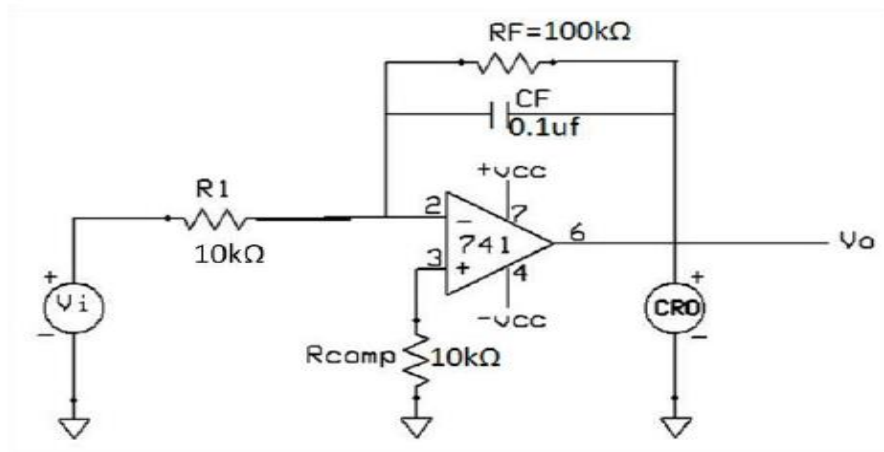
1. Mention different amplifier configurations.

2. Draw an Op- amp circuit whose output $V_O = V_1 + V_2 - V_3 - V_4$.

3. Show that the o/p of an n-input inverting adder is $V_O = -(V_a + V_b + \dots + V_n)$

4. Draw the circuit of non-inverting adder with 3 inputs and find the o/p Voltage V_O .

5. Applications of adder and subtractor.

CIRCUIT DIAGRAM:**Integrator****Design equations:*****Integrator:***

Choose $T = 2\pi R_f C_f$

Where T = Time period of the input signal Assume C_f and find R_f

Select $R_f = 100R_1$

$$V_{o(p-p)} = \frac{-1}{RC} \int_0^{T/2} V_{i(p-p)} dt$$

Integrator:

For $T = 1 \text{ msec}$

$$f_a = 1/T = 1 \text{ KHz}$$

$$f_a = 1 \text{ KHz} = 1/(2\pi R_f C_f)$$

Assuming $C_f = 1\mu_f$, R_f is found from $R_f = 1/(2\pi f_a C_f)$

$$R_f = 100 \text{ K}\Omega$$

$$R_f = 100 R_1, R_1 = 10 \text{ K}\Omega$$

Exp. No:

Date:

INTEGRATOR AND DIFFERENTIATOR**AIM:** To design, construct and verify the response of

- Integrator using Op-amp IC741 for sine and square wave inputs at 1 KHz frequency.
- Differentiator using Op-amp IC741 for sine and square wave inputs at 1 KHz frequency

APPARATUS REQUIRED:

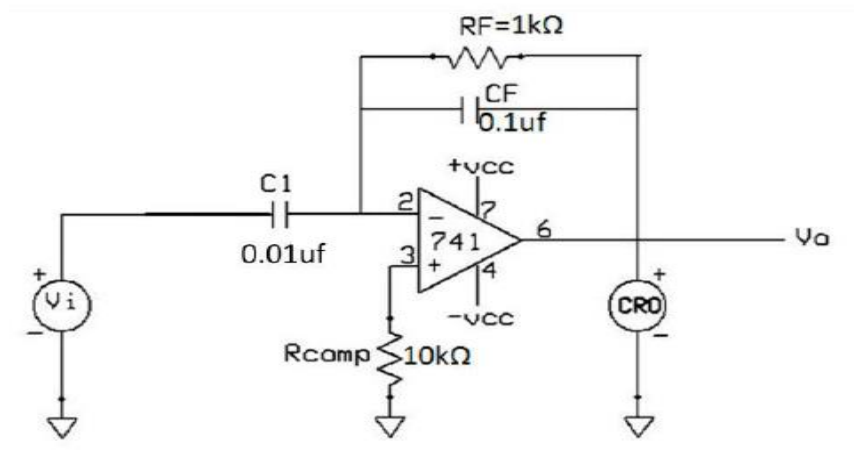
S. No.	Equipment/Component	Specifications/Value	Quantity
1	IC	741	1
2	Resistors	10 k Ω	2
		100k Ω	1
3	Regulated Power supply	(0 – 10)V	1
4	capacitor	0.1 μ f, 0.01 μ f	1
5	Function Generator	(0 – 3MHz), 20V _{p-p}	
6	Cathode Ray Oscilloscope	20MHz	1
7	Connecting wires		As per required

PROCEDURE:**Integrator:**

- Connect the circuit as shown in figure:1
- Apply the power supplies as $V_{CC} = +12V$ and $V_{EE} = -12V$.
- Apply square wave input at 1KHz and 2Vp-p amplitude, choose the time period of the signal $T \geq R_F C_F$
- Observe integrator output at terminal V_o .
- Plot the input and output waveforms.

Differentiator:

- Connect the circuit as per the diagram shown in Fig.2
- Apply a square wave/sine input of 4V(p-p) at 1KHz
- Observe the output at pin 6
- Draw the input and output waveforms as shown in Fig.

CIRCUIT DIAGRAM:**Differentiator****Design equations:**

Select given frequency $f_a = 1/(2\pi R_f C_1)$, Assume C_1

and find R_f Select $f_b = 10 f_a$ $1/2\pi R_1 C_1$ and find

R_1

From $R_1 C_1 = R_f C_f$, find C_f

Differentiator Design:

For $T = 1 \text{ msec}$

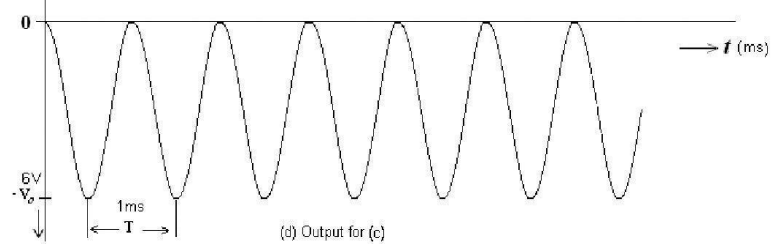
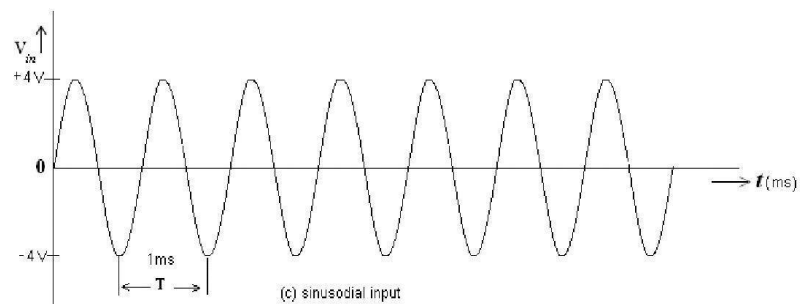
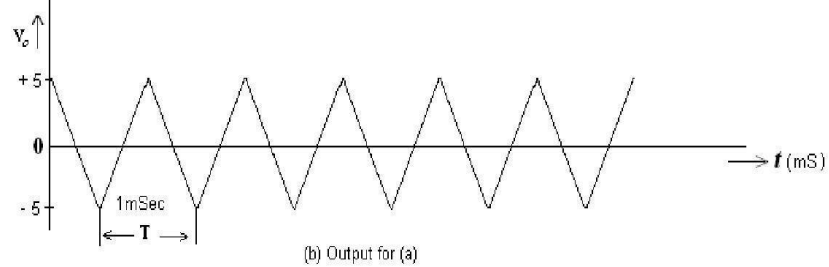
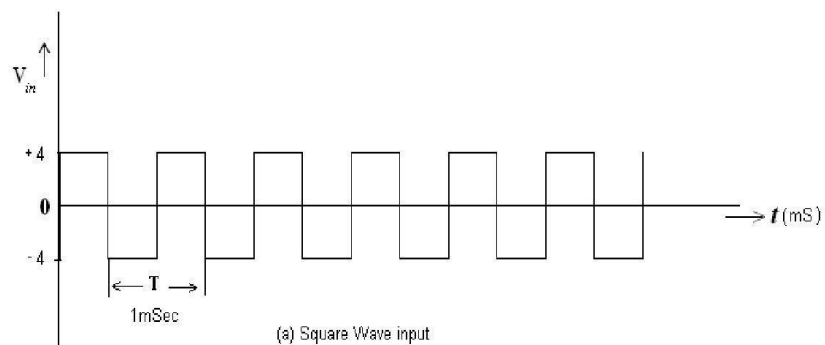
$$f = 1/T = 1 \text{ KHz}$$

$$f_a = 1 \text{ KHz} = 1/(2\pi R_f C_1)$$

Assuming $C_1 = 0.1 \mu\text{f}$, R_f is found from $R_f = 1/(2\pi f_a C_1)$

$$R_f = 1 \text{ K}\Omega$$

$$f_b = 10 f_a = 1/2\pi R_1 C_1 \text{ for } C_1 = 0.1 \mu\text{f}; R_{\text{comp}} = 10 \text{ K}\Omega$$

MODEL WAVEFORMS:**Integrator**

TABULAR COLUMN:***Integrator:***

Input –Square wave		Output – Triangular	
Amplitude (VP-P) (V)	Time period (ms)	Amplitude (VP-P) (V)	Time period (ms)

Input –sine wave		Output – cosine	
Amplitude (VP-P) (V)	Time period (ms)	Amplitude (VP-P) (V)	Time period (ms)

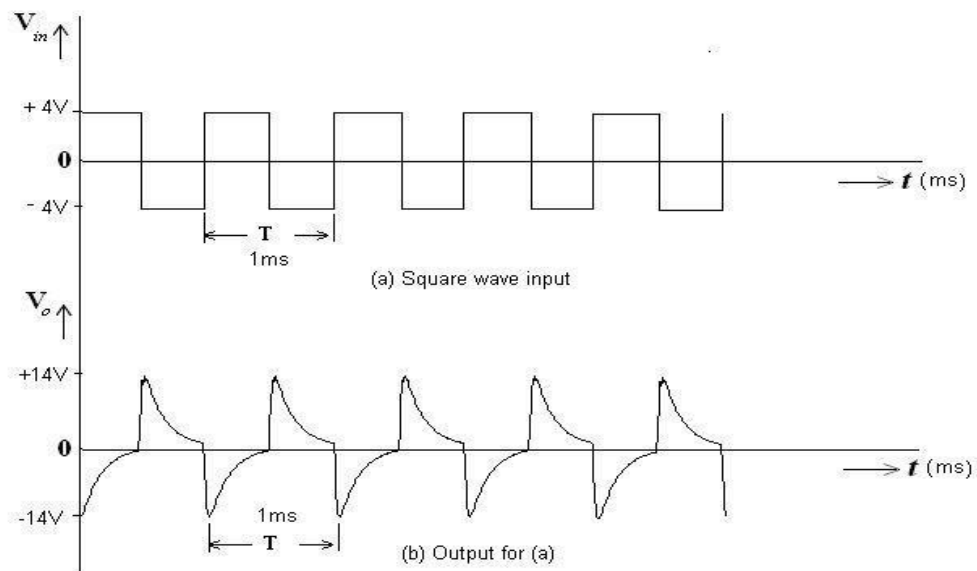
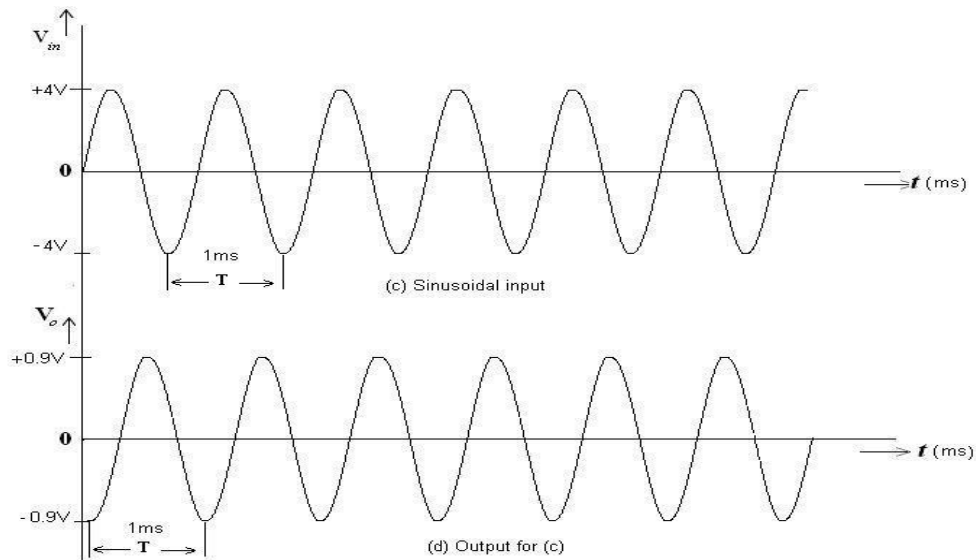
Differentiator

Amplitude (VP-P) (V)	Time period (ms)	Amplitude (VP-P) (V)	Time period (ms)

Input –sine wave		Output - cosine	
Amplitude (VP-P) (V)	Time period (ms)	Amplitude (VP-P) (V)	Time period (ms)

PRECAUTIONS:

1. Connections should be made properly.
2. Avoid loose connections.

MODEL WAVEFORMS:**Differentiator**

RESULT:

CONCLUSION:

VIVA QUESTIONS:

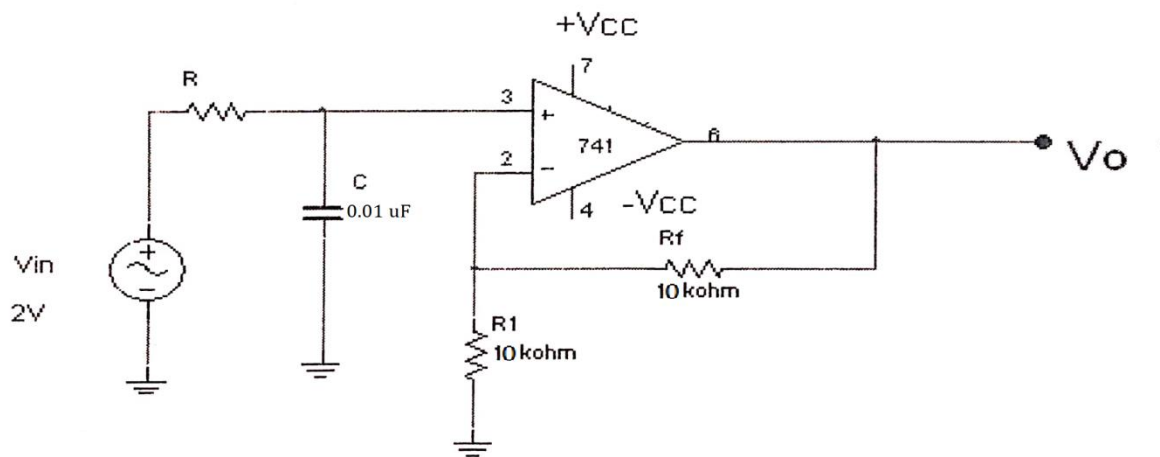
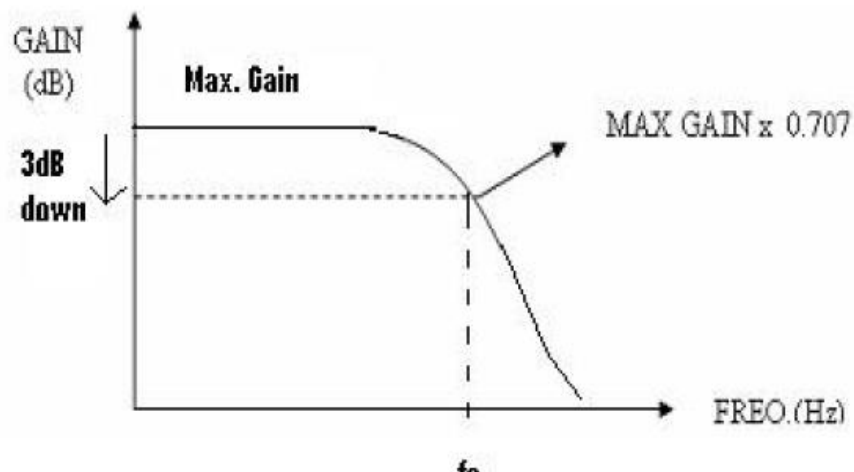
1. What is integrator and write the expression for output of integrator?

2. What is differentiator and write the expression for output of differentiator?

3. What is the output of ideal integrator & differentiator for unit step input?

4. Write the applications of integrator & differentiator in communication?

5. Compare integrator & differentiator.

LOW PASS FILTER (FIRST ORDER)**FREQUENCY RESPONSE:**

Exp. No:**Date:****ACTIVE FILTER – (LPF&HPF First Order)**

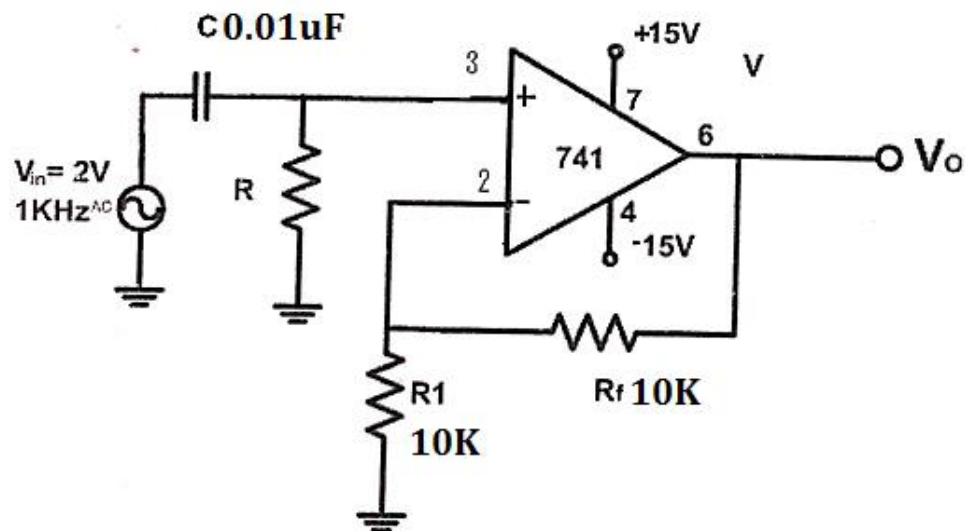
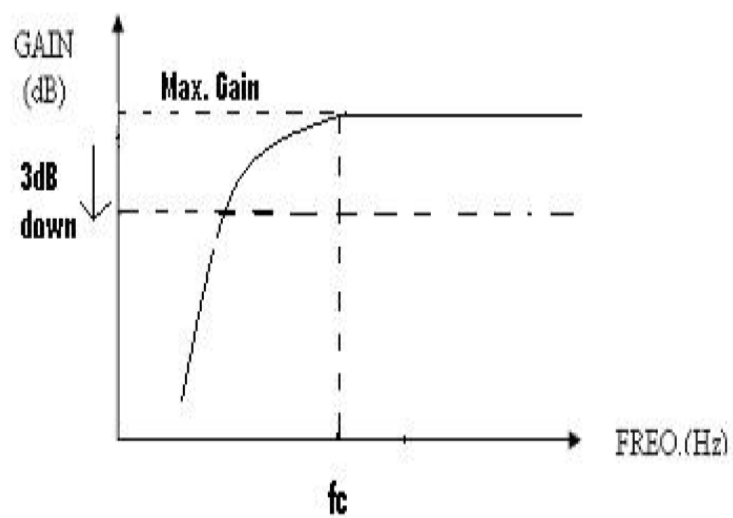
AIM: To design assemble and test the first order butter worth low pass filter and high pass filter.

APPARATUS:

S.NO	NAME OF THE ITEM	RANGE	QUANTITY
1	IC	741	1
2	Resistors	10k Ω ,	1
		1k Ω	1
3	Capacitors	0.01 μ f	1
4	Function Generator	1Mhz	1
5	CRO	20Mhz	1
6	Bread Board		1
7	Fixed Power Supply		1

PROCEDURE:**LPF&HPF First Order:**

1. Connections are made as per the circuit diagram.
2. Apply sinusoidal wave of constant amplitude as the input such that op-amp does not go into saturation.
3. Vary the input frequency and note down the output amplitude at each step
4. Plot the frequency response.

HIGH PASS FILTER (FIRST ORDER)**FREQUENCY RESPONSE:**

TABULAR COLUMN: LPF

Frequency(HZ)	O/P Voltage Vo(p-p)	Gain magnitude, $ v_o/v_i $	Magnitude (dB) = $20\log v_o/v_i $

HPF

Frequency(HZ)	O/P Voltage Vo(p-p)	Gain magnitude, $ v_o/v_i $	Magnitude (dB) = $20\log v_o/v_i $

Applications of filters:

1. In communications systems, use filters to suppress noise, to isolate a single communication from many channels, to prevent spillover of adjacent bands, and to recover the original

message signal from modulated signals.

2. In instrumentation systems, engineers use filters to select desired frequency components or eliminate undesired ones. In addition, we can use these filters to limit the bandwidth of analog signals before converting them to digital signals. You also need these filters to convert the digital signals back to analog representations.
3. In audio systems, engineers use filters in crossover networks to send different frequencies to different speakers. In the music industry, record and playback applications require fine control of frequency components.
4. In biomedical systems, filters are used to interface physiological sensors with data logging and diagnostic equipment.

RESULT:**CONCLUSION:****VIVA QUESTIONS:**

1. List the advantages of active filters over passive filter.

2. Derive f_H of second order LPF.
3. Draw the frequency response for ideal and practical of all types of filters.
4. Design a first order low pass filter for 2 KHz frequency.
5. What are the applications of LPF and HPF?

CIRCUIT DIAGRAM:

Square wave generator:

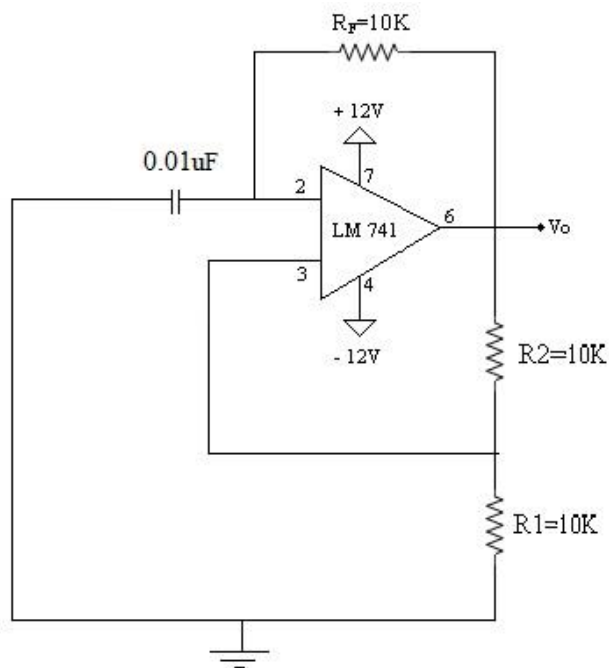


Figure 1

Triangular wave generator:

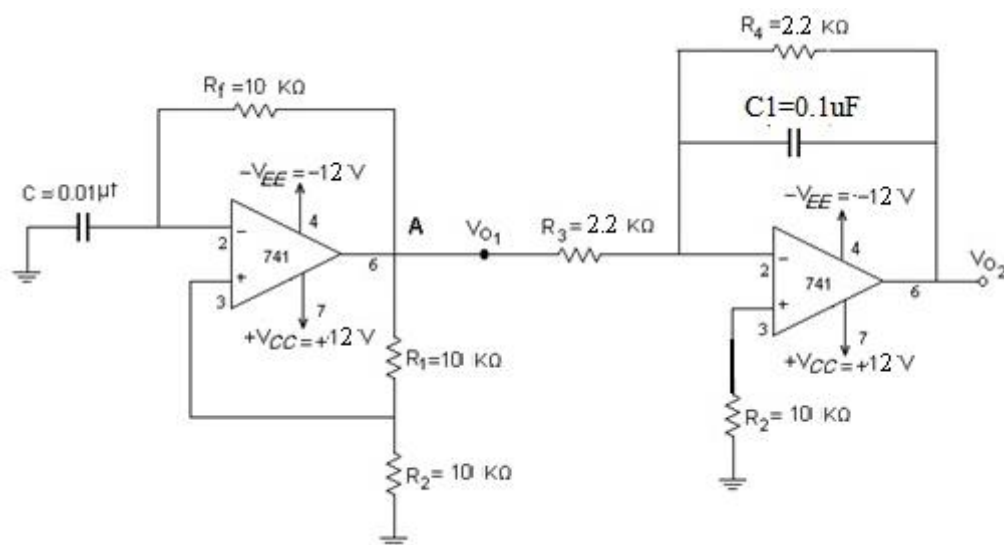


Figure 2

Exp. No:

Date:

WAVEFORM GENERATORS

AIM: To generate square wave and triangular wave form by using 741 OPAMPs.

APPARATUS:

S. No.	Equipment/Component name	Specifications/Value	Quantity
1	IC	741	2
2	Resistors	10k Ω	4
		2.2k Ω	2
3	Capacitor	0.01 μ F	1
		0.1 μ F	1
4	Regulated Power supply	(0 – 30)V	1
5	Cathode Ray Oscilloscope	20MHz	1
6	Connecting wires		-
7	Bread board trainer		1

PROCEDURE:

Square wave generator:

1. Connect the circuit as shown in figure:1
2. Apply the power supplies as $V_{CC} = +12V$ and $V_{EE} = -12V$.
3. Observe the square waveform at the output terminal V_{O1} .
4. Measure the frequency of the oscillations.
5. Compare the Theoretical and Practical frequency values.
6. Plot the output waveform.

Triangular wave generator:

1. Connect the circuit as shown in figure:2
2. Apply the power supplies $V_{CC} = +12V$ and $V_{EE} = -12V$.
3. Observe the square waveform at the output terminal V_{O2} .
4. Measure the frequency of the oscillations.
5. Compare the Theoretical and Practical frequency values.
6. Plot the output waveform.

CALCULATIONS:

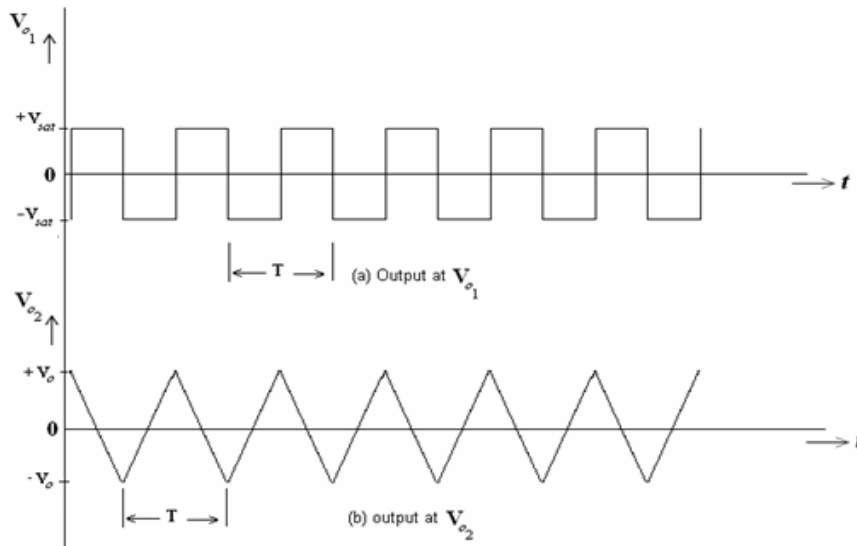
$$frequency = \frac{1}{T}$$

Where T is the time period

$$T = 2RC \left(\ln \left(\frac{1+\beta}{1-\beta} \right) \right) \quad \text{where } R=R_f$$

$$\text{Where, } \beta = \frac{R_2}{R_1 + R_2}$$

MODEL WAVE FORMS:



TABULAR COLUMN:

S. No.	Theoretical		Practical					
			Square wave			Triangular wave		
	Time period T (ms)	Frequency F (KHz)	Time period T (ms)	Frequency F (KHz)	output voltage V_o (V)	Time period T (ms)	Frequency F (KHz)	output voltage V_o (V)

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What are the different types of function generators IC's?

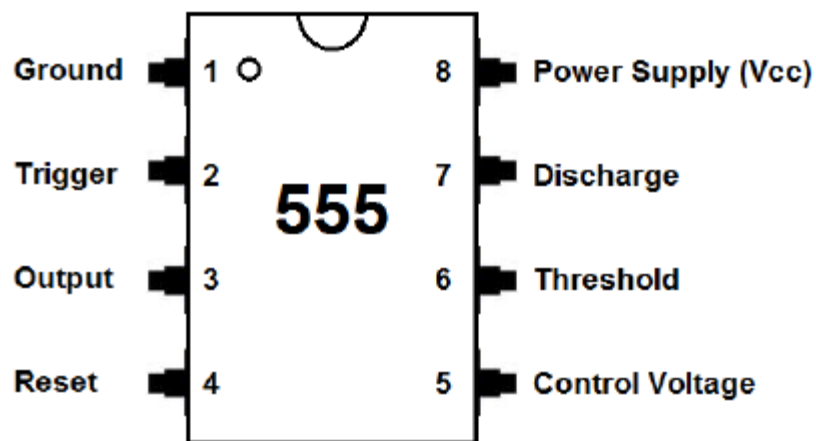
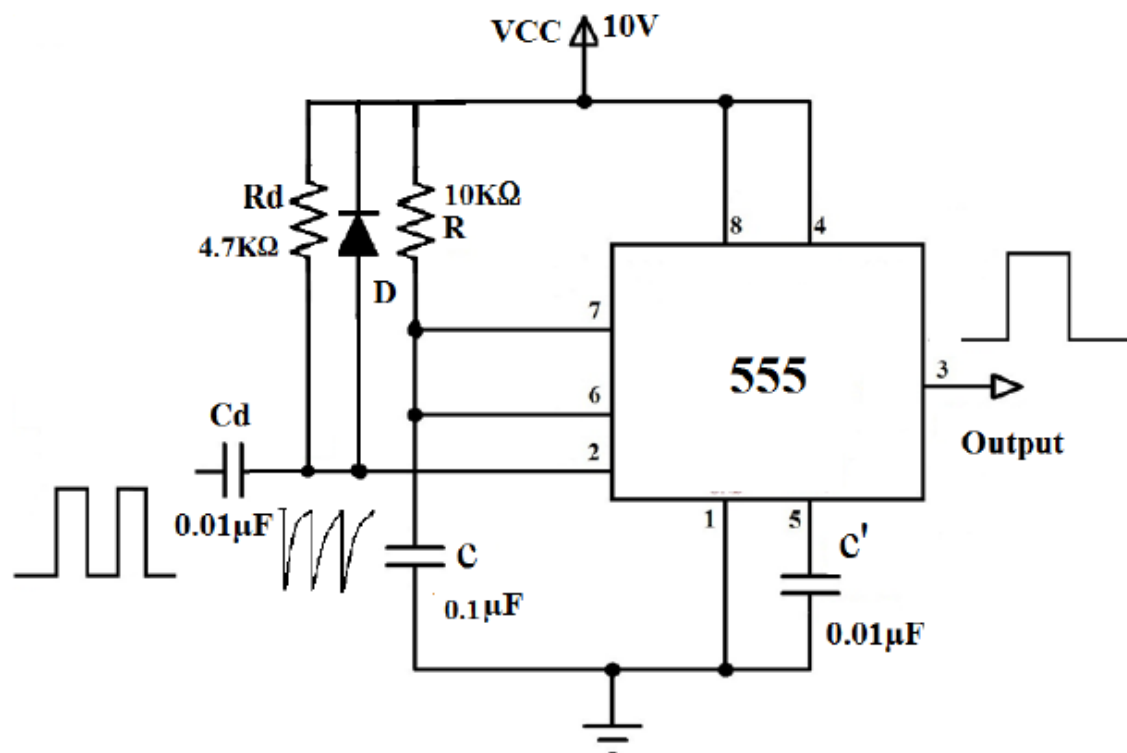
2. What type of output waveforms is obtained from function generator?

3. What is the advantage of using OP-AMP as an oscillator?

4. Why do we call sine to square wave converter as zero crossing detectors?

5. What are the applications of function generator?

PIN DIAGRAM -IC 555:

**CIRCUIT DIAGRAM:****Exp. No:****Date:**

MONOSTABLE MULTIVIBRATOR

AIM: To design and verify the performance of 555 timer under the monostable multivibrator.

APPARATUS:

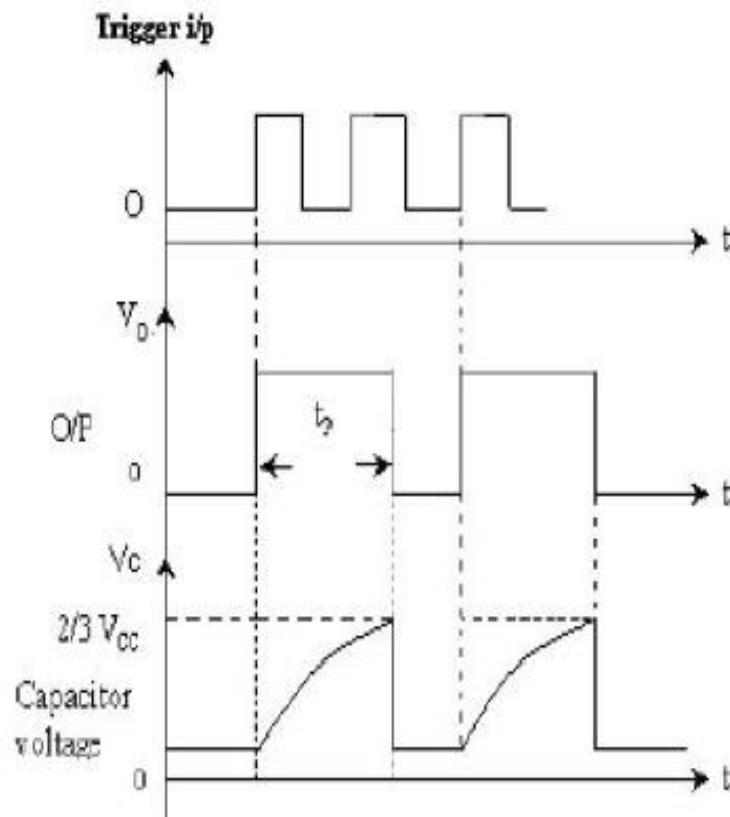
S.NO	NAME OF THE ITEM	RANGE	QUANTITY
1	IC	555	1
2	Resistors	4.7k Ω	1
		10k Ω	1
3	Capacitors	0.1 μ F	1
		0.01 μ F	2
4	Function Generator	1Mhz	1
5	CRO	20Mhz	1
6	Bread Board		1
7	Fixed Power Supply	(0-30V)	1

DESIGN PROBLEMS:

1. design a monostable circuit with T high=12ms
2. design a monostable circuit with T low=12ms

PROCEDURE:

1. Connect the circuit using the component values as obtained in part 4.
2. Apply trigger input with amplitude of 5 volt and at a frequency of 1 KHz and observe the output waveform.
3. Observe and sketch the capacitor voltage waveform (pin – 6) and output waveform (pin – 3).
4. Measure the pulse width of the output waveform and compare with theoretical pulse width.
5. Draw graphs for output waveforms.

EXPECTED WAVEFORMS:**OBSERVATION TABLE:**

S.No	Theoretical value of o/p pulse width (in m.sec). $t_p = 1.1 RC$	Practical value of output pulse width(in m.sec)

Observations:

Trigger input

Amplitude =

Square wave Output signal

Amplitude =

Triangle wave Output signal

Amplitude =

Time period =

Time period =

Time period =

Applications:

1. Frequency divider
2. Pulse width modulation
3. Linear ramp generator
4. Missing pulse detector

RESULT:

.

CONCLUSION:

VIVA QUESTIONS:

1. List the important features of the 555 Timer.

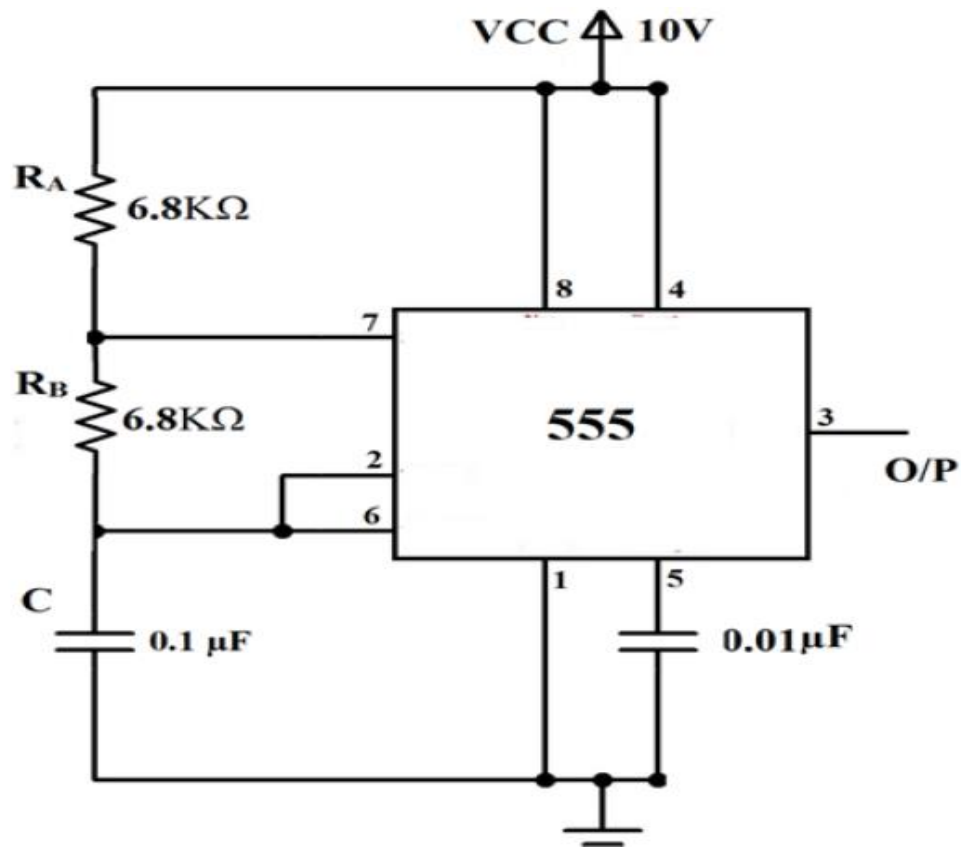
2. What is the function of control input (pin5) of 555 timers?

3. List the applications of 555 timers in Monostable mode.

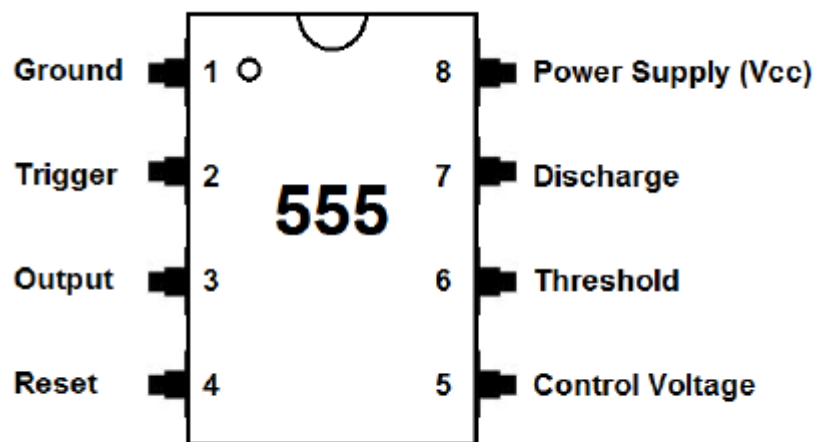
- 4 . Why do we use negative trigger for Monostable operation?

- 5 . Explain the trigger circuit used for Monostable multivibrator?

CIRCUIT DIAGRAM:
ASTABLE MULTIVIBRATOR



PIN DIAGRAM:



Exp. No:**Date:****ASTABLE MULTIVIBRATOR**

AIM: to compare the obtained output frequency and %Duty cycle with the To design a Astable circuit for a given frequency Duty cycle and gien frequency and %Duty cycle by using IC 555 timer.

APPARATUS REQUIRED:

:

S. No.	Equipment/Component	Specifications/Value	Quantity
1	FPS	0-5V	1
2	Dual Trace Oscilloscope	(30 MHz)	1
3	IC 555 timer.	--	1
4	Bread board	--	1
5	Resistors	6.8 k Ω	2
6	Capacitors	0.1 μ F	1
		0.01 μ F	1

PROCEDURE:

1. Check the components.
2. Setup the symmetric astable multivibrator circuit on the breadboard and check the connections.
3. Switch on the power supply.
4. Observe output and capacitor voltage on different channels of the oscilloscope simultaneously.
5. Draw the waveforms on the graph.
6. Measure the frequency of oscillation and duty cycle .
7. Repeat the procedures for asymmetric astable multivibrator.

PRECAUTIONS:

- 1) Keep current knob of power supply in maximum position.
- 2) Check the op amp before connections.
- 3) Avoid loose contacts.
- 4) Avoid parallax error while observing output in CRO.

OBSERVATION TABLE:

S.NO	Theoretical Values					Practical Values				
	t_c (m.sec)	t_d (m.sec)	T (m.sec)	f (in Hz)	D	t_c (m.sec)	t_d (m.sec)	T (m.sec)	F (inHz)	D

DESIGN PROCEDURE:

$$T = 0.69 (R_A + 2R_B) C \text{ or } f = 1.44 / \{ (R_A + 2R_B) C \}, \text{ Here } T = T_1 + T_2$$

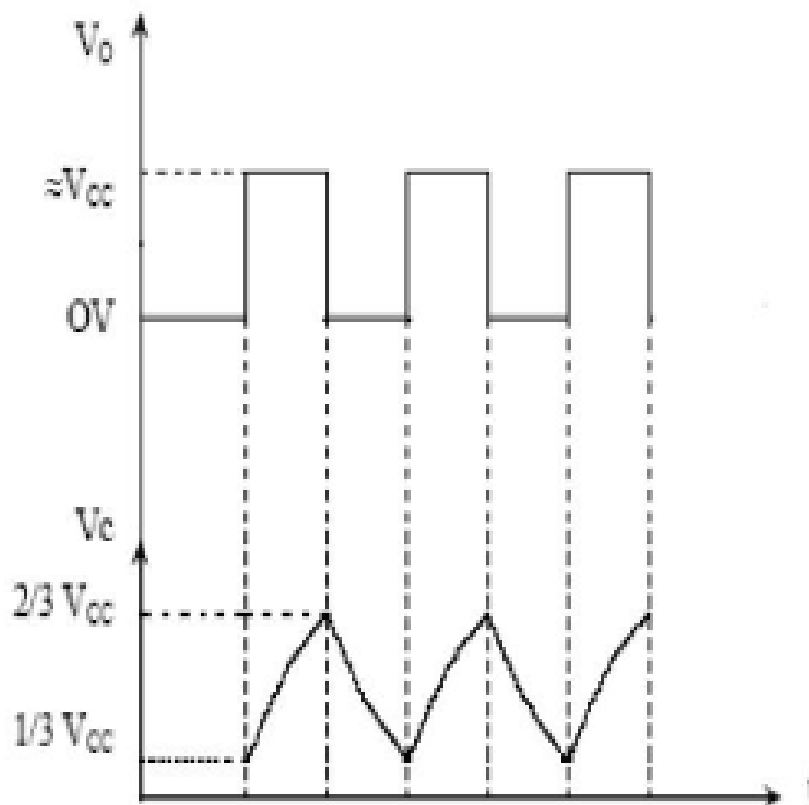
$$T_1 = 0.69(R_A + R_B)C \text{ (charging)}$$

$$T_2 = 0.69(R_B)C \text{ (discharging)}$$

$$\text{Let } T_1 = 1\text{ms} ; T_2 = 0.5\text{ms} ; C = 0.1 \text{ Mf}, 0.69 R_B C = 0.5\text{ms}$$

$$R_B = 7.2 \text{ K}\Omega = 6.8\text{K}\Omega \text{ (std)}, 0.69 (R_A + R_B) C = 1\text{ms}$$

$$R_A + R_B = 14.49 \text{ K}\Omega, R_A = 14.49 - R_B, R_A = 7.2 \text{ K}\Omega = 6.8\text{K}\Omega$$

MODELWAVEFORM:

RESULT:

CONCLUSION:

VIVA QUESTIONS:

- 1). What is difference between oscillator and Multivibratort?

- 2). How many stable states are present in a Astable multivibrator circuit?

- 3) Write the expression for frequency and % Duty cycle in a Astable multivibrator circuit?

4) Write any three applications of a Astable multivibrator circuit?

5) Can a Astable multivibrator circuit be used to produce Sinusoidal waveforms. Why?

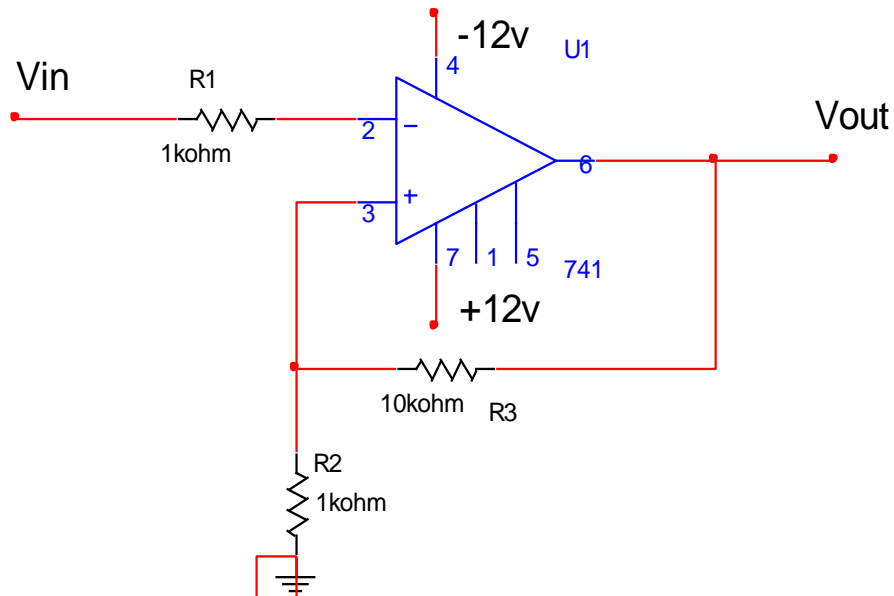
CIRCUIT DIAGRAM**SCHMITT TRIGGER**

Fig : Circuit diagram of schmitt trigger using IC 741

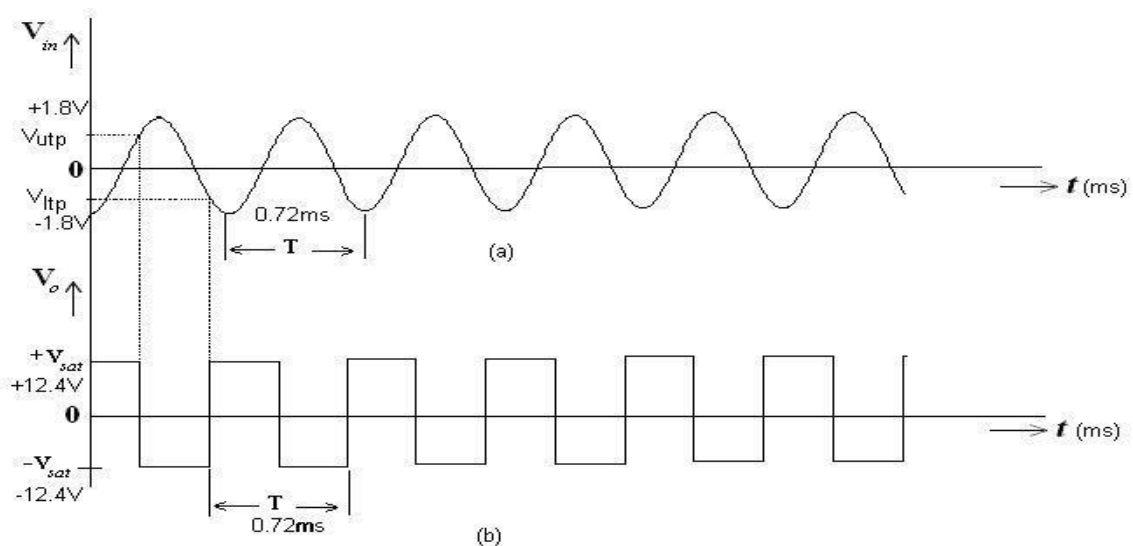
WAVE FORMS OF SCHMITTH TRIGGER:

Fig: Expected input and output waveforms of Schmitt trigge

Exp. No:**Date:****SCHMITT TRIGGER****AIM:** To construct and study the Schmitt Trigger using IC741 and IC 555 Operational Amplifiers**APPARATUS :**

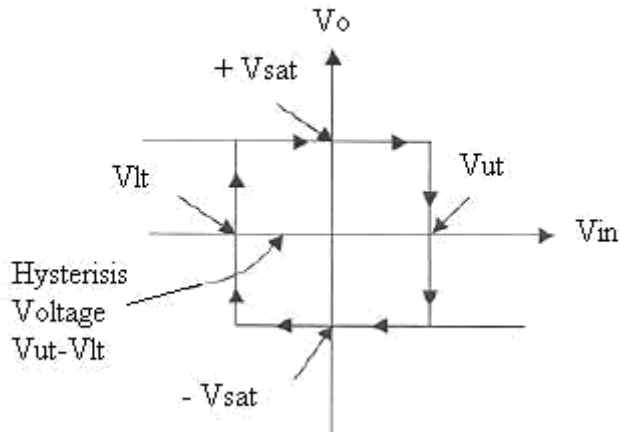
S.NO	NAME OF THE ITEM	RANGE	QUANTITY
1	IC	741	1
2	Resistors	10 K Ω	1
		1k Ω	2
3	Function Generator	1Mhz	1
4	CRO	20Mhz	1
5	Bread Board	-	1
6	Fixed Power Supply	(0-30V)	1

PROCEDURE:

1. Connect the circuit as shown Fig.
2. Set Function Generator output for sine wave signal of Amplitude at 1V(p-p) & frequency 1KHz.
3. Set R1 and R2 values at fixed positions and note down the values in tabular column.
Calculate theoretical values of V_{ut} and V_{lt} and note down the values in tabular column.
($+V_{sat} = 14V$, $-V_{sat} = -14V$).
4. Apply Function Generator output at input terminals V_i , connect C.R.O- CH2 at output terminals V_o , C.R.O-CH1 at input terminals V_i .
5. Observe square wave output on C.R.O for the given input sine wave & compare them with the sample waveform as shown in fig.2.
6. Note down the practical V_{ut} , V_{lt} and V_H values in tabular column.
7. Compare the theoretical and practical values of V_{ut} , V_{lt} and V_H

Hysteresis Graph

V_o versus V_{in} plot of Hysteresis Voltage



TABULAR COLUMN:

S.No	Theoretical Values				Practical value	
	R_1	R_2	$V_{ut} = \frac{R_1}{R_1 + R_2} (+V_{sat})$	$V_{lt} = \frac{R_1}{R_1 + R_2} (-V_{sat})$	V_{ut}	V_{lt}
1						
2						
3						

Observations for Schmitt trigger using IC 741:

Input signal

Amplitude =

Time period =

Output signal

Amplitude =

Time period =

Applications:

1. on/off controllers
2. Used as a comparator

RESULT:

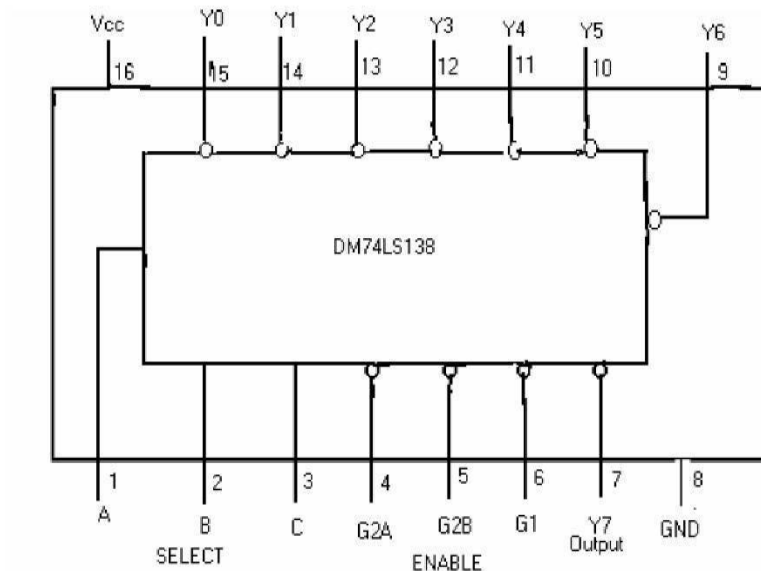
CONCLUSION:

VIVA QUESTIONS:

1. How can a comparator be converted to Schmitt trigger
2. What do you mean by the Phenomenon hysteresis or backlash?
3. Why do we call Schmitt trigger as square wave generator.
4. What are the applications of Schmitt trigger?
5. Design a Schmitt trigger with an $UTP = 3V$ and $LTP = 5V$ and an input voltage of $10v$.

PART-II

DIGITAL IC EXPERIMENTS

PIN DIAGRAM:Truth Table: -

INPUTS						OUTPUTS							
ENABLES													
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
0	x	x	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

Exp. No:**Date:****3 TO 8 DECODER-74LS138****AIM:** To verify operation of the 3 to 8 decoder using IC 74138.**APPARATUS:**

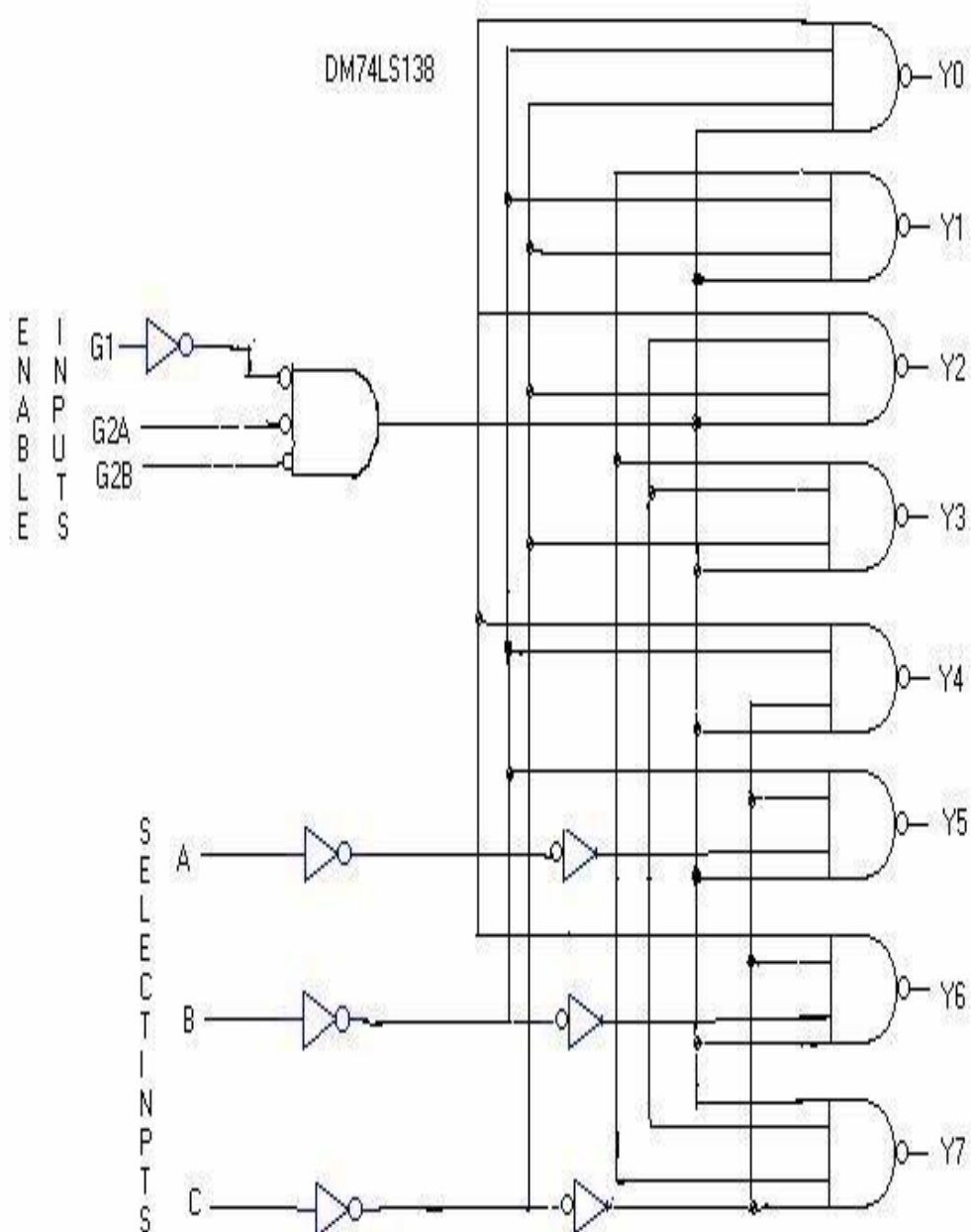
S.NO	APPARATUS	IC NUMBER	QUANTITY
1	IC	74LS138	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

A decoder is a combinational circuit that connects the binary information from 'n' input lines to a maximum of 2^n unique output lines. The IC 74138 accepts three binary inputs and when enable provides 8 individual active low outputs. The device has 3 enable inputs. Two active low and one active high.

PROCEDURE:-

1. Make the connections as per the circuit diagram.
2. Change the values of G1, G2A, G2B, A, B, and C, using switches.
3. Observe status of Y0, to Y7 on LED's.
4. Verify the truth table.

LOGIC DIAGRAM:

RESULT:-

CONCLUSION:

VIVA QUESTIONS:

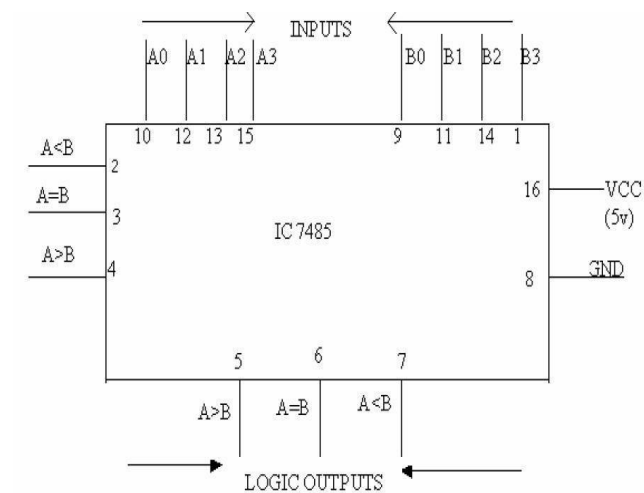
1. What do you understand by decoder?

2. What is de-multiplexer?

3. What do you understand by encoder?

4. What is the main difference between decoder and demultiplexer?

5. Why Binary is different from Gray code?

LOGIC DIAGRAM:**TRUTH TABLE:**

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

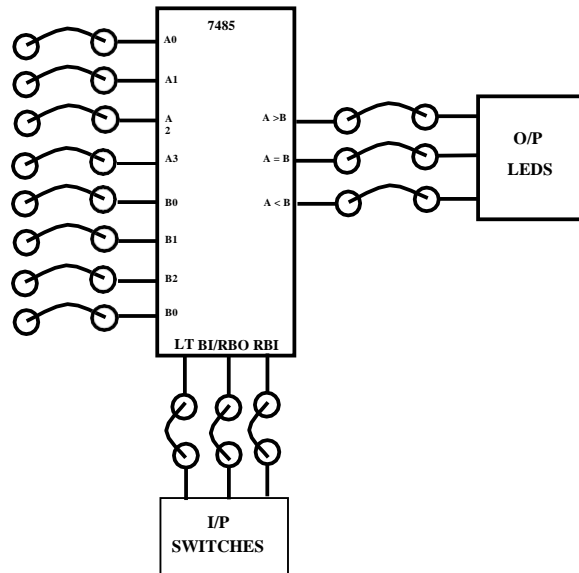
H = High Level, L = Low Level, X = Don't Care

Exp. No:**Date:****4 - BIT COMPARATOR 74LS85****AIM:-** To study the operation of 4-bit Magnitude Comparator using Ic7485.**APPARATUS:-**

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	74LS85	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

PROCEDURE:

1. Do the connection as per block diagram shown below and switch ON the power supply.
2. Give step by step inputs to A & B of comparator starting from MSB (A3 and B3).
3. Initially just observe the comparison between inputs A & B inputs and ignore the cascading inputs.
4. Once all possible combinations for A & B inputs are over then apply cascading inputs as per function table. Observe the outputs of comparator and verify it with function table.
5. Cascading inputs are used to increase the input line capacity of comparator.

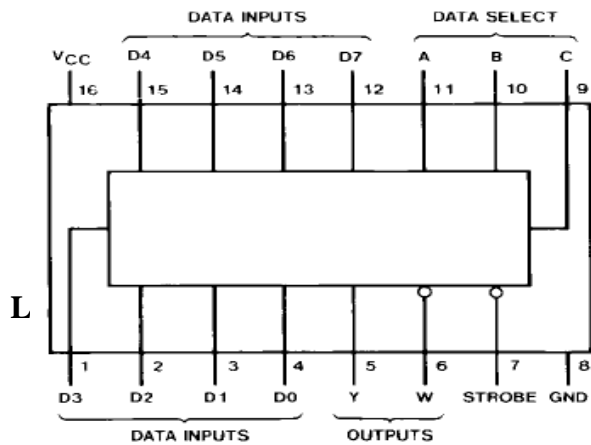
LOGIC DIAGRAM CONNECTIONS:

RESULT:-

CONCLUSION:

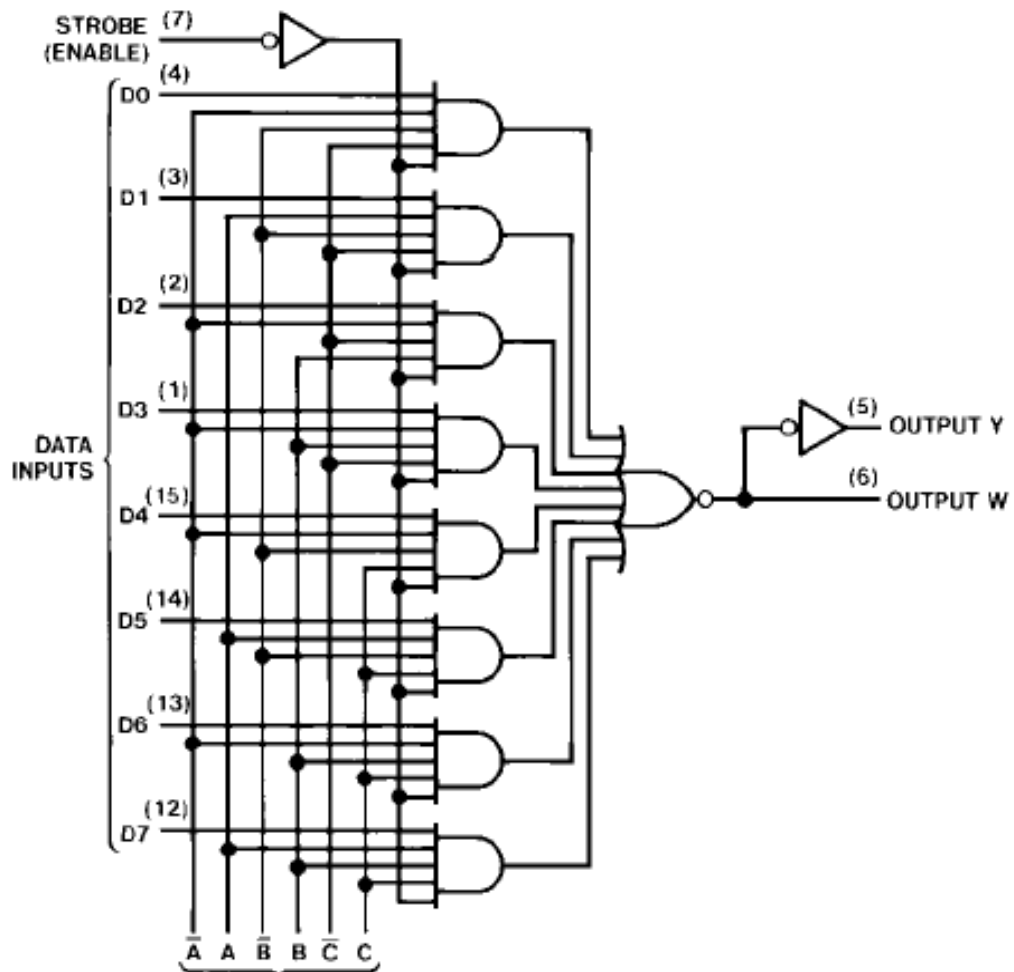
VIVA QUESTIONS:

1. What is a comparator?
2. What are the applications of comparator?
3. Derive the Boolean expressions of one bit comparator and two bit comparators.
4. How do you realize a higher magnitude comparator using lower bit comparator
5. Design a 2 bit comparator using a single Logic gates?

74LS151 MULTIPLEXER:**LOGIC SYMBOL****TRUTH TABLE**

Inputs				Outputs	
Select			Strobe S	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = HIGH Level
L = LOW Level
X = Don't Care
D0, D1...D7 = the level of the respective D input



Exp. No:**Date:****8X1 MULTIPLEXER-74X151 & 2X4 DEMULTIPLEXER-74X155**

AIM: To construct multiplexer and de-multiplexer circuits using IC-74X151 and IC-74X155 respectively.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	74151	1
		74155	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

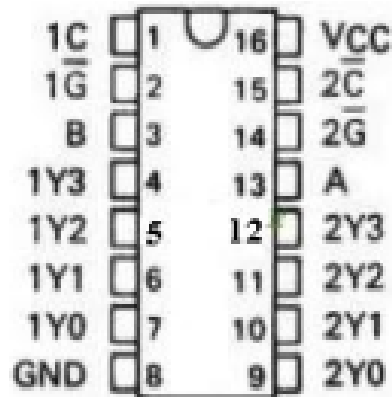
The multiplexers contains full on-chip decoding unit to select desired data source. The 74151 selects one-of-eight data sources. It has a enable input which must be at a LOW logic level to enable these devices. These perform parallel-to-serial conversion. The 74150 selects one-of sixteen data sources.

The 74155 sends the data source to one of four data destinations. It has a enable input which must be at a LOW logic level to enable these devices.

The binary decoder with enable input connected to data line known as De multiplexer.

PROCEDURE:

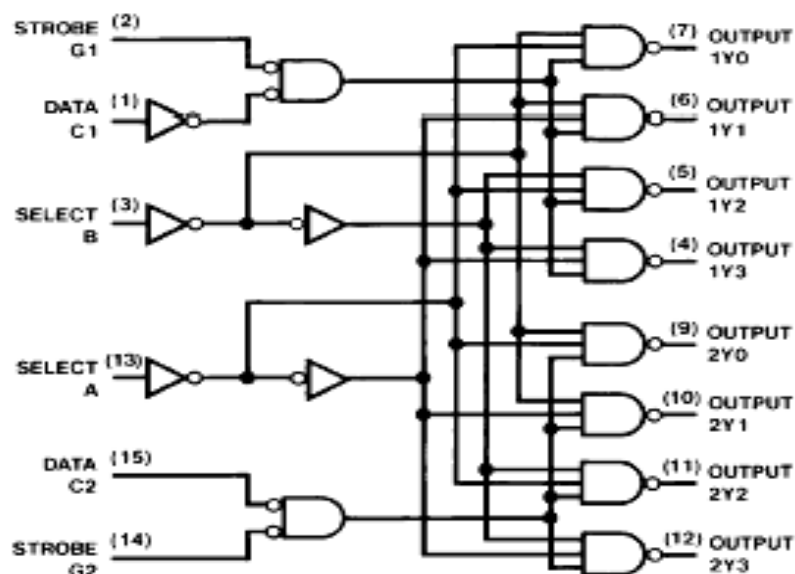
1. Connections are made as per the logic diagram.
2. Apply +5V for Vcc & 0V for GND
3. Outputs will be verified for different combinations of inputs.

2X4 DEMULTIPLEXER:**PIN DIAGRAM**

:

FUNCTIONAL TABLE

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

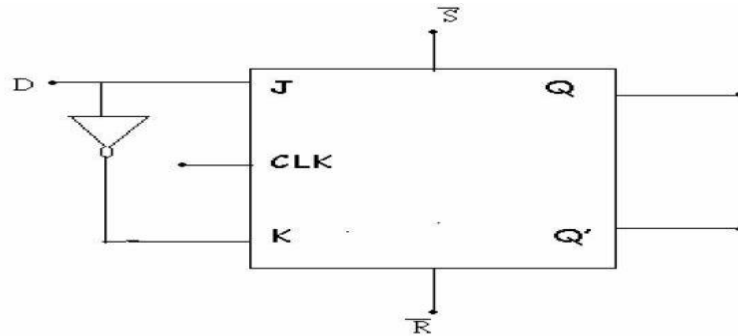
**LOGIC DIAGRAM
FOR 2X4 DEMUX**

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What are the different methods to obtain minimal expression?
2. What is a Min term and Max term?
3. State the difference between SOP and POS?
4. How do you realize a given function using multiplexer?
5. What is a multiplexer?

D-Flip -Flop:**D-flip-flop using Nand gates :**

S'	R'	CLOCK	D	Q	Q'	COMMENT
0	0	X	X	1	1	Race
0	1	X	X	1	0	Set
1	0	X	X	0	1	Reset
1	1		1	1	0	Data Transfer
1	1		0	0	1	Data Transfer

Truth Table - 3

R

TRUTH TABLE:

S'	R'	CLOCK	D	Q	Q'	COMMENT
0	0	X	X	1	1	Race
0	1	X	X	1	0	Set
1	0	X	X	0	1	Reset
1	1		1	1	0	Data Transfer
1	1		0	0	1	Data Transfer

Truth Table - 3

Exp. No:

Date:

D, JK FLIP FLOPS**AIM:** To verify the truth table of D, JK Flip Flops**APPARATUS:-**

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	7474,7476	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

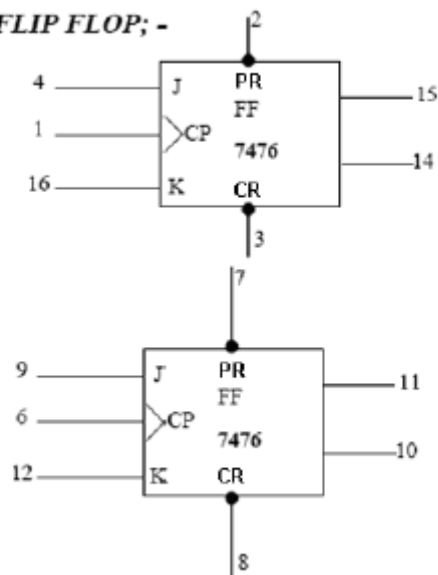
PROCEDURE:**D Flip-Flop:**

1. Do the connection for T Flip-Flop as shown in above.
2. Connect PR to **PRESET**, CR to **CLEAR** and T terminals to the logic input switch.
3. Connect the CLK of T Flip-Flop to CLOCK terminal.
4. Connect Q and /Q terminals to LED indicators in O/P LED section.
5. Set the PR, CR, CLK and T Signals by means of the switches as per the truth table of T flipflop given Above and verify the Q and /Q outputs.

J-K Flip-Flop:

1. Connect PR to **PRESET**, CR to **CLEAR** and J and K terminals to the logic inputSwitches
2. Connect CLK of JK flip-flop to Clock terminal.
3. Connect Q and /Q terminals to LED indicators in O/P section.
4. Set the PR, CR, CLK, J and K Signals by means of the switches as per the truth table of JK flip-flop given above and verify the Q and /Q outputs by changing possible input condition

IC 7476 JK FLIP FLOP; -



TRUTH TABLE FOR JK-FLIP FLOP (IC 7476); -

SD Preset	CD Clear	Clock	J	K	OUTPUTS	
					Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	\bar{Q}_0

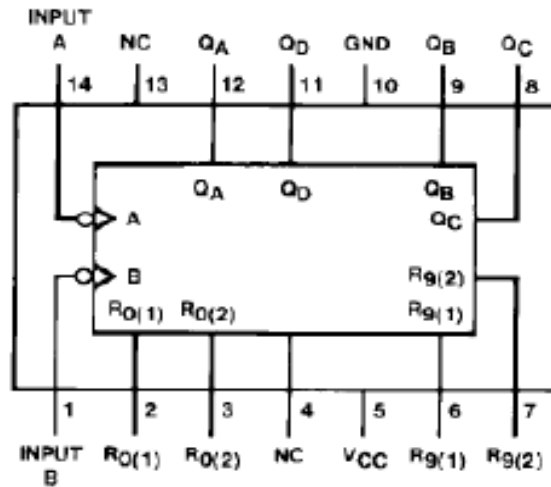
*Unstable condition. It will not remain after C_n and P_n inputs return to their inactive (high) state

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What is flip-flop?
2. How many types of flip-flop are used?
3. What are the characteristic equation for T flip-flop?
4. What is full form of T flip-flop?
5. Which Gates are used in SR flip flops to a JK flip-flop?

DECADE COUNTER 74LS90**PIN DIAGRAM:-**

1) BCD Count sequence when O/P Q_A is connected to input B for BCD count.

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

2) BCD Count sequence when O/P Q_D is connected to input A for Bi-quinary count

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Exp. No:

Date:

DECADE COUNTER 74LS90**AIM:** To construct and verify the working of a single digit decade counter using IC 7490.**APPARATUS:**

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC74LS90	1
2	Digital IC Trainer Kit		1
3	Patch card		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

The 7490 monolithic counter contains four master slave flip-flops and additional gating to provide a divide-by two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The counter has a gated zero reset and also has gated set to nine inputs for used in BCD nine's complement applications.

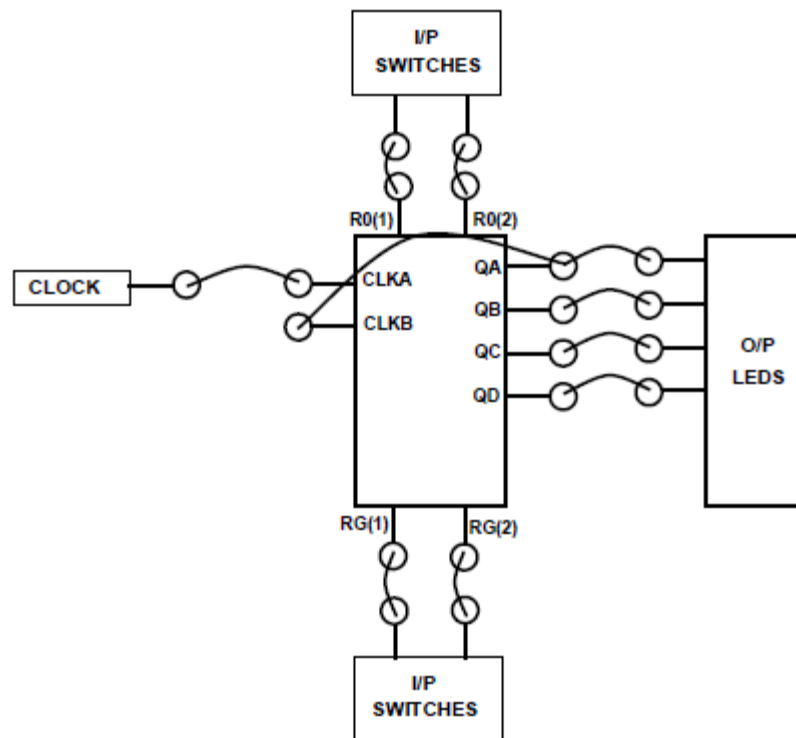
To use the maximum count length (decade or four-bit binary), the B input is connected to the QA output. The input count pulses are applied to input A and the outputs are as described in the appropriate Function Table.

A symmetrical divide-by-ten count can be obtained from the counters by connecting the QD output to the A input and applying the input count to the B input which gives a divide by- ten square wave at output QA.

RESET/ COUNT function table

Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

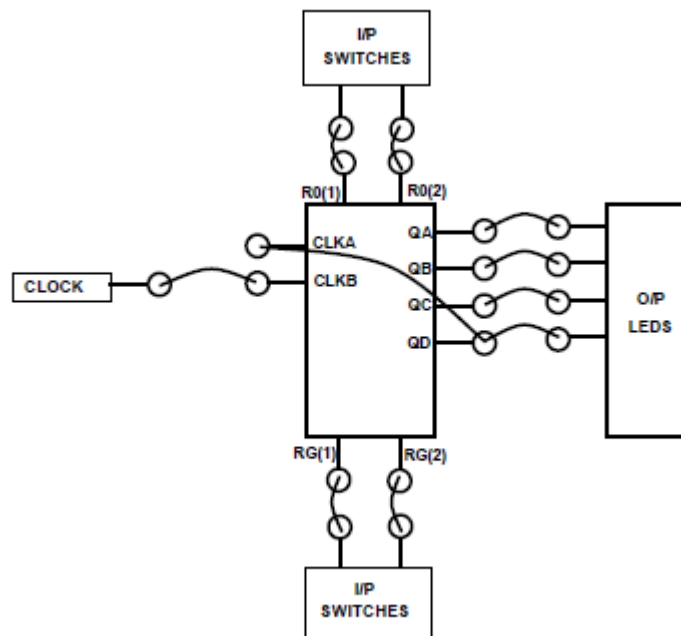
H = HIGH Level
L = LOW Level
X = Don't Care

**PROCEDURE:**

1. Do the connection as shown in block diagram above and switch ON the power supply.
2. Provide the proper logic inputs to R0 (1), R0 (2), RG (1) and RG (2) by referring its RESET/ COUNT function table.
3. Now provide Clock pulse one at a time by pressing Clock switch & observe the led indication at O/P section. It should be as shown in table.

SR NO	CLOCK PULSES	OUTPUTS			
		QD	QC	QB	QA
1	1	0	0	0	0
2	2	0	0	0	1
3	3	0	0	1	0
4	4	0	0	1	1
5	5	0	1	0	0
6	6	0	1	0	1
7	7	0	1	1	0
8	8	0	1	1	1
9	9	1	0	0	0
10	10	1	0	0	1

4. Once the count reached to 1001 counter resets to 0000. That means it count 10 clock pulses and counter advances its counts by ten. The 7490 can be configured in following mode also.

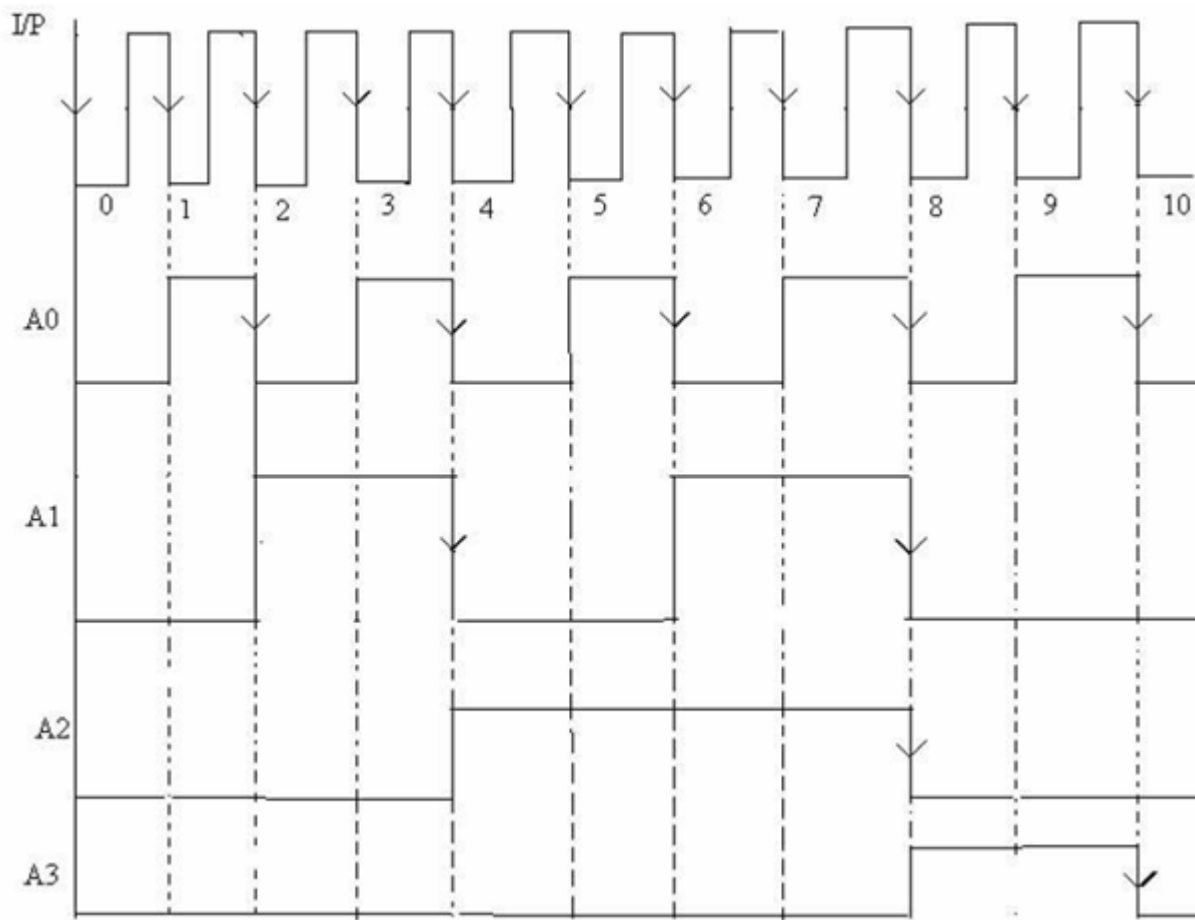


5. Do the connection as shown in block diagram above
6. Provide the proper logic inputs to R0 (1), R0 (2), RG (1) and RG (2) by referring its RESET/ COUNT function table.
7. Now provide Clock pulse one at a time by pressing Clock switch & observe the LED Indication at O/P section. It should be as shown in table.

SR NO	CLOCK PULSES	OUTPUTS			
		QA	QD	QC	QB
1	1	0	0	0	1
2	2	0	0	1	0
3	3	0	0	1	1
4	4	0	1	0	0
5	5	1	0	0	0
6	6	1	0	0	1
7	7	1	0	1	0
8	8	1	0	1	1
9	9	1	1	0	0
10	10	0	0	0	0

8. In this case counter output is not in sequence as in earlier case. Once the count reached to 1100 counter resets to 0000. That means it count 10 clock pulses.

WAVE FORMS:



RESULT:

CONCLUSION:

VIVA QUESTIONS:

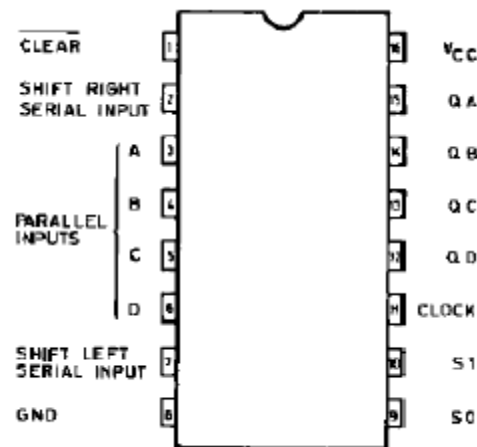
1. Define counter, mention some application?

2. What is the difference between ring counter and Johnson counter?

3. What is the other name for decade counter?

4. How many states are there in decade counter?

5. How many flip-flops are needed for a decade counter?

UNIVERSAL SHIFT REGISTER**PIN DIAGRAM of 74194****TRUTH TABLE**

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X		X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H		X	X	a	b	c	d	a	b	c	d
H	L	H		X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H		X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L		H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L		L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

X: Don't Care : Don't Care

a ~ d : The level of steady state input voltage at input A ~ D respectively

QA0 ~ QD0 : No change

QAn ~ QDn : The level of QA, QB, QC, respectively, before the most recent positive transition of the clock.

Exp. No:

Date:

UNIVERSAL SHIFT REGISTER-74LS194**AIM:** - To study the following applications of the Universal shift register using IC 74194.

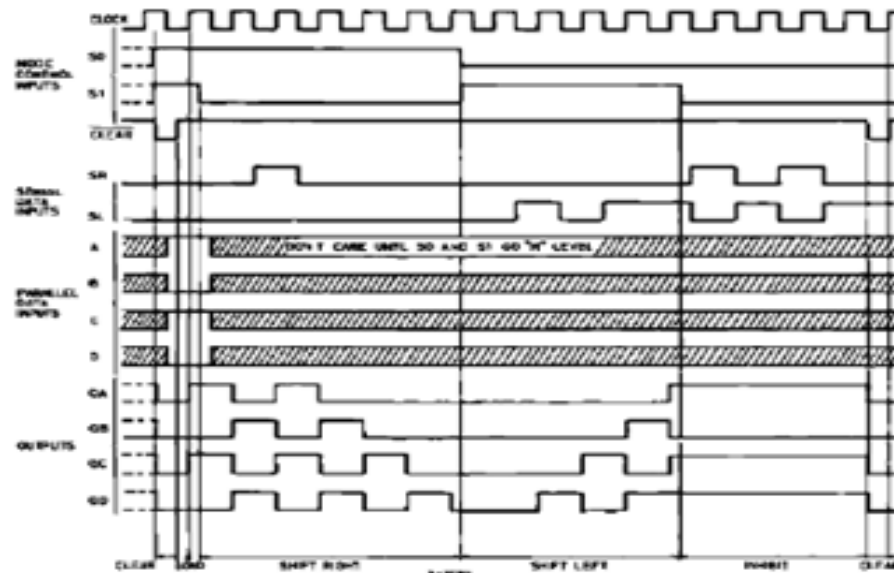
- a. Left Shift Register
- b. PIPO mode
- c. Right Shift Register

APPARATUS:-

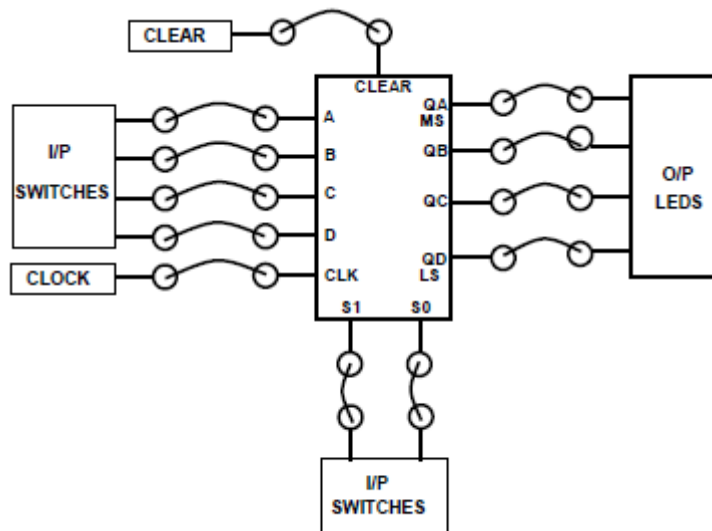
S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC74LS194	1
2	Digital IC Trainer Kit		
3	Patch card		REQUIRED
4	Fixed Power Supply	(0-5V)	1

PROCEDURE:**a) Left Shift Register**

1. Do the connection as per Right Shift register.
2. Set $S_1 = '1'$, $S_0 = '0'$, $SL = '1'$ and $SR = X$. Connect Clear of Shift Register to CLEAR terminal.
3. Connect outputs QA to QD of reg. to LED indicators.
4. Switch on the power supply. All Led indicators are in OFF positions.
5. Now give clock signal to Shift register by CLOCK terminal and observe the LED indication. The led indication should follow the sequence as shown in table
6. From the above function table we can conclude that this register work as Left shift register as it shifts '1' towards left by one position at every clock pulse.
7. To start the counting again or to reset the register press CLEAR.



PIN DIAGRAM OF PIPO mode:



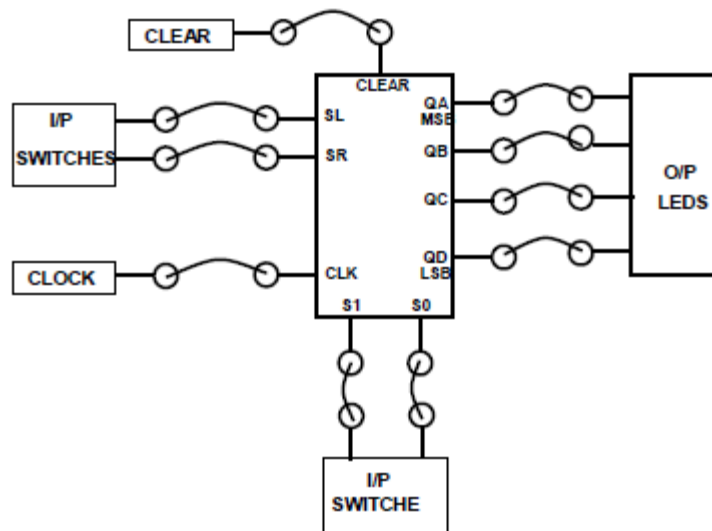
PROCEDURE:

b) PIPO mode

1. Do the connection as shown in block diagram above.
2. Set ABCD = 1010 using logic switches. Set S1 = S0 = '1' or Logic HIGH, connect Clear of Shift reg. to CLEAR terminal
3. Connect outputs QA to QD of reg. to LED indicators.
4. Switch on the power supply. All Led indicators are in OFF positions.
5. Now give clock signal to Shift register by CLOCK terminal, as soon as clock is reached to Reg. led indicators will show 1010, which is the input we have set for register.
6. Now change the data at input side using I/P switches & press clock switch, LED Indication now displays the new data. It means this shift register works as parallel in parallel out under clock signal control.

c) Right Shift Register

1. Do the connection as per block diagram shown below,
2. Set S1 = '0', S0 = '1', SL = X, SR = '1'. Connect Clear of Shift Reg. to CLEAR Terminal
3. Connect outputs QA to QD of reg. to LED indicators.
4. Switch on the power supply. All Led indicators are in OFF positions.
5. Now give clock signal to Shift register by CLOCK terminal and observe the LED indication. The led indication should follow the sequence as shown in table.
6. From the above function table we can conclude that this register work as right shift register as it shifts '1' towards right by one position at every clock pulse.
7. To start the counting again or to reset the register press CLEAR.

PIN DIAGRAM OF RIGHT SHIFT REGISTER**TRUTH TABLE:****RIGHT SHIFT REGISTER**

SR	CLOCK	Q _A	Q _B	Q _C	Q _D	O/P
1	0	0	0	0	0	0
2	1	1	0	0	0	8
3	2	1	1	0	0	12
4	3	1	1	1	0	14
5	4	1	1	1	1	15

LEFT SHIFT REGISTER

SR	CLOCK	Q _A (MSB)	Q _B	Q _C	Q _D	O/P in DEC
1	0	0	0	0	0	0
2	1	1	0	0	1	1
3	2	1	0	1	1	3
4	3	1	1	1	1	7
5	4	1	1	1	1	15

RESULT:-

CONCLUSION:

VIVA QUESTIONS:

1. What do you mean by shift register?

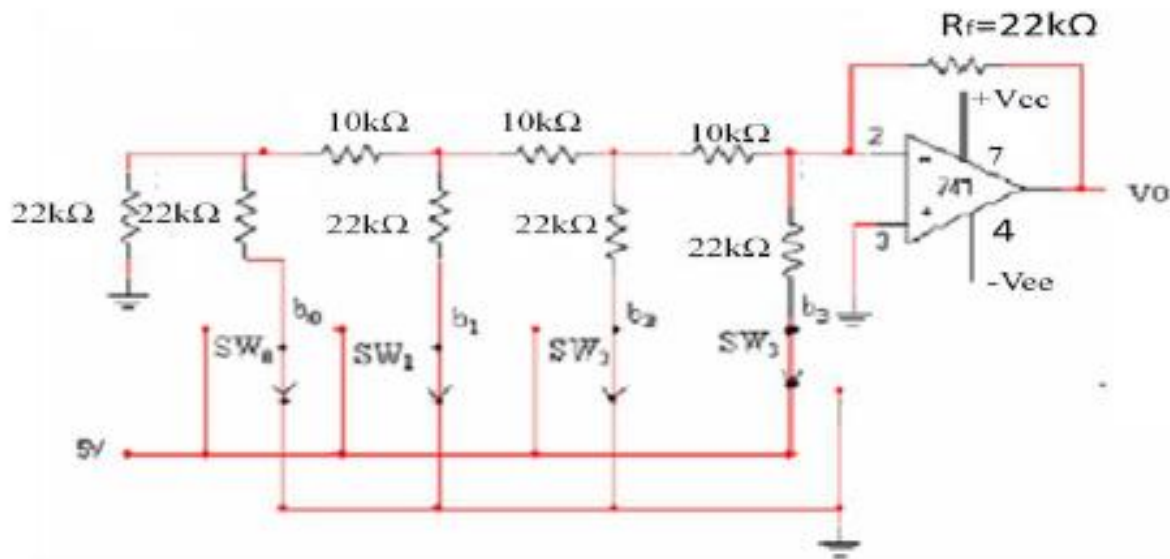
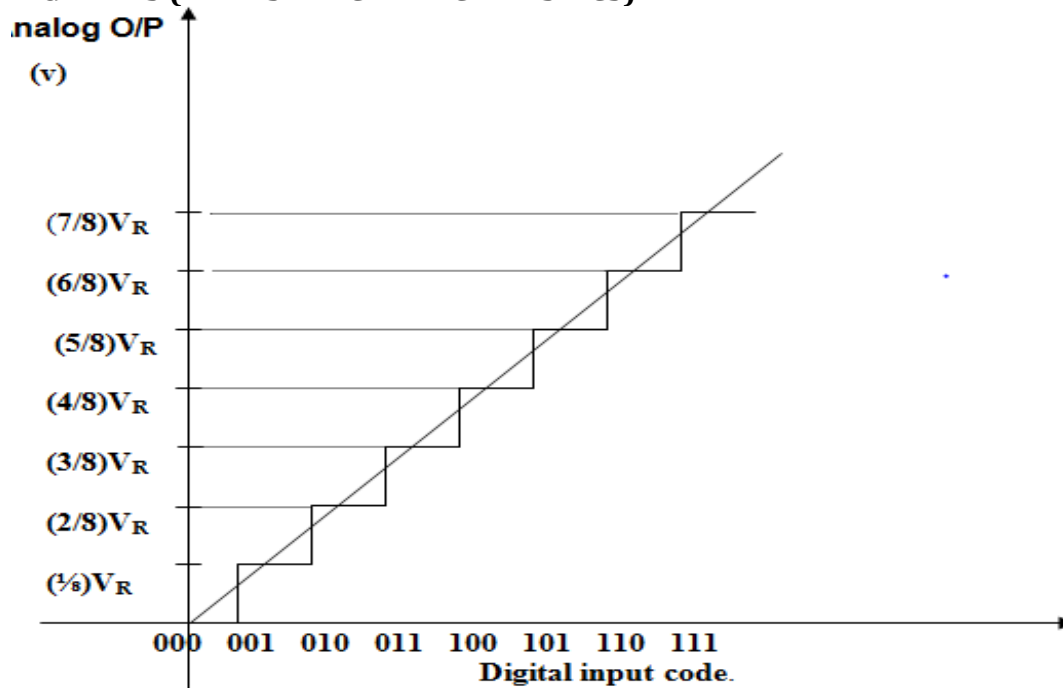
- 2.Explain the operation of a left shift register & a right shift register?

- 3.What is the difference between a register and shift register?

- 4.What is meant by universal shift register?

5. Explain the various modes in which the data can be entered or taken out from a register?

Additional Experiments

CIRCUIT DIAGRAM:***R- 2R LADDER TYPE DAC:*****EXPECTED GRAPHS (TRANSFER CHARACTERISTICS):**

Exp. No:

Date:

4-BIT DAC USING OP-AMP

AIM: To design and simulate the 4-bit DAC using R-2R ladder type technique and also by using Binary To method by using OP AMP with multisim software.

APPA RATUS REQUIRED:

S. No.	Equipment/Component	Specifications/Value	Quantity
1	IC	741	1
2	Resistors	10 k Ω	3
		22k Ω	6
3	Regulated Power supply	(0 – 10)V	1
4	Function Generator	(0 – 3MHz), 20V _{p-p}	
5	Cathode Ray Oscilloscope	20MHz	1
6	Connecting wires		-

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Apply proper biasing voltages to the pin 4 and pin 7.
3. Measure the output voltages for all the binary input combinations using a DMM.
4. Plot the graph of binary input voltage verses analog output voltage.
5. Measure the size of each step and hence calculate resolution which is given by $[V_{ES}/2^{n-1}]$.

TABULAR COLUMN:**USING R-2R LADDER METHOD**

S.No	DIGITAL INPUT				Analog output (V)
	B ₀	B ₁	B ₂	B ₃	
1	0	0	0	0	
2	0	0	0	1	
3	0	0	1	0	
4	0	0	1	1	
5	0	1	0	0	
6	0	1	0	1	
7	0	1	1	0	
8	0	1	1	1	
9	1	0	0	0	
10	1	0	0	1	
11	1	0	1	0	
12	1	0	1	1	
13	1	1	0	0	
14	1	1	0	1	
15	1	1	1	0	
16	1	1	1	1	

RESULT:

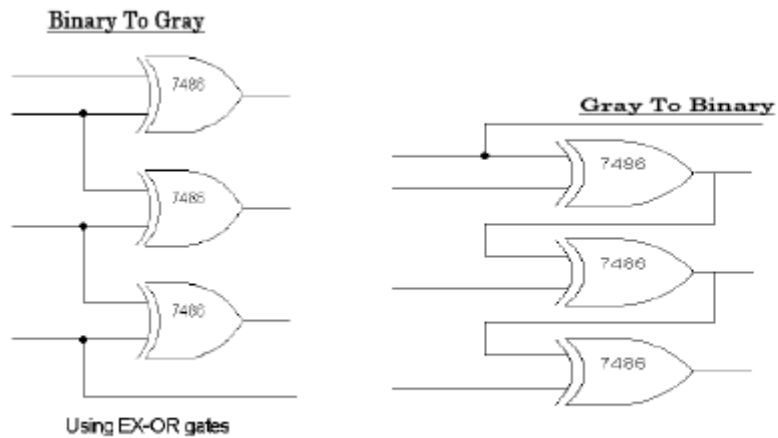
CONCLUSION:

VIVA QUESTIONS:

1. What are ADC's and DAC's?
2. Define Resolution?
3. What are the different types of ADC's?
4. What are the different types of DAC's?
5. Which is the fastest ADC?

Binary to Gray and Gray to Binary Conversion

Logic diagram of Binary to Gray Logic diagram of Gray to Binary code conversion



TRUTH TABLE:

Inputs				Outputs			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Exp. No:

Date:

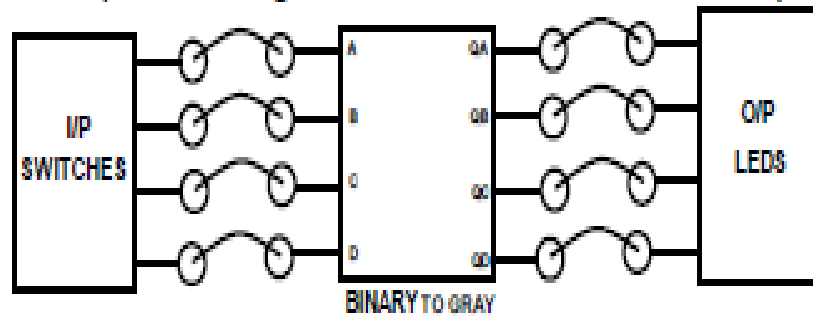
BINARY TO GRAY&GRAY TO BINARY**AIM:-** To study of Binary to Gray, Gray to Binary Convertors.**APPARATUS: -**

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	74LS86	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5V)	1

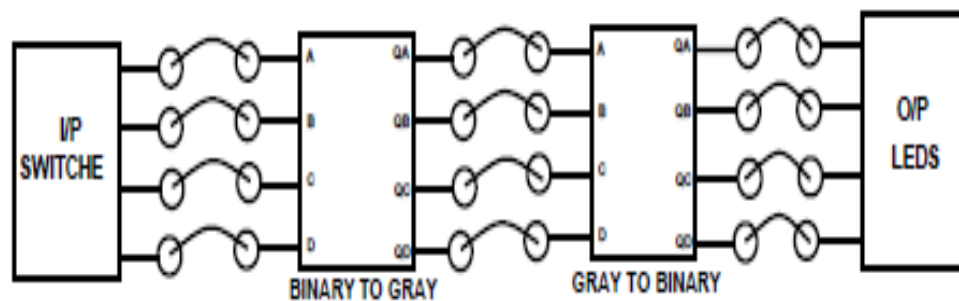
PROCEDURE:

1. Do the connections as per block diagram shown below and switch on the power supply
2. Apply logic inputs to the block diagram from I/P switches and observe the corresponding generated code on LEDs at O/P section Verify the truth table for binary to gray code conversion.
3. For Gray to Binary do the connection as shown below.
4. Apply logic inputs to the block diagram from I/P switches and observe the corresponding generated code on LEDs at O/P section.
5. Verify the truth table for Gray to Binary code conversion.

Binary to Gray:



Binary to Gray and Gray to Binary:



RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. How many types of code converters are there?
2. Which gate is mostly used in code converter circuits?
3. What is the conversion of Gray code 1100 to binary?
4. What is the Gray code for the binary code 11010?
5. What is the need of code converters?