LINEAR IC APPLICATIONS (15A05402)

LECTURE NOTES

B.TECH

REGULATION:R15

III-YEAR & I-SEM

Prepared by:

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B. Tech III-ISem. (ECE)

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15A04503 LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

Course Objectives:

- Design of OPAMPS, Classification of OPAMPs.
- To study and design various linear applications of OPAMPs.
- To study and design various non linear applications of OPAMPs

Course Outcomes:

- Understand the basic building blocks of linear integrated circuits and its characteristics.
- Analyze the linear, non-linear and specialized applications of operational amplifiers.
- Understand the theory of ADC and DAC.
- Realize the importance of Operational Amplifier.

UNIT – I

Differential Amplifiers: Differential amplifier configurations, Balanced and unbalanced output differential amplifiers, current mirror, level Translator. **Operational amplifiers:** Introduction, Block diagram, Ideal op-amp, Equivalent Circuit, Voltage Transfer curve, open loop op-amp configurations. Introduction to dual OP-AMP TL082 as a general purpose JFET-input Operational Amplifier.

UNIT-II

Introduction, feedback configurations, voltage series feedback, voltage shunt feedback and differential amplifiers, properties of Practical op-amp. **Frequency response:** Introduction, compensating networks, frequency response of internally compensated op-amps and non compensated op-amps, High frequency opamp equivalent circuit, open loop gain Vs frequency, closed loop frequency response, circuit stability, slew rate.

UNIT-III

DC and AC amplifiers, peaking amplifier, summing, scaling and averaging amplifiers, instrumentation amplifier, voltage to current converter, current to voltage converter, integrator, differentiator, active filters, First, Second and Third order Butterworth filter and its frequency response, Tow-Thomas biquad filter.

UNIT-IV

Oscillators, Phase shift and wein bridge oscillators, Square, triangular and sawtooth wave generators, Comparators, zero crossing detector, Schmitt trigger, characteristics and limitations.**Specialized applications:** 555 timer IC (monostable&astable operation) & its applications, PLL, operating principles, Monolithic PLL, applications, analog multiplier and phase detection, Wide bandwidth precision analog multiplier MPY634 and its applications.

UNIT V

Analog and Digital Data Conversions, D/A converter – specifications – weighted resistor type, R-2R Ladder type, Voltage Mode and Current-Mode R - 2R Ladder types - switches for D/A converters, high speed sample-and-hold circuits, A/D Converters – specifications – Flash type – Successive Approximation type – Single Slope type – Dual Slope type – A/D Converter using Voltage-to-Time Conversion – Over-sampling A/D Converters,

TEXT BOOKS:

1. D. Roy Chowdhury, “Linear Integrated Circuits”, New Age International (p) Ltd, 2nd Edition, 2003.
2. K.LalKishore,“Operational Amplifiers and Linear Integrated Circuits”, Pearson Education,2007.

REFERENCES:

1. Ramakanth A. Gayakwad, “Op-Amps & Linear ICs”, PHI, 4th edition, 1987.
2. R.F.Coughlin& Fredrick Driscoll, “Operational Amplifiers & Linear Integrated Circuits”, 6th Edition, PHI.
3. David A. Bell, “Operational Amplifiers & Linear ICs”, Oxford University Press, 2nd edition, 2010.

UNIT -1

INTERATED CIRCUITS

OPERATIONAL AMPLIFIER:

The operational amplifier is a direct-coupled high gain amplifier usable from 0 to over 1MH Z to which feedback is added to control its overall response characteristic i.e. gain and bandwidth. The op-amp exhibits the gain down to zero frequency.

Such direct coupled (dc) amplifiers do not use blocking (coupling and by pass) capacitors since these would reduce the amplification to zero at zero frequency. Large by pass capacitors may be used but it is not possible to fabricate large capacitors on a IC chip. The capacitors fabricated are usually less than 20 pf. Transistor, diodes and resistors are also fabricated on the same chip.

DIFFERENTIAL AMPLIFIER:

Differential amplifier is a basic building block of an op-amp. The function of a differential amplifier is to amplify the difference between two input signals. How the differential amplifier is developed? Let us consider two emitter-biased circuits as shown
in fig.1

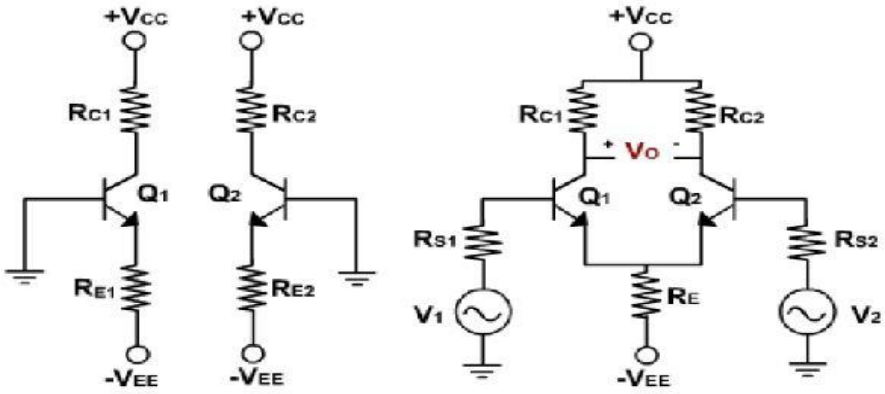


Fig. 1

The two transistors Q1 and Q2 have identical characteristics. The resistances of the circuits are equal, i.e. RE1 = R E2, RC1 = R C2 and the magnitude of +VCC is equal to the magnitude of -VEE. These voltages are measured with respect to ground.

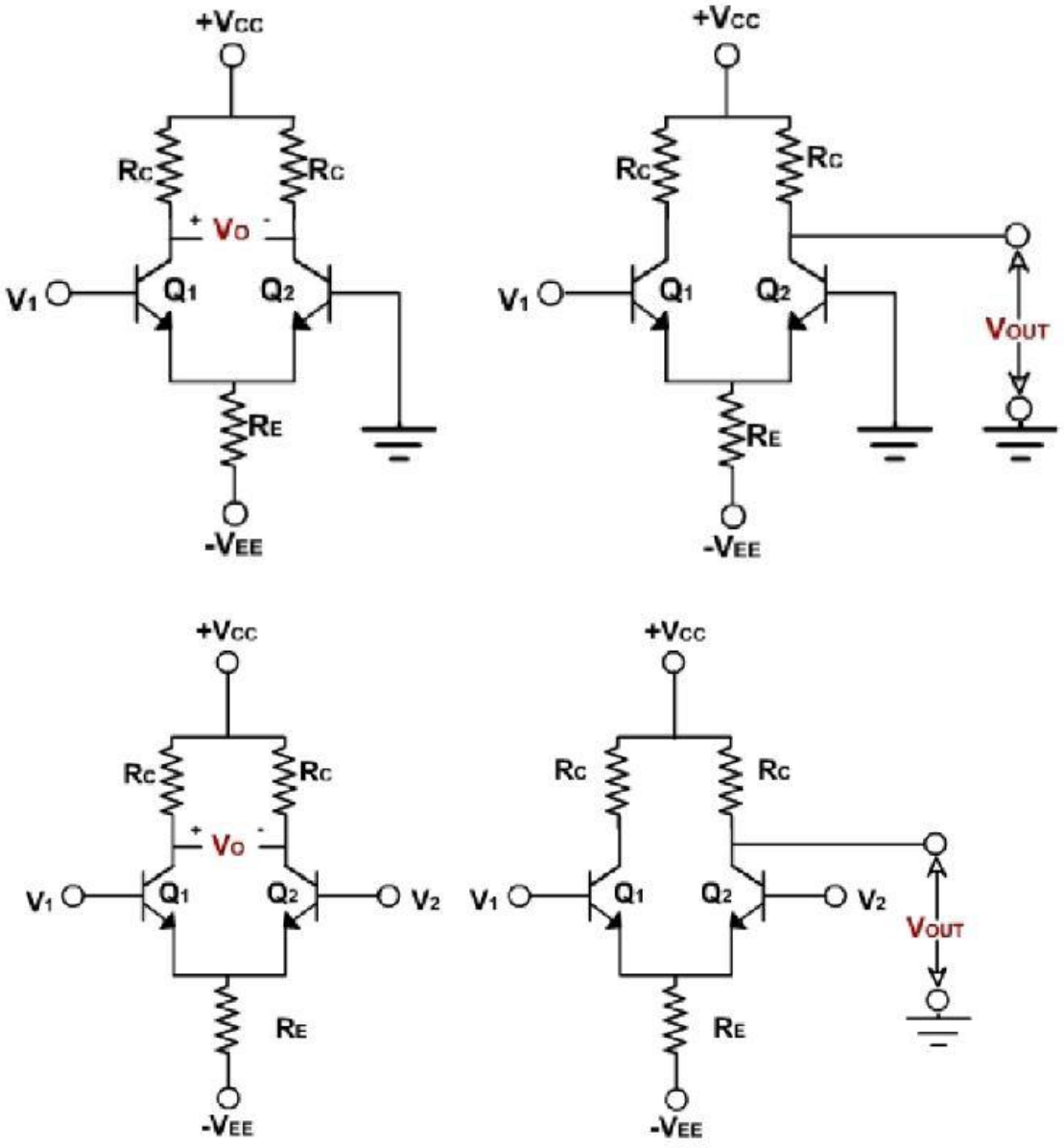
To make a differential amplifier, the two circuits are connected as shown in fig.1. The two +VCC and –VEE supply terminals are made common because they are same. The two emitters are also connected and the parallel combination of RE1 and RE2 is replaced by a resistance RE. The two input signals v1 & v2 are applied at the base of Q1 and at the base of Q2. The output voltage is taken between two collectors. The collector resistances are equal and therefore denoted by RC = RC1 = RC2.

Ideally, the output voltage is zero when the two inputs are equal. When v1 is greater then v2 the output voltage with the polarity shown appears. When v1 is less than v2, the output voltage has the opposite polarity.

The four differential amplifier configurations are following:

1. Dual input, balanced output differential amplifier.
2. Dual input, unbalanced output differential amplifier.
3. Single input balanced output differential amplifier.

4. Single input unbalanced output differential amplifier



These configurations are shown in fig 2, and are defined by number of input signals used and the way an output voltage is measured. If use two input signals, the configuration is said to be dual input, otherwise it is a single input configuration. On the other hand, if the output voltage is measured between two collectors, it is referred to as a balanced output because both the collectors are at the same dc potential w.r.t. ground. If the output is measured at one of the collectors w.r.t. ground, the configuration is called an unbalanced output. A multistage amplifier with a desired gain can be obtained using direct connection between successive stages of differential amplifiers. The advantage of direct coupling is that it removes the lower cut off frequency imposed by the coupling capacitors, and they are therefore, capable of amplifying dc as well as ac input signals.

DUAL INPUT , BALANCED OUTPUT DIFFERENTIAL AMPLIFIER :

The circuit is shown in fig 1**,** v1 and v2 are the two inputs, applied to the bases of Q1 and Q2 transistors. The output voltage is measured between the two collectors C1 and C2 , which are at same dc potentials.

DC ANALYSIS :

To obtain the operating point (ICC and VCEQ) for differential amplifier dc equivalent circuit is drawn by reducing the input voltages v1 and v2 to zero as shown in fig. 3.

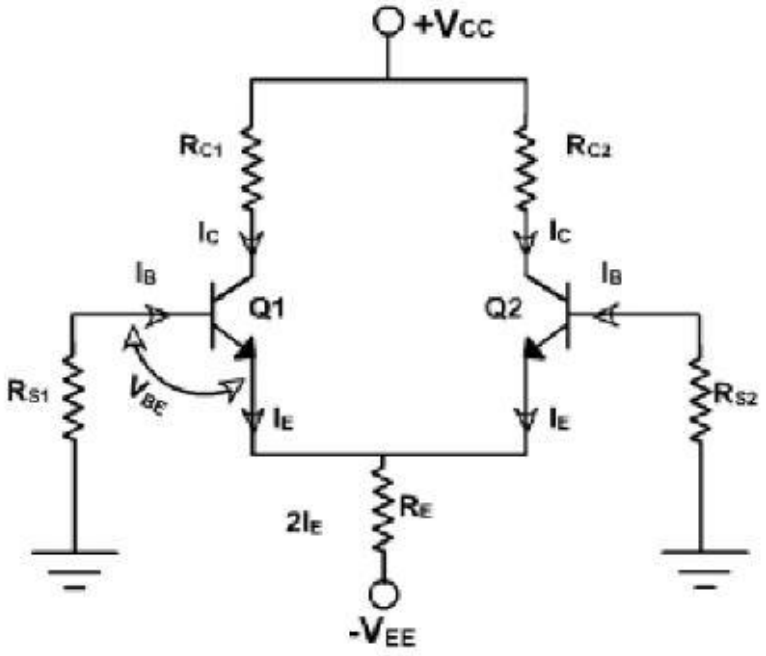


Fig. 3

$$R_S\ I_B + V_{BE} + 2\ I_E\ R_E = V_{EE}$$

But $I_B = \frac{I_E}{\beta_{dc}}$ and $I_C \approx I_E$

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E + R_S / \beta_{dc}} \qquad (E\text{-}1)$$

$V_{BE} = 0.6V$ for S_i and $0.2V$ for G_e.

Generally $\frac{R_S}{\beta_{dc}} << 2R_E$ because R_S is the internal resistance of input signal.

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E}$$

The value of RE sets up the emitter current in transistors Q1 and Q2 for a given value of VEE. The emitter current in Q1 and Q2 are independent of collector resistance RC. The voltage at the emitter of Q1 is approximately equal to -VBE if the voltage drop across R is negligible. Knowing the value of IC the voltage at the collector VC is given by

$$VC = VCC - Ic\,Rc$$

and

$$VCE = VC - VE$$
$$= VCC - IC\,RC + VBE$$

$$VCE = VCC + VBE - ICRC \quad (E\text{-}2)$$

From the two equations VCEQ and ICQ can be determined. This dc analysis applicable for all types of differential amplifier.

Example - 1

The following specifications are given for the dual input, balanced-output differential amplifier of fig.1**:**

RC = 2.2K ohm, RB = 4.7 K ohm, Rin 1 = Rin 2 = 50 ohm, +VCC = 10V, -VEE = -10 V, βdc =100 and VBE = 0.715V. Determine the operating points (ICQ and VCEQ) of the two transistors.

$$V_{CEQ} = V_{CC} + V_{BB} - R_C I_{CQ}$$
$$= 10 + 0.715 - (2.2k\Omega)(0.988mA)$$
$$= 8.54V$$

The values of I_{CQ} and V_{CEQ} are same for both the transistors.

DIFFERENTIAL INPUT RESISTANCE :

Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other terminal grounded. This means that the input resistance R_{i1} seen from the input signal source v_1 is determined with the signal source v_2 set at zero. Similarly, the input signal v_1 is set at zero to determine the input resistance R_{i2} seen from the input signal source v_2. Resistance R_{S1} and R_{S2} are ignored because they are very small.

$$R_{i1} = \left.\frac{v_1}{i_{b1}}\right|_{v_2 = 0}$$
$$= \left.\frac{v_1}{i_{e1}/\beta}\right|_{v_2 = 0}$$

Substituting i_{e1},

$$R_{i1} = \frac{\beta r'_e (r'_e + 2R_E)}{r'_e + R_E}$$

Since $R_E >> r'_e$

$\therefore \quad r'_e + 2R_E >> 2R_E$

or $\quad r'_e + R_E >> R_E$

$$\therefore R_{i1} = 2\beta r_e' \qquad (E\text{-}3)$$

Similarly,

$$R_{i2} = \left.\frac{V_2}{i_{b2}}\right|_{v_1=0}$$

$$= \left.\frac{V_2}{i_{e2}/\beta}\right|_{v_1=0}$$

$$R_{i2} = 2\beta r'_e \qquad \text{(E-4)}$$

The factor of 2 arises because the re' of each transistor is in series. To get very high input impedance with differential amplifier is to use Darlington transistors. Another way is to use FET.

OUTPUT RESISTANCE :

Output resistance is defined as the equivalent resistance that would be measured at output terminal with respect to ground. Therefore, the output resistance RO1 measured between collector C1 and ground is equal to that of the collector resistance RC. Similarly the output resistance RO2 measured at C2 with respect to ground is equal to that of the collector resistor RC.

RO1 = RO2 = RC (E-5)

The current gain of the differential amplifier is undefined. Like CE amplifier the ifferential amplifier is a small signal amplifier. It is generally used as a voltage amplifier and not as current or power amplifier.

A dual input, balanced output difference amplifier circuit is shown in fig.

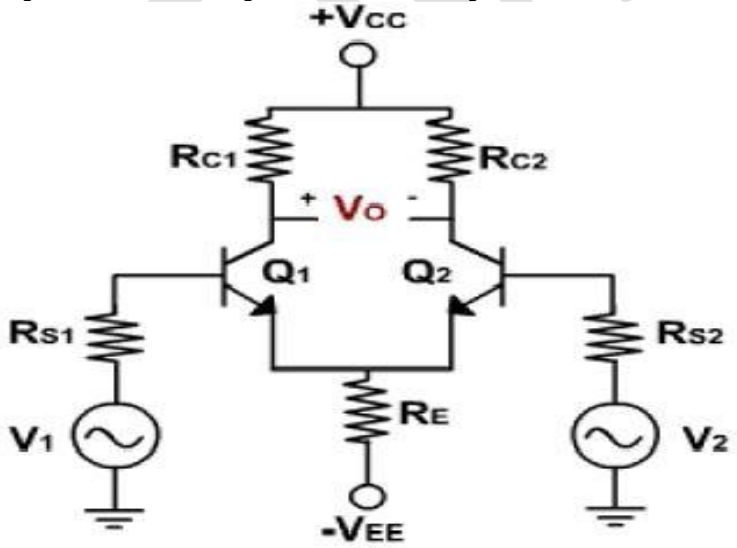


Fig. 1

Inverting & Non - Inverting Inputs**:**

In differential amplifier the output voltage v_O is given by

V_O = Ad (v1 - v2) When v2 = 0, V_O = Ad v1

when v1 = 0, V_O = - Ad v2

Therefore the input voltage v1 is called the non inventing input because a positive voltage v1 acting alone produces a positive output voltage vO. Similarly, the positive voltage v2 acting alone produces a negative output voltage hence v2 is called inverting input. Consequently B1 is called non inverting input terminal and B2 is called inverting input terminal.

COMMON MODE GAIN:

A common mode signal is one that drives both inputs of a differential amplifier equally. The common mode signal is interference, static and other kinds of undesirable pickup etc. The connecting wires on the input bases act like small antennas. If a differential amplifier is operating in anenvironment with lot of electromagnetic interference, each base picks up an unwanted interference voltage. If both the transistors were matched in all respects then the balanced output would be theoretically zero. This is the important characteristic of a differential amplifier. It discriminates against common mode input signals. In other words, it refuses to amplify the common mode signals. The practical effectiveness of rejecting the common signal depends on the degree of matching between the two CE stages forming the differential amplifier.

In other words, more closely are the currents in the input transistors, the better is the common mode signal rejection e.g. If v1 and v2 are the two input signals, then the output of a practical opamp cannot be described by simply

v0 = Ad (v1 - v2)

In practical differential amplifier, the output depends not only on difference signal but also upon the common mode signal (average).

vd = (v1 - vd)

In practical differential amplifier, the output depends not only on difference signal but also upon the common mode signal (average).
vd = (v1 - vd)

and vC = ½ (v1 + v2)

The output voltage, therefore can be expressed as

$v_o = A_1 v_1 + A_2 v_2$

Where A1 & A2 are the voltage amplification from input 1(2) to output under the condition that input 2 (1) is grounded.

$$\therefore v_1 = v_C + \frac{1}{2} v_d \quad , \quad v_2 = v_C - \frac{1}{2} v_d$$

Substituting V_1 & V_2 in output voltage equation

$$v_o = A_1 \left(v_C + \frac{1}{2} v_d\right) + A_2 \left(v_C - \frac{1}{2} v_d\right)$$

$$= \frac{1}{2} (A_1 - A_2) v_d + (A_1 - A_2) v_C$$

$$= A_d v_d + A_C v_C$$

The voltage gain for the difference signal is Ad and for the common mode signal is AC. The ability of a differential amplifier to reject a common mode signal is expressed by its common

mode rejection ratio (CMRR). It is the ratio of differential gain Ad to the common mode gain AC. Date sheet always specify CMRR in decibels CMRR = 20 log CMRR.

Dual Input, Unbalanced Output Differential Amplifier:

In this case, two input signals are given however the output is measured at only one of the two collector w.r.t. ground as shown in fig. 2. The output is referred to as an unbalanced output because the collector at which the output voltage is measured is at some finite dc potential with respect to ground..

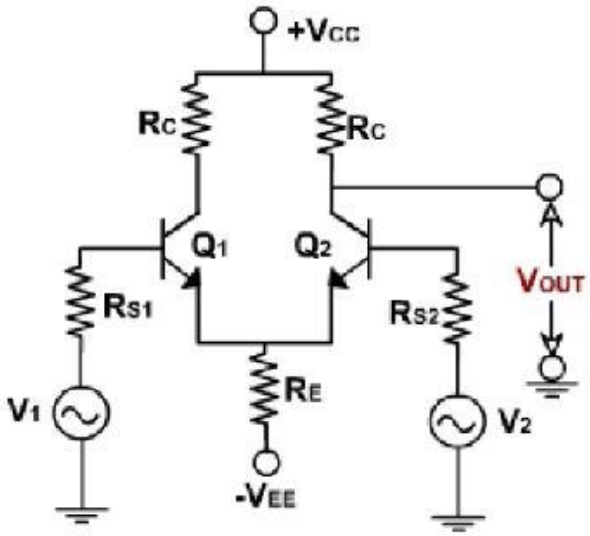


Fig. 2

In other words, there is some dc voltage at the output terminal without any input signal applied. DC analysis is exactly same as that of first case.

$$I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + R_2 / \beta_{dc}}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C$$

AC Analysis:

The output voltage gain in this case is given by

$$A_d = \frac{V_O}{V_d} = \frac{R_C}{2r'_e}$$

The voltage gain is half the gain of the dual input, balanced output differential amplifier. Since atthe output there is a dc error voltage, therefore, to reduce the voltage to zero, this configuration is normally followed by a level translator circuit.

Differential amplifier with swamping resistors:

By using external resistors R'_E in series with each emitter, the dependence of voltage gain on variations of r'_e can be reduced. It also increases the linearity range of the differential amplifier.
Fig. 3, shows the differential amplifier with swamping resistor R'_E. The value of R'_E is usually large enough to swamp the effect of r'_e.

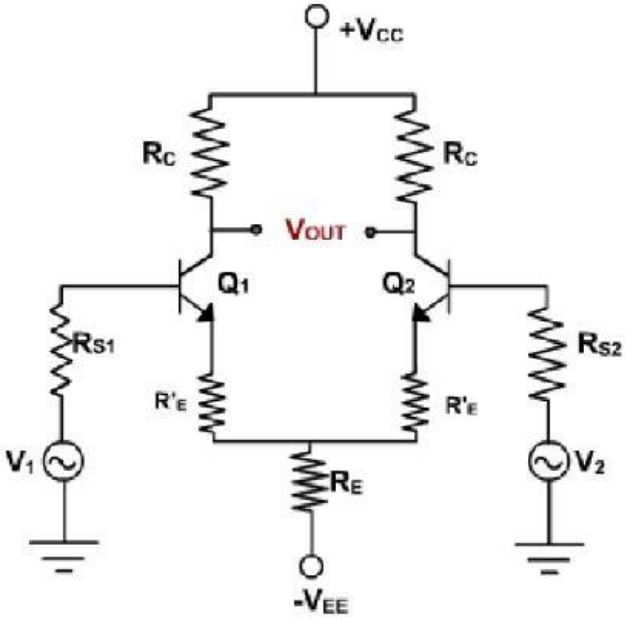


Fig. 3

$$R_1 I_B + V_{BE} + R'_E I_E + 2 R_E I_E = V_{EE}$$

$$R_1 I_E / \beta_{dc} + V_{BE} + R'_E I_E + 2 R_E I_E = V_{EE}$$

From the equation, I_E can be obtained as

$$I_E = \frac{V_{EE} - V_{BE}}{R'_E + 2R_E + R_1 / \beta_{dc}}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C$$

The new voltage gain is given by $A_d = \frac{R_C}{r_e + R_E}$

The input resistance is given by $R_{i1} = R_{i2} = 2\beta\ (r'_e + R'_E)$

The output resistance with or without R'_E is the same i.e.

$$R_{O1} = R_{O1} = R_C$$

Constant Current Bias:

In the dc analysis of differential amplifier, we have seen that the emitter current IE depends upon the value of βdc. To make operating point stable IE current should be constant irrespective value of βdc. For constant IE, RE should be very large. This also increases the value of CMRR but if RE value is increased to very large value, IE (quiescent operating current) decreases. To maintain same value of IE, the emitter supply VEE must be increased. To get very high value of resistance RE and constant IE, current, current bias is used.

Fig.

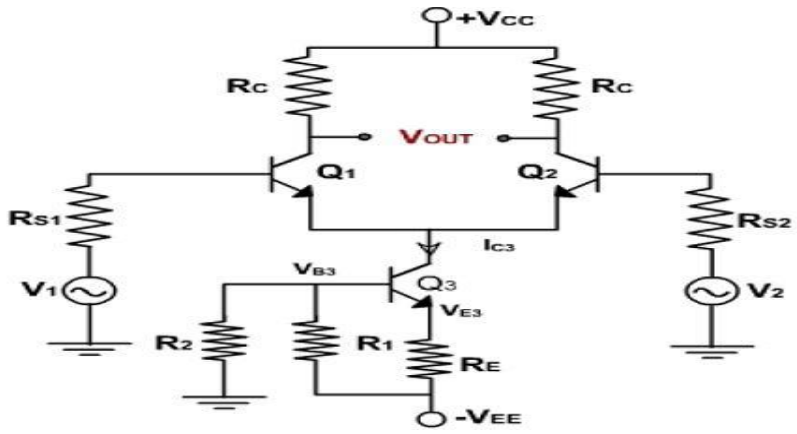


Figure 5.1

Fig. 1, shows the dual input balanced output differential amplifier using a constant current bias. The resistance RE is replace by constant current transistor Q3. The dc collector current in Q3 is established by R1, R2, & RE.

Applying the voltage divider rule, the voltage at the base of Q3 is

$$V_{B3} = \frac{R_2}{R_1 + R_2}(-V_{EE})$$

$$V_{E3} = V_{B3} - V_{BE3}$$

$$= -\frac{R_2}{R_1 + R_2} V_{EE} - V_{BE3}$$

$$I_{BE3} = I_{C3} = \frac{V_{E3} - (-V_{EE})}{R_E}$$

$$= \frac{V_{EE} - \left(\frac{R_2}{R_1 + R_2}\right) V_{EE} - V_{BE3}}{R_E}$$

Because the two halves of the differential amplifiers are symmetrical, each has half of the current IC3.

$$I_{E1} = I_{E2} = \frac{I_{C3}}{2} = \frac{V_{EE} - \left[\frac{R_2}{R_1 + R_2} V_{EE}\right] - V_{BE3}}{2R_E}$$

The collector current, IC3 in transistor Q3 is fixed because no signal is injected into either the emitter or the base of Q3. Besides supplying constant emitter current, the constant current bias also provides a very high source resistance since the ac equivalent or the dc source is ideally an open circuit. Therefore, all the performance equations obtained for differential amplifier using emitter bias are also valid. As seen in IE expressions, the current depends upon VBE3. If temperature changes, VBE changes and current IE also changes. To improve thermal stability, a diode is placed in series with resistance R1as shown in fig. 2.

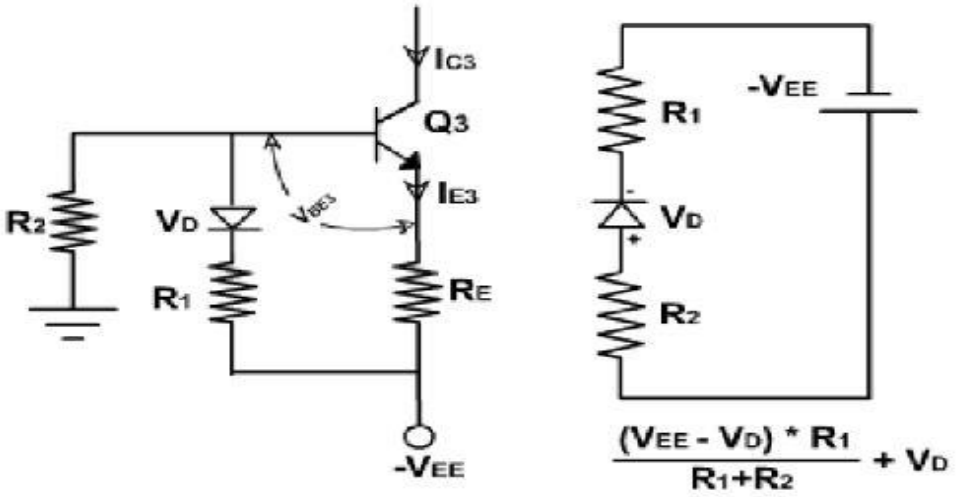


Fig. 2

This helps to hold the current IE3 constant even though the temperature changes. Applying KVL to the base circuit of Q3.

$$(V_{EE} - V_D)\ \frac{R_1}{R_1+R_2} + V_D = V_{BE3} + I_{E3}R_E$$

where V_D is the diode voltage. Thus,

$$I_{E3} = \frac{1}{R_E}\left\{ V_{EE}\ \frac{R_1}{R_1+R_2} + V_D\ \frac{R_1}{R_1+R_2} - V_{BE3} \right\}$$

If R_1 and R_2 are so chosen that

$$\frac{R_2}{R_1+R_2}\ V_D = V_{BE3}$$

then,

$$I_{E3} = \frac{1}{R_3} \cdot \frac{V_{EE}R_1}{R_1+R_2}$$

Fig. 1, shows the dual input balanced output differential amplifier using a constant current bias. The resistance RE is replace by constant current transistor Q3. The dc collector current in Q3 is established by R1, R2, & RE.

Applying the voltage divider rule, the voltage at the base of Q3 is

Therefore, the current IE3 is constant and independent of temperature because of the added diode D. Without D the current would vary with temperature because VBE3 decreases approximately by 2mV/° C. The diode has same temperature dependence and hence the two variations cancel each other and IE3 does not vary appreciably with temperature. Since the cut ? in voltage VD of diode approximately the same value as the base to emitter voltage VBE3 of a transistor the above condition cannot be satisfied with one diode. Hence two diodes are used in series for VD. In this case the common mode gain reduces to zero.

Some times zener diode may be used in place of diodes and resistance as shown in fig. 3. Zeners are available over a wide range of voltages and can have matching temperature coefficient The voltage at the base of transistor QB is

$$V_{B3} = V_Z - V_{EE}$$

$$V_{E3} = V_{B3} - V_{BE3}$$

$$= V_Z - V_{EE} - V_{BE3}$$

$$\therefore I_{E3} = \frac{V_{E3} - (-V_{EE})}{R_E}$$

$$= \frac{V_Z - V_{BE3}}{R_E}$$

The value of R2 is selected so that I2 = 1.2 IZ(min) where IZ is the minimum current required to cause the zener diode to conduct in the reverse region, that is to block the rated voltage VZ.

$$R_2 = \frac{V_{EE} - V_Z}{I_2}$$

$$\text{Where } I_2 = 1.2\, I_{Z(min)}$$

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. ... The current mirror is used to provide bias currents and active loads to circuits.

UNIT – II OPERATIONAL AMPLIFIER

The purpose of these experiments is to introduce the most important of all analog building blocks, the *operational amplifier* ("op-amp" for short). This handout gives an introduction to these amplifiers and a smattering of the various configurations that they can be used in. Apart from their most common use as amplifiers (both inverting and non-inverting), they also find applications as buffers (load isolators), adders, subtractors, integrators, logarithmic amplifiers, impedance converters, filters (low-pass, high-pass, band-pass, band-reject or notch), and differential amplifiers. So let's get set for a fun-filled adventure with op-amps!

General Operational Amplifier:

An operational amplifier generally consists of three stages, anmely,1. a differential amplifier 2. additional amplifier stages to provide the required voltage gain and dc level shifting 3. an emitter-follower or source follower output stage to provide current gain and low output resistance. A low-frequency or dc gain of approximately 10^4 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp. The output voltage is required to be at ground, when the differential input voltages is zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed. Moreover, as the input bias currents are to be very small of the order of picoamperes, an FET input stage is normally preferred. The figure shows a general op-amp circuit using JFET input devices.

Input stage:

The input differential amplifier stage uses p-channel JFETs M_1 and M_2. It employs a three transistor active load formed by Q_3 , Q_4 , and Q_5 . the bias current for the stage is provided by a two-transistor current source using PNP transistors Q_6 and Q_7. Resistor R_1 increases the output resistance seen looking into the collector of Q_4 as indicated by R_{04}. This is necessary to provide bias current stability against the transistor parameter variations. Resistor R_2 establishes a definite bias current through Q_5 . A single ended output is taken out at the collector of Q_4 . MOSFET's are used in place of JFETs with additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

Gain stage:

The second stage or the gain stage uses Darlington transistor pair formed by Q_8 and Q_9 as shown in figure. The transistor Q_8 is connected as an emitter follower, providing large input resistance. Therefore, it minimizes the loading effect on the input differential amplifier stage. The transistor Q_9 provides an additional gain and Q_{10} acts as an active load for this stage. The current mirror formed by Q_7 and Q_{10} establishes the bias current for Q_9 . The V_{BE} drop across Q_9 and drop across R_5 constitute the voltage drop across R_4 , and this voltage sets the current through Q_8 . It can be set to a small value, such that the base current of Q_8 also is very less.

Output stage:

The final stage of the op-amp is a class AB complementary push-pull output stage. Q_{11} is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage. Bias current for Q_{11} is provided by the current mirror formed by Q_7 and Q_{12}, through Q_{13} and Q_{14} for minimizing the cross over distortion. Transistors can also be used in place of the two diodes. The overall voltage gain A_V of the op-amp is the product of voltage gain of each stage as given by $A_V = |A_d|\,|A_2||A_3|$ Where A_d is the gain of the differential amplifier stage, A_2 is the gain of the second gain stage and A_3 is the gain of the output stage.

IC 741 Bipolar operational amplifier:

The IC 741 produced since 1966 by several manufactures is a widely used general purpose operational amplifier. Figure shows that equivalent circuit of the 741 op-amp, divided into various individual stages.

The op-amp circuit consists of three stages.

1. the input differential amplifier
2. The gain stage
3. the output stage.

A bias circuit is used to establish the bias current for whole of the circuit in the IC. The op-amp is supplied with positive and negative supply voltages of value ± 15V, and the supply voltages as low as ±5V can also be used.

Bias Circuit:

The reference bias current I_{REF} for the 741 circuit is established by the bias circuit consisting of two diodes-connected transistors Q_{11} and Q_{12} and resistor R_5. The widlar current source formed by Q_{11} , Q_{10} and R_4 provide bias current for the differential amplifier stage at the collector of Q_{10}. Transistors Q_8 and Q_9 form another current mirror providing bias current for the differential amplifier. The reference bias current I_{REF} also provides mirrored and proportional current at the collector of the double –collector lateral PNP transistor Q_{13}. The transistor Q_{13} and Q_{12} thus form a two-output current mirror with Q_{13A} providing bias current for output stage and Q_{13B} providing bias current for Q_{17}. The transistor Q_{18} and Q_{19} provide dc bias for the output stage. Formed by Q_{14} and Q_{20} and they establish two V_{BE} drops of potential difference between the bases of Q_{14} and Q_{18} .

Input stage:

The input differential amplifier stage consists of transistors Q_1 through Q_7 with biasing provided by Q_8 through Q_{12}. The transistor Q_1 and Q_2 form emitter – followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using Q_3 and Q_4 which offers a large voltage gain. The transistors Q5, Q6 and Q7 along with resistors R_1, R_2 and R_3 from the active load for input stage. The single-ended output is available at the collector of Q_6. the two null terminals in the input stage facilitate the null adjustment. The lateral PNP transistors Q_3 and Q_4 provide additional protection against voltage breakdown conditions. The emitter-base junction Q_3 and Q_4 have higher emitter-base breakdown voltages of about 50V. Therefore, placing PNP transistors in series with NPN transistors provide protection against accidental shorting of supply to the input terminals.

Gain Stage:

The Second or the gain stage consists of transistors Q_{16} and Q_{17}, with Q_{16} acting as an emitter – follower for achieving high input resistance. The transistor Q_{17} operates in common

emitter configuration with its collector voltage applied as input to the output stage. Level shifting is done for this signal at this stage. Internal compensation through Miller compensation technique is achieved using the feedback capacitor C_1 connected between the output and input terminals of the gain stage.

Output stage:

The output stage is a class AB circuit consisting of complementary emitter follower transistor pair Q_{14} and Q_{20}. Hence, they provide an effective loss output resistance and current gain. The output of the gain stage is connected at the base of Q_{22}, which is connected as an emitter – follower providing a very high input resistance, and it offers no appreciable loading effect on the gain stage. It is biased by transistor Q_{13A} which also drives Q_{18} and Q_{19}, that are used for establishing a quiescent bias current in the output transistors Q_{14} and Q_{20}.

Ideal op-amp characteristics:

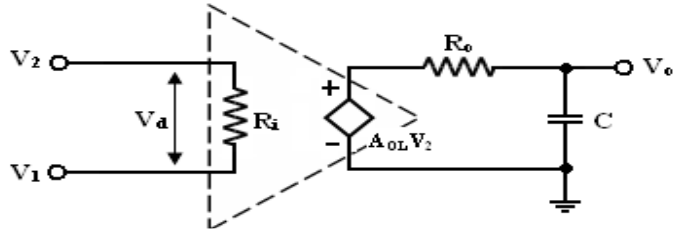
1. Infinite voltage gain A.
2. Infinite input resistance R_i, so that almost any signal source can drive it and there is no loading of the proceeding stage.
3. Zero output resistance R_o, so that the output can drive an infinite number of other devices.
4. Zero output voltage, when input voltage is zero.
5. Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified with out attenuation.
6. Infinite common mode rejection ratio, so that the output common mode noise voltage is zero.
7. Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

AC Characteristics:

For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

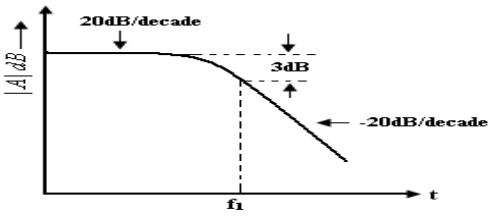
Frequency Response:

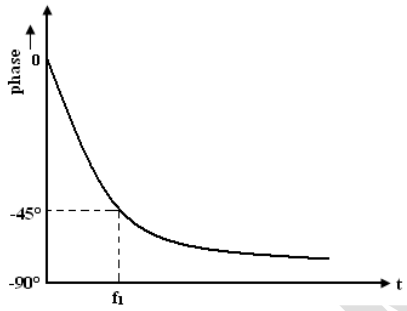
The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response. Op-amp should have an infinite bandwidth Bw =∞ (i.e) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the o/p.



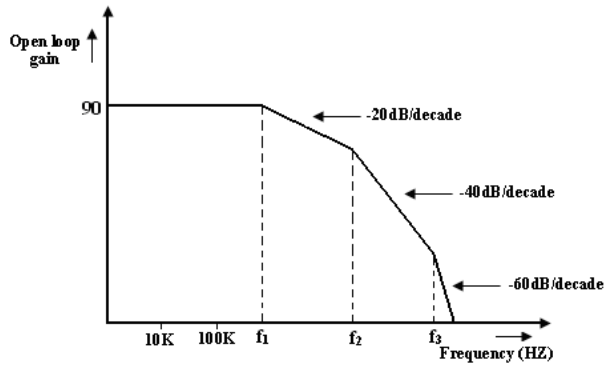
There is one pole due to R_0 C and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig. f1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop volt gain are fu of frequency can be written as, The magnitude and phase angle characteristics from eqn (29) and (30)

1. For frequency f<< f_1 the magnitude of the gain is 20 log A_{OL} in dB.
2. At frequency f = f_1 the gain in 3 dB down from the dc value of A_{OL} in dB. This frequency f_1 is called corner frequency.
3. For f>> f_1 the fain roll-off at the rate off -20dB/decade or -6dB/decade.





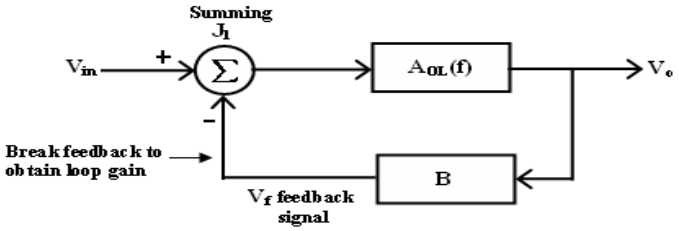
From the phase characteristics that the phase angle is zero at frequency f =0. At the corner frequency f_1 the phase angle is -45^0 (lagging and a infinite frequency the phase angle is -90^0 . It shows that a maximum of 90^0 phase change can occur in an op-amp with a single capacitor C. Zero frequency is taken as te decade below the corner frequency and infinite frequency is one decade above the corner frequency.



Circuit Stability:

A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. (or) A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable sys keeps on increasing until

the system break down. The unstable system are impractical and need be made stable. The criterian gn for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability , ex: Bode plots.Bode plots are compared



of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram.

The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred ―Transfer frequency' From fig we represented it by $A_{OL}(f)$ which is given by $A_{OL}(f) = V_0/Vin$ if $V_f = 0$. -----(1)

where $A_{OL}(f)$ = open loop volt gain. The closed loop gain A_f is given by

$A_F = V_0/Vin$

$A_F = A_{OL} / (1+(A_{OL})(B)$ ----(2)

B = gain of feedback circuit.

B is a constant if the feedback circuit uses only resistive components. Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

1. Method:1:

Determine the phase angle when the magnitude of $(A_{OL})(B)$ is 0dB (or) 1. If phase angle is > .- 180^0, the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

2. Method 2:

Determine the phase angle when the magnitude of $(A_{OL})(B)$ is 0dB (or) 1. If phase angle is > .- 180^0, If the magnitude is –ve decibels then the system is stable. However, the some systems the phase angle of a system may reach -180^0, under such conditions method 1 must be used to determine the system stability.

Slew Rate:

Another important frequency related parameter of an op-amp is the slew rate. (Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs).

Reason for Slew rate:

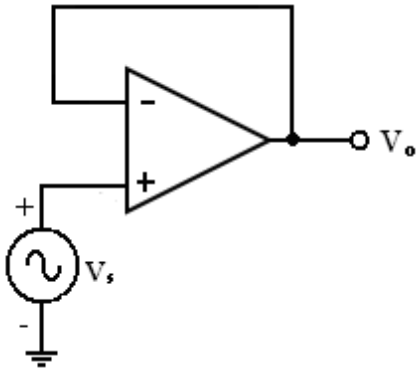
There is usually a capacitor within 0, outside an op-amp oscillation. It is this capacitor which prevents the o/p voltage from fast changing input. The rate at which the volt across the capacitor increases is given by $dVc/dt = I/C$ --------(1)

I -> Maximum amount furnished by the op-amp to capacitor C. Op-amp should have the either a higher current or small compensating capacitors.

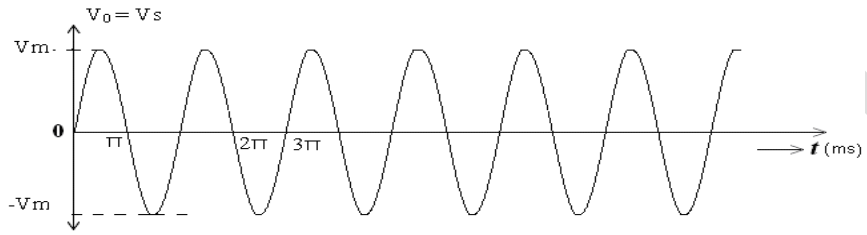
For 741 IC, the maximum internal capacitor charging current is limited to about 15μA. So the slew rate of 741 IC is $SR = dVc/dt|max = Imax/C$.

For a sine wave input, the effect of slew rate can be calculated as consider volt follower -> The input is large amp, high frequency sine wave .

If Vs = Vm Sinwt then output V_0 = Vm sinwt . The rate of change of output is given by dV_0/dt =



Vm w coswt.



Input and Output Waveforms

The max rate of change of output across when coswt =1

(i.e) SR = dV_0/dt |max = wVm.

SR = 2ΠfVm V/s = 2ΠfVm v/ms.

Thus the maximum frequency fmax at which we can obtain an undistorted output volt of peak value Vm is given by

fmax (Hz) = Slew rate/6.28 * Vm . called the full power response. It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

DC Characteristics of op-amp:

Current is taken from the source into the op-amp inputs respond differently to current and Voltage due to mismatch in transistor.

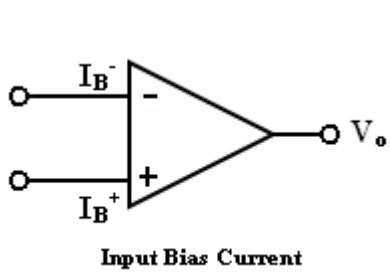
DC output voltages are,

1. Input bias current
2. Input offset current
3. Input offset voltage
4. Thermal drift

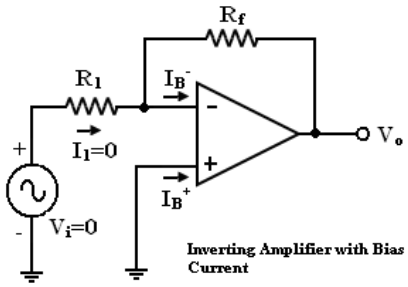
Input bias current:

The op-amp‘s input is differential amplifier, which may be made of BJT or FET.

- In an ideal op-amp, we assumed that no current is drawn from the input terminals.
- The base currents entering into the inverting and non-inverting terminals (I_{B-} & I_{B+} respectively).
- Even though both the transistors are identical, I_{B-} and I_{B+} are not exactly equal due to internal imbalance between the two inputs.
- Manufacturers specify the input bias current I_B



Input Bias Current

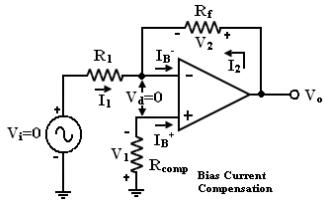


Inverting Amplifier with Bias Current

If input voltage $V_i = 0V$. The output Voltage V_o should also be ($V_o = 0$)
$I_B = 500nA$ We find that the output voltage is offset by,

$$V_o = I_{B@b\,c} R_f Q\ 2\ `\ a$$

Op-amp with a 1M feedback resistor
$V_o = 5000nA$ X 1M = 500mV
The output is driven to 500mV with zero input, because of the bias currents.
In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated. Where a compensation resistor R_{comp} has been added between the non-inverting input terminal and ground as shown in the figure below.



Bias Current Compensation

Current IB flowing through the compensating resistor Rcomp, then by KVL we get,
-V1+0+V2-Vo = 0 (or)
Vo = V2 – V1 ——>(3)
By selecting proper value of Rcomp, V2 can be cancelled with V1 and the Vo = 0. The value of Rcomp
is derived a
V1 = IB+Rcomp (or) IB+ = V1/Rcomp ——>(4)
The node_a‘ is at voltage (-V1).Because the voltage at
the non-inverting input terminal is(-V1).
So with Vi = 0 we get,
I1 = V1/R1 ——>(5)
I2 = V2/Rf ——>(6)
For compensation, Vo should equal to zero (Vo = 0, Vi = 0). i.e. from equation (3) V2 = V1. So that,
I2 = V1/Rf ——>(7)
KCL at node _a‘ gives,
IB- = I2 + I1
Rcomp = R1 || Rf ———>(9)

i.e. to compensate for bias current, the compensating resistor, Rcomp should be equal to the parallel combination of resistor R1 and Rf.

Input offset current:

 Bias current compensation will work if both bias currents IB
+ and IB- are equal.

 Since the input transistor cannot be made identical. There will always be some small difference between IB
+ and IB-. This difference is called the offset current

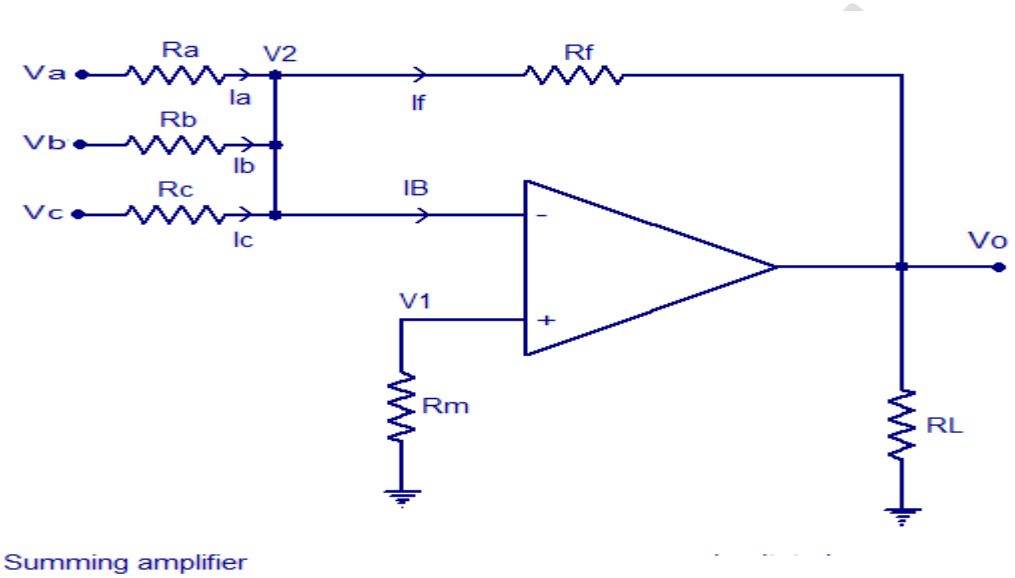
|Ios| = IB+-IB- ——>(10)

UNIT-III

OPAMP APLLICATIONS-1

Summing amplifier using opamp

Summing amplifier is a type operational amplifier circuit which can be used to sum signals. The sum of the input signal is amplified by a certain factor and made available at the output .Any number of input signal can be summed using an opamp. The circuit shown below is a three input summing amplifier in the inverting mode.



Summing amplifier circuit

In the circuit, the input signals Va,Vb,Vc are applied to the inverting input of the opamp through input resistors Ra,Rb,Rc. Any number of input signals can be applied to the inverting input in the above manner. Rf is the feedback resistor.Non inverting input of the opamp is grounded using resistor Rm. RL is the load resistor. By applying kirchhoff's current law at not V2 we get,

Ia+Ib+Ic = If+Ib

Since the input resistance of an ideal opamp is close to infinity and has infinite gain. We can neglect Ib & V2
There for Ia+Ib+Ic = If …….(1)

Equation (1) can be rewritten as

(Va/Ra) + (Vb/Rb)+ (Vc/Rc) = (V2-Vo)/Rf

Neglecting Vo,

we get Va/Ra + Vb/Rb + Vc/Rc = -Vo/Rf

Vo = -Rf ((Va/Ra)+(Vb/Rb)+(Vc/Rc))

Vo = -((Rf/Ra)Va + (Rf/Rb) Vb + (Rf/Rc) Vc)……..(2)

If resistor Ra, Rb, Rc has same value ie; Ra=Rb=Rc=R, then equation (2) can be written as

Vo = -(Rf/R) x (Va + Vb +Vc)…….(3)

If the values of Rf and R are made equal , then the equation becomes,

Vo = -(Va + Vb +Vc)

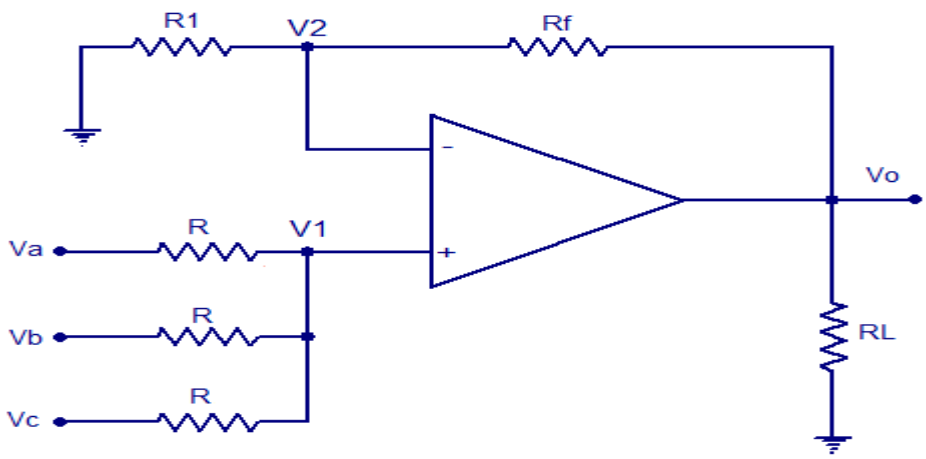
Averaging Circuit :

An averaging circuit can be made from the above circuit by making the all input resistor equal in value ie; Ra = Rb = Rc =R and the gain must be selected such that if there are m inputs, then Rf/R must be equal to 1/m.

Scaling amplifier

In a scaling amplifier each input will be multiplied by a different factor and then summed together. Scaling amplifier is also called a weighted amplifier. Here different values are chosen for Ra, Rb and Rc. The governing equation is Vo = -((Rf/Ra)Va + (Rf/Rb) Vb + (Rf/Rc) Vc).

Summing amplifier in non inverting configuration.



Summing amplifier non inverting configuration

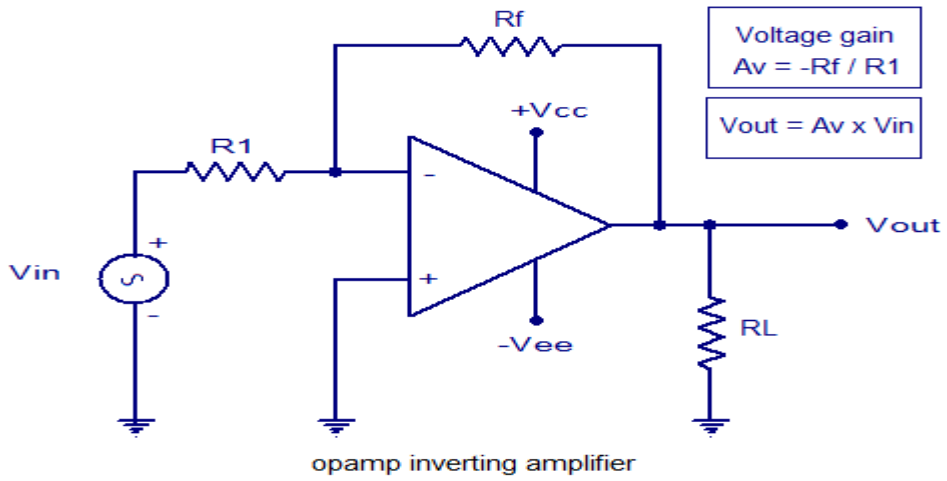
A non inverting summing amplifier circuit with three inputs are shown above. The voltage inputs Va, Vb and Vc are applied to non inverting input of the opamp. Rf is the feedback resistor. The output voltage of the circuit is governed by the equation;

Vo = (1+ (Rf/R1)) ((Va+Vb+Vc)/3)

AC AMPLIFIER

Opamp inverting amplifier

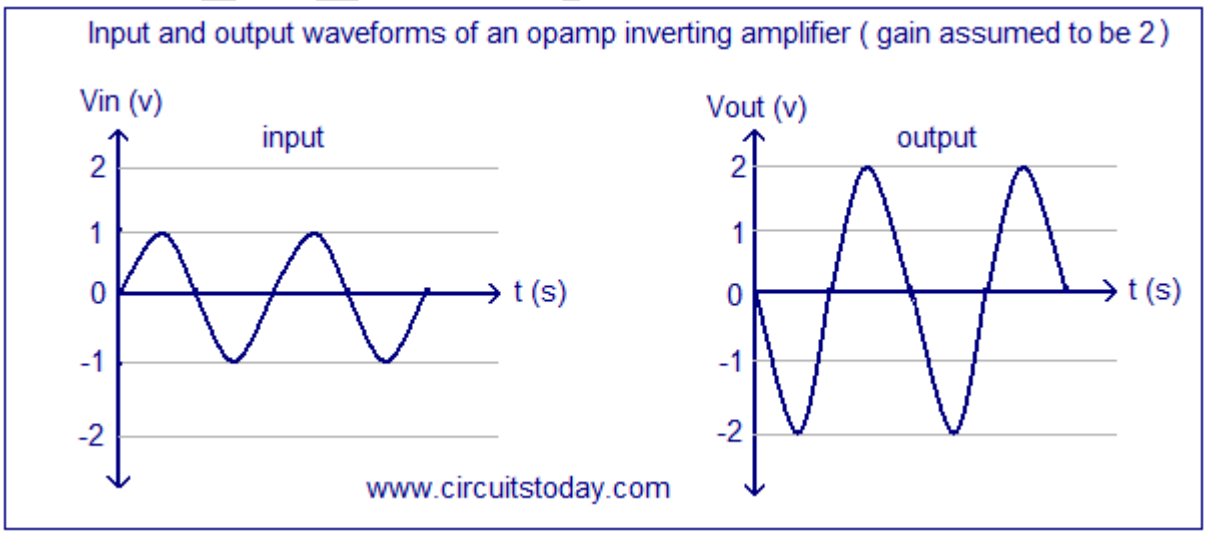
An inverting amplifier using opamp is a type of amplifier using opamp where the output waveform will be phase opposite to the input waveform. The input waveform will be amplifier by the factor Av (voltage gain of the amplifier) in magnitude and its phase will be inverted. In the inverting amplifier circuit the signal to be amplified is applied to the inverting input of the opamp through the input resistance R1. Rf is the feedback resistor. Rf and Rin together determines the gain of the amplifier. Inverting operational amplifier gain can be expressed using the equation Av = – Rf/R1. Negative sign implies that the output signal is negated. The circuit diagram of a basic inverting amplifier using opamp is shown below.



opamp inverting amplifier

Inverting amplifier using opamp

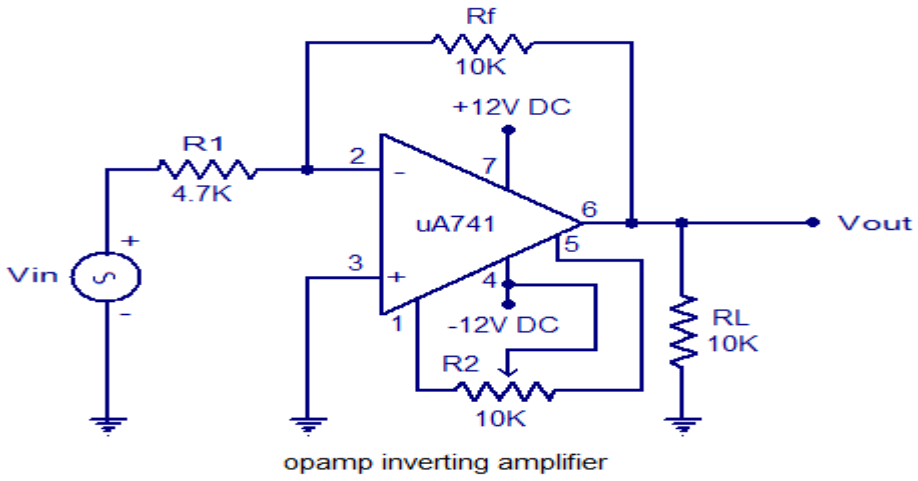
The input and output waveforms of an inverting amplifier using opamp is shown below. The graph is drawn assuming that the gain (Av) of the amplifier is 2 and the input signal is a sine wave. It is clear from the graph that the output is twice in magnitude when compared to the input (Vout = Av x Vin) and phase opposite to the input.



Inverting operatinal amplifier waveform

Practical inverting amplifier using 741.

A simple practical inverting amplifier using 741 IC is shown below. uA 741 is a high performance and of course the most popular operational amplifier. It can be used in a verity of applications like integrator, differentiator, voltage follower, amplifier etc. uA 741 has a wide supply voltage range (+/-22V DC) and has a high open loop gain. The IC has an integrated compensation network for improving stability and has short circuit protection.



opamp inverting amplifier

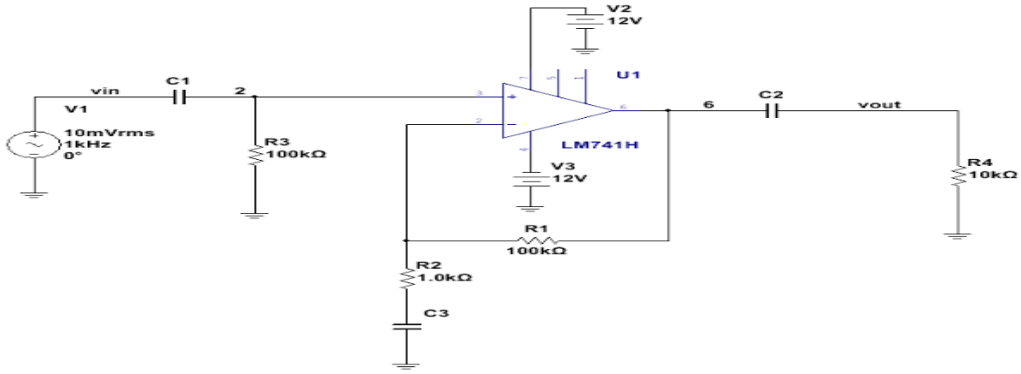
Practical inverting amplifier using 741

Signal to be amplified is applied to the inverting pi (pin2) of the IC. Non inverting pin (pin3) is connected to ground. R1 is the input resistor and Rf is the feedback resistor. Rf and R1 together sets the gain of the amplifier. With the used values of R1 and Rf the gain will be 10 (Av = -Rf/R1 = 10K/1K = 10). RL is the load resistor and the amplified signal will be available across it. POT R2 can be used for nullifying the output offset voltage. If you are planning to assemble the circuit, the power supply must be well regulated and filtered. Noise from the power supply can adversely affect the performance of the circuit. When assembling on PCB it is recommended to mount the IC on the board using an IC base.

Non Inverting AC Amplifier:

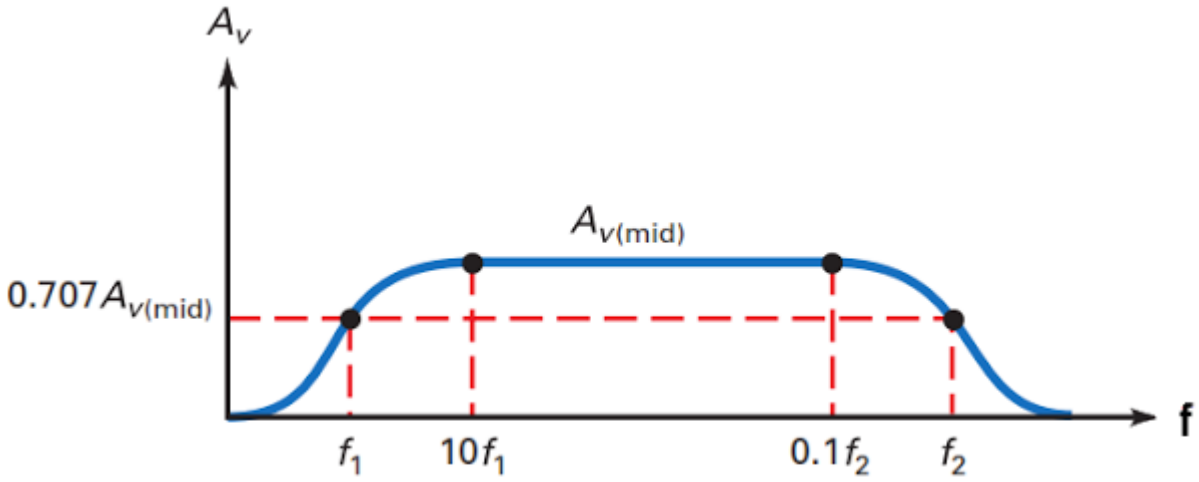
The two capacitors C1 and C2 are the coupling capacitors. We can put another capacitor connecting resistor R2 to the ground. This is a bypass capacitor which allows high frequency to go to the ground. By connecting such capacitor we can reduce the output offset voltage. The

following is the ac amplifier circuit with this third capacitor C3.



The function of these capacitors is to allow certain frequency to pass and block the lower frequency including the DC. The next step is to find out the value of these capacitors.

To know the value of these capacitors we need to see the frequency response of ac amplifier.



The figure shows two cutoff frequencies f1 and f2. These are the frequencies at which the gain decreases to 0.707 of the maximum gain.

The coupling capacitors C1 and C2 and the bypass capacitor C3 determines the lower cutoff frequency f1. The upper cutoff frequency f2 is determined by the unity gain frequency and voltage gain of the amplifier.

The coupling capacitor C1 is determined by the following equation.

\[f_{c1}=\frac{1}{2 \pi R_3C_1}\]

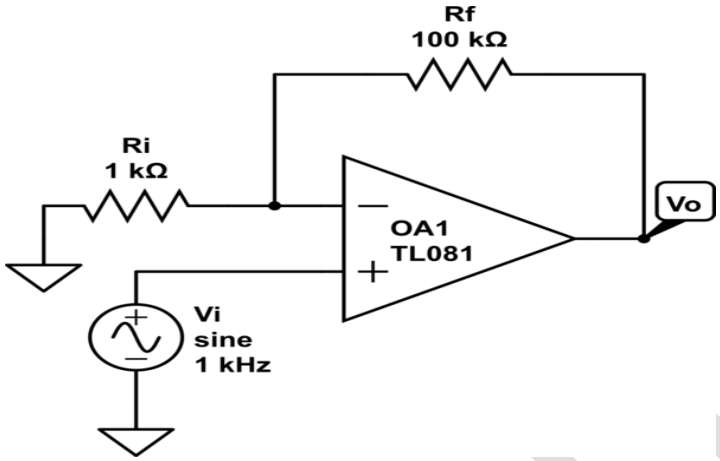
and the coupling capacitor C2 is determined by the following equation.

\[f_{c2}=\frac{1}{2 \pi R_4C_2}\]

The bypass capacitor C3 is determined by the following equation.

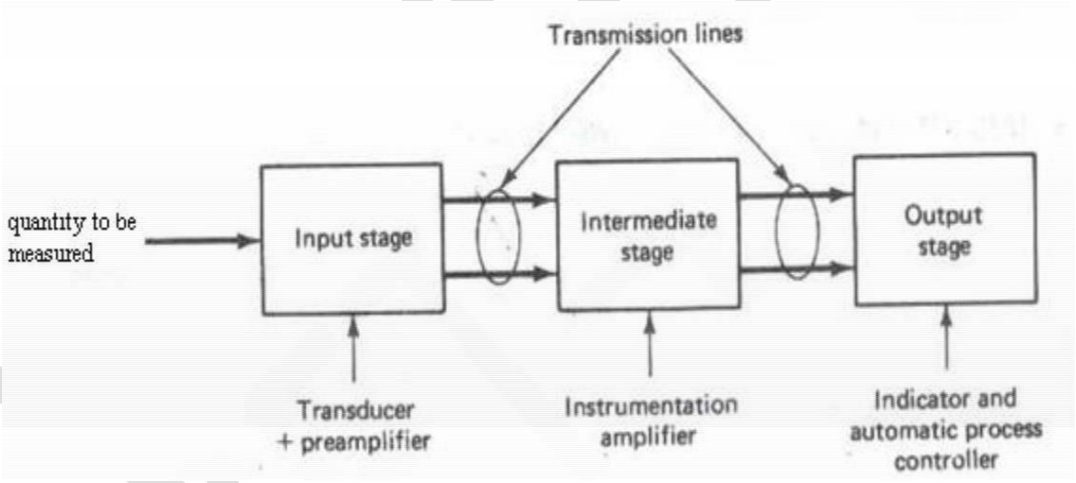
\[f_{c3}=\frac{1}{2 \pi R_2C_3}\]

If we let all the capacitors C1, C2 and C3 be 1uF then we get fc1 as 1.59Hz, fc2 as 15.9Hz and fc3 as 159Hz. Out of these frequencies the dominant frequency is the highest frequency which is 159Hz.



INSTRUMENTATION AMPLIFIER:

In many industrial and consumer applications the measurement and control of physical conditions are very important. For example measurements of temperature and humidity inside a dairy or meat plant permit the operator to make necessary adjustments to maintain product quality. Similarly, precise temperature control of plastic furnace is needed to produce a particular type of plastic.



Instrumentation Amplifier

The transducer is a device that converts one form of energy into another. For example a strain gage when subjected to pressure or force undergoes a change in its resistance (electrical energy).An instrumentation system is used to measure the output signal produced by a transducer and often to control the physical signal producing it. Above fig shows a simplified form of such a system. The input stage is composed of a pre-amplifier and some sort of transducer, depending on the physical quantity to be measured. The output stage may use devices such as meters, oscilloscopes, charts, or magnetic records.

In Figure 1.33 the connecting lines between the blocks represent transmission lines, used especially when the transducer is at a remote test site monitoring hazardous conditions such as high temperatures or liquid levels of flammable chemicals. These transmission lines permit signal transfer from unit to unit. The length of the transmission lines depends primarily on the physical quantities to be monitored and on system requirements.

The signal source of the instrumentation amplifier is the output of the transducer. Although some transducers produce outputs with sufficient strength to per- m.; their use directly, many do not. To amplify the low-level output signal of the transducer so that it can drive the indicator or display is the major function of the instrumentation amplifier. In short, the instrumentation amplifier is intended for precise, low-level signal amplification where low noise, low thermal and time drifts, high input resistance, and accurate closed-loop gain are required. Besides, low power consumption, high common-mode rejection ratio, and high slew rate are desirable for superior performance.

There are many instrumentation operational amplifiers, such as the /LA 725, ICL7605, and LH0036, that make a circuit extremely stable and accurate. These ICs are, however, relatively expensive; they are very precise special-purpose circuits in which most of the electrical parameters, such as offsets, drifts, and power consumption, are minimized, whereas input resistance, CMRR, and supply range are optimized. Some instrumentation amplifiers are even available in modular form to suit special installation requirements.

Obviously, the requirements for instrumentation op-amps are more rigid than those for general-purpose applications. However, where the requirements are not too strict, the general-purpose op-amp can be employed in the differential mode.

We will call such amplifiers differential instrumentation amplifiers. Since most instrumentation systems use a transducer in a bridge circuit, we will consider a simplified differential instrumentation system arrangement using a transducer bridge circuit.

V TO I CONVERTER:

Fig.1.35 shows a voltage to current converter in which load resistor RL is floating (not connected to ground). The input voltage is applied to the non-inverting input terminal and the feedback voltage across R drives the inverting input terminal. This circuit is also called a current series negative feedback, amplifier because the feedback voltage across R depends on the output current iL and is in series with the input difference voltage Vd.

Writing the voltage equation for the input loop.

vin = vd + vf

But vd » since A is very large,therefore,

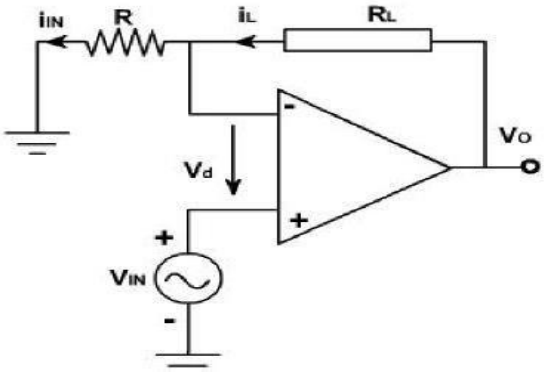
vin = vf vin = R iin

iin = v in / R.

and since input current is zero.

iL = iin = vin ./ R

The value of load resistance does not appear in this equation. Therefore, the output current is independent of the value of load resistance. Thus the input voltage is converted into current; the source must be capable of supplying this load current.

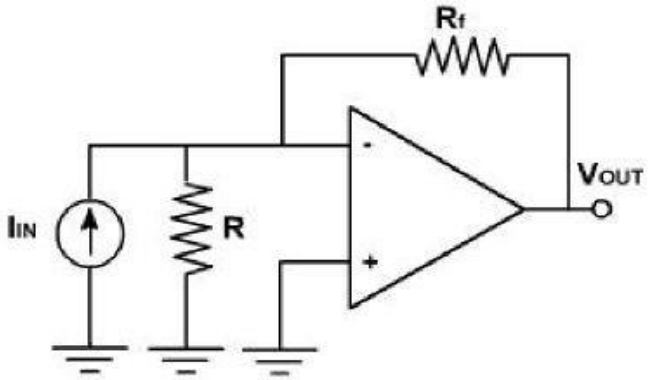


Circuit Diagram of V to I Converter

The maximum load current is VCC/ R. In this circuit v in may be positive or negative.

I TO V CONVERTER:

Current to voltage converter:
The circuit shown in fig is a current to voltage converter.

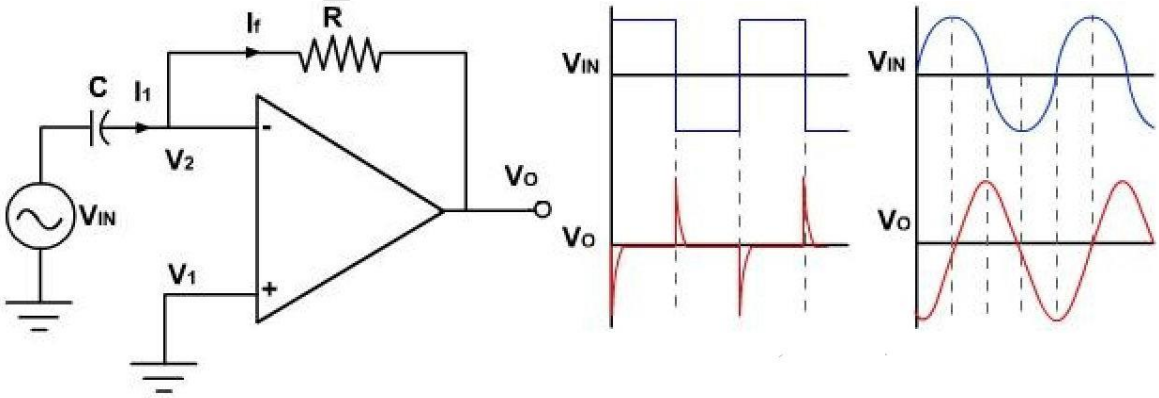


Due to virtual ground the current through R is zero and the input current flows through Rf. Therefore, vout =-Rf * iin

The lower limit on current measure with this circuit is set by the bias current of the inverting input.

DIFFERENTIATOR:

A circuit in which the output voltage waveform is the differentiation of input voltage is called differentiator as shown infig.2.10.



Circuit Diagram of Differentiator

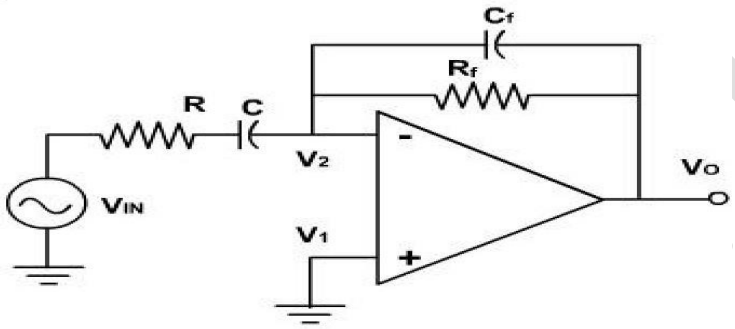
The expression for the output voltage can be obtained from the Kirchoff's current equation written at node v2.

$$\text{Since,} \qquad i_{in} = i_f$$

$$\text{Therefore,} \quad C\frac{d}{dt}(V_{in} - 0) = \frac{0 - V_o}{R}$$

$$V_o = -RC\frac{dV_{in}}{dt}$$

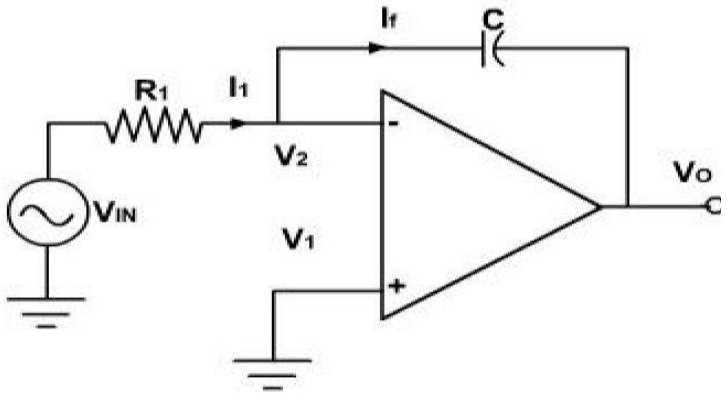
Thus the output vo is equal to the RC times the negative instantaneous rate of change of the input voltage vin with time. A cosine wave input produces sine output. Fig.1.39 also shows the output waveform for different input voltages.



The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to Rf C. As the frequency changes, the gain changes. Also at higher frequencies the circuit is highly susceptible at high frequency noise and noise gets amplified. Both the high frequency noise and problem can be corrected by adding, few components. as shown in fig.1.40.

Integrator:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is called integrator. Fig.1.41, shows an integrator circuit using OPAMP.



Circuit Diagram of Integrator

Here, the feedback element is a capacitor. The current drawn by OPAMP is zero and also the V2 is virtually grounded.

Therefore, i1 = if and v2 = v1 = 0

$$\frac{v_{in} - 0}{R} = C \frac{d(0 - v_o)}{dt}$$

Integrating both sides with respect to time from 0 to t, we get

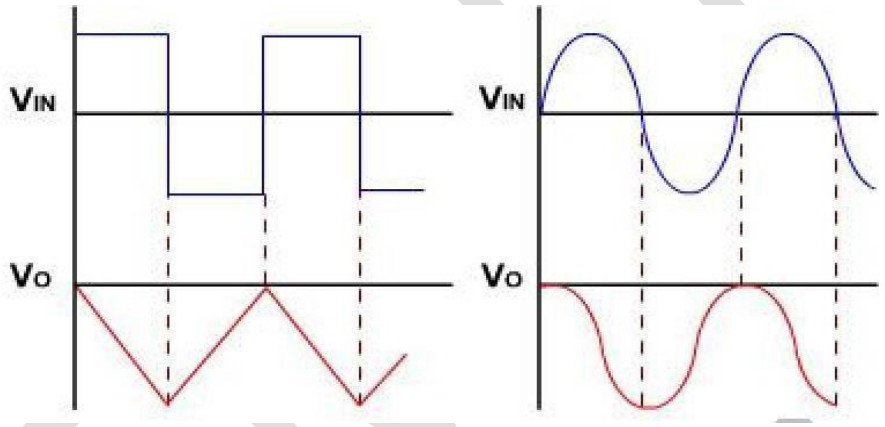
$$\int_0^t \frac{v_{in}}{R} dt = \int_0^t C \frac{d(-v_o)}{dt} dt$$

$$= C(-v_o) + v_o\Big|_{t=0}$$

$$\text{if } V_O|_{t=0} = 0\ V, \text{then}$$

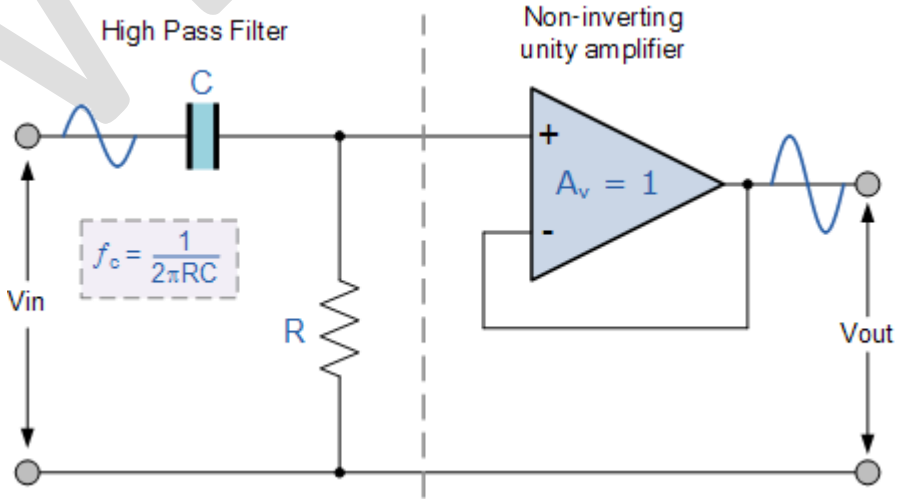
$$v_o = \frac{-1}{R} \int_0^t v_{in}\, dt$$

The output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant RC. If the input is a sine wave the output will be cosine wave. If the input is a square wave, the output will be a triangular wave. For accurate integration, the time period of the input signal T must be longer than or equal to RC.



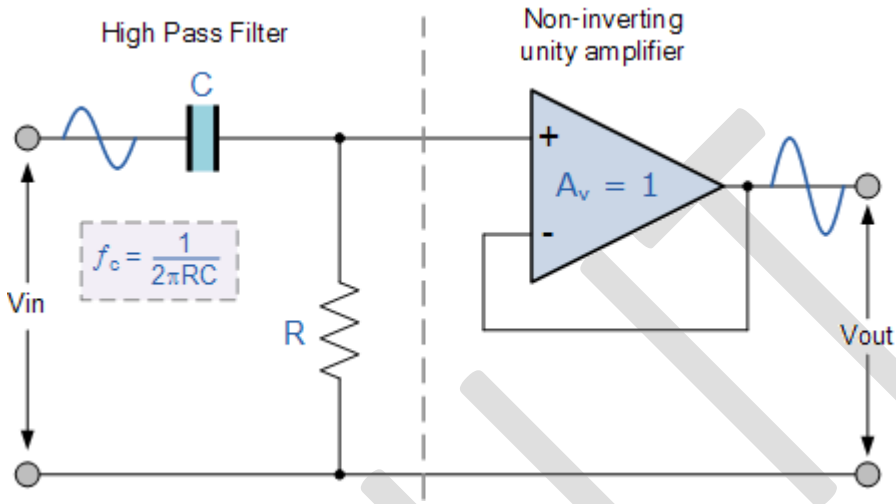
ACTIVE FILTERS :

Active High Pass Filter



The basic electrical operation of an **Active High Pass Filter** (HPF) is exactly the same as we saw for its equivalent RC passive high pass filter circuit, except this time the circuit has an operational amplifier or op-amp included within its filter design providing amplification and gain control.

First Order High Pass Filter



Technically, there is no such thing as an active high pass filter. Unlike Passive High Pass Filters which have an "infinite" frequency response, the maximum pass band frequency response of an active high pass filter is limited by the open-loop characteristics or bandwidth of the operational amplifier being used, making them appear as if they are band pass filters with a high frequency cut-off determined by the selection of op-amp and gain.

In the Operational Amplifier tutorial we saw that the maximum frequency response of an op-amp is limited to the Gain/Bandwidth product or open loop voltage gain (A_V) of the operational amplifier being used giving it a bandwidth limitation, where the closed loop response of the op amp intersects the open loop response.

A commonly available operational amplifier such as the uA741 has a typical "open-loop" (without any feedback) DC voltage gain of about 100dB maximum reducing at a roll off rate of -20dB/Decade (-6db/Octave) as the input frequency increases. The gain of the uA741 reduces until it reaches unity gain, (0dB) or its "transition frequency" (ft) which is about 1MHz. This causes the op-amp to have a frequency response curve very similar to that of a first-order low pass filter and this is shown below.

Gain for an Active High Pass Filter :

$$\text{Voltage Gain, (Av)} = \frac{\text{Vout}}{\text{Vin}} = \frac{A_F\left(\frac{f}{fc}\right)}{\sqrt{1+\left(\frac{f}{fc}\right)^2}}$$

- Where:
- A_F = the Pass band Gain of the filter, (1 + R2/R1)
- f = the Frequency of the Input Signal in Hertz, (Hz)
- fc = the Cut-off Frequency in Hertz, (Hz)

Just like the low pass filter, the operation of a high pass active filter can be verified from the frequency gain equation above as:

- 1. At very low frequencies, $f < fc$ $\quad \frac{\text{Vout}}{\text{Vin}} < A_F$
- 2. At the cut-off frequency, $f = fc$ $\quad \frac{\text{Vout}}{\text{Vin}} = \frac{A_F}{\sqrt{2}} = 0.707\,A_F$
- 3. At very high frequencies, $f > fc$ $\quad \frac{\text{Vout}}{\text{Vin}} \cong A_F$
- Then, the Active High Pass Filter has a gain A_F that increases from 0Hz to the low frequency cut-off point, f_C at 20dB/decade as the frequency increases. At f_C the gain is $0.707A_F$, and after f_C all frequencies are pass band frequencies so the filter has a constant gain A_F with the highest frequency being determined by the closed loop bandwidth of the op-amp.
- When dealing with filter circuits the magnitude of the pass band gain of the circuit is generally expressed in decibels or dB as a function of the voltage gain, and this is defined as:

Magnitude of Voltage Gain in (dB)

$$\text{Av(dB)} = 20\log_{10}\left(\frac{\text{Vout}}{\text{Vin}}\right)$$

$$\therefore -3\text{dB} = 20\log_{10}\left(0.707\,\frac{\text{Vout}}{\text{Vin}}\right)$$

For a first-order filter the frequency response curve of the filter increases by 20dB/decade or 6dB/octave up to the determined cut-off frequency point which is always at -3dB below the

maximum gain value. As with the previous filter circuits, the lower cut-off or corner frequency (fc) can be found by using the same formula:

$$fc = \frac{1}{2\pi RC} \; Hz$$

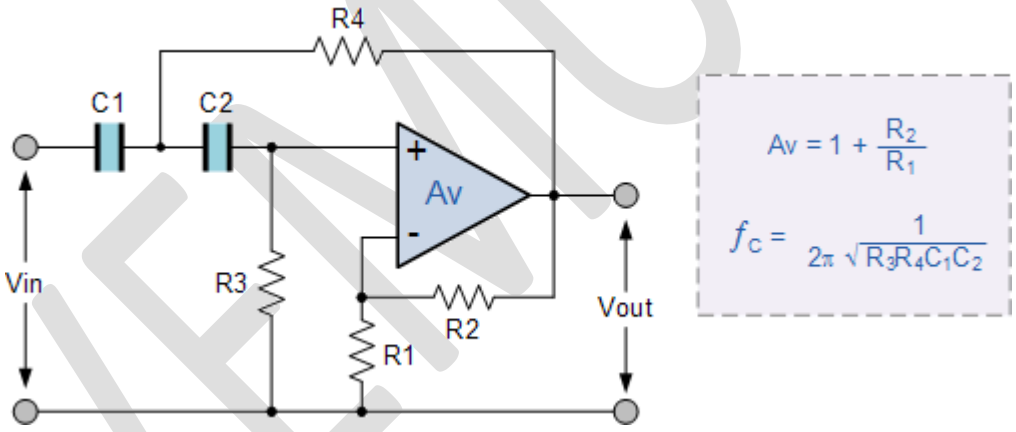
The corresponding phase angle or phase shift of the output signal is the same as that given for the passive RC filter and leads that of the input signal. It is equal to +45° at the cut-off frequency fc value and is given as:

$$Phase\ Shift\ \phi = tan^{-1}\left(\frac{1}{2\pi fRC}\right)$$

A simple first-order active high pass filter can also be made using an inverting operational amplifier configuration as well, and an example of this circuit design is given along with its corresponding frequency response curve. A gain of 40dB has been assumed for the circuit.

Second-order High Pass Active Filter

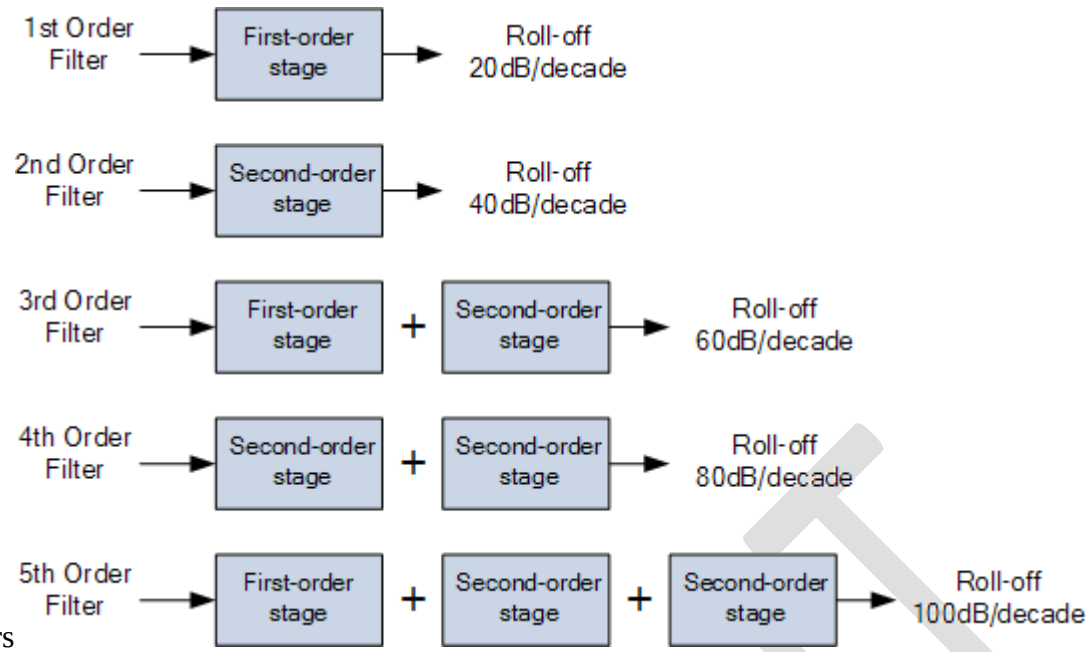
Second-order Active High Pass Filter Circuit



Higher-order high pass active filters, such as third, fourth, fifth, etc are formed simply by cascading together first and second-order filters. For example, a third order high pass filter is formed by cascading in series first and second order filters, a fourth-order high pass filter by cascading two second-order filters together and so on.

Then an Active High Pass Filter with an even order number will consist of only second-order filters, while an odd order number will start with a first-order filter at the beginning as shown.

Cascading Active High Pass

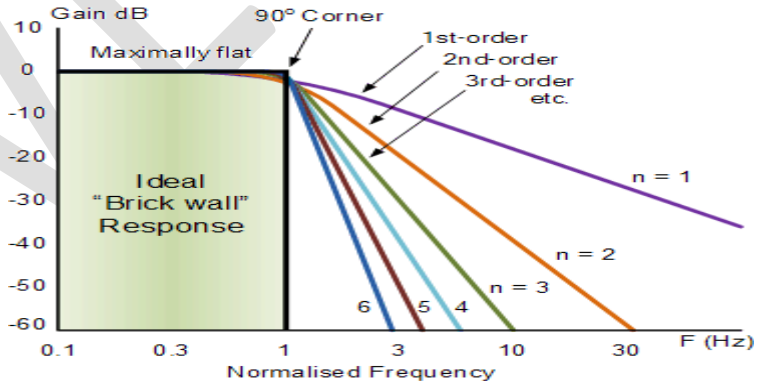


Filters

BUTTERWORTH FILTER DESIGN :

Low Pass Butterworth Filter Design

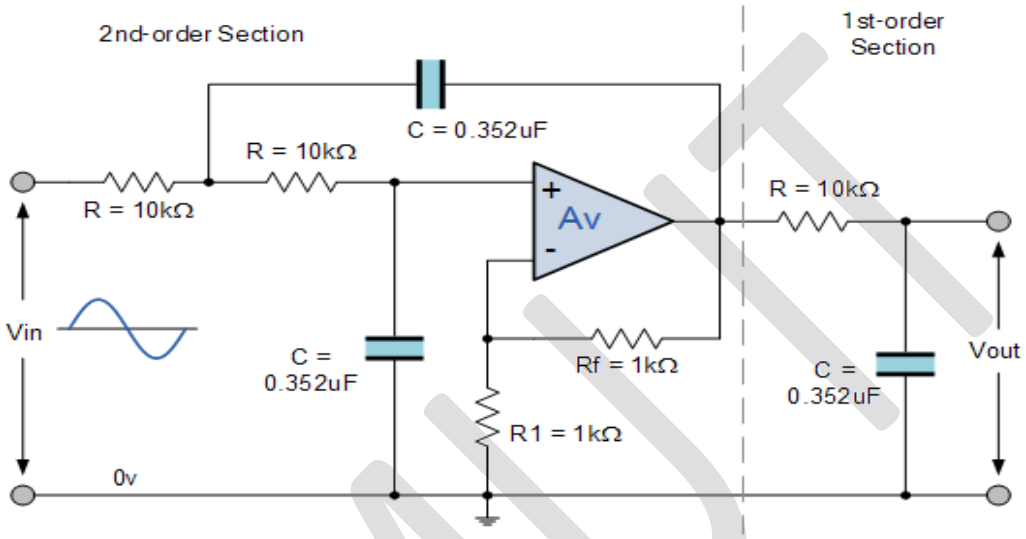
The frequency response of the **Butterworth Filter** approximation function is also often referred to as "maximally flat" (no ripples) response because the pass band is designed to have a frequency response which is as flat as mathematically possible from 0Hz (DC) until the cut-off frequency at -3dB with no ripples. Higher frequencies beyond the cut-off point rolls-off down to zero in the stop band at 20dB/decade or 6dB/octave. This is because it has a "quality factor", "Q" of just 0.707. However, one main disadvantage of the Butterworth filter is that it achieves this pass band flatness at the expense of a wide transition band as the filter changes from the pass band to the stop band. It also has poor phase characteristics as well.



Where the generalised equation representing a “nth” Order Butterworth filter, the frequency response is given as:

$$H_{(j\omega)} = \frac{1}{\sqrt{1+\varepsilon^2\left(\frac{\omega}{\omega_p}\right)^{2n}}}$$

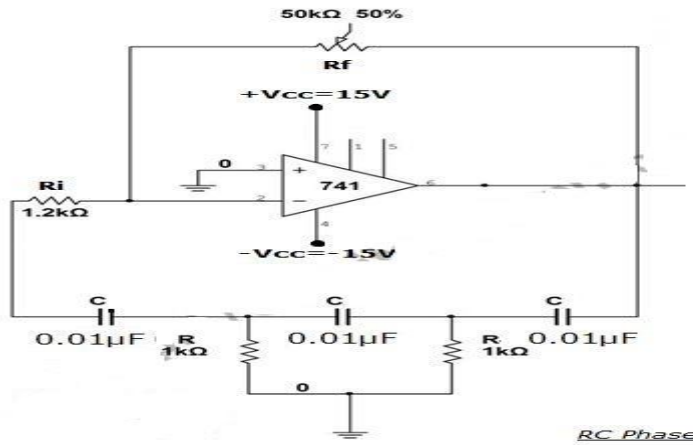
THIRD-ORDER BUTTERWORTH LOW PASS FILTER :



UNIT-IV

OP-AMP APPLICATIONS -2

OSCILLATORS:



RC Phaseshift Oscillator

Working of RC Phase shift oscillator

- The feedback network offers 180 degrees phase shift at the oscillation frequency and the op amp is configured as an Inverting amplifier, it also provide 180 degrees phase shift. Hence to total phase shift around the loop is 360=0degrees, it is essential for sustained oscillations.

  At the oscillation frequency each of the resistor capacitor filter produces a phase shift of 60° so the whole filter circuit produces a phase shift of 180°.

- The energy storage capacity of capacitor in this circuit produces a noise voltage which is similar to a small sine wave, it is then amplified using op amp inverting amplifier.

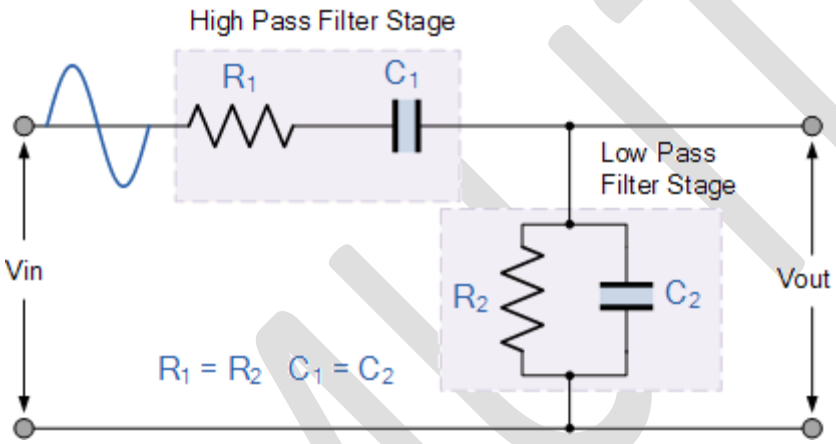
- By taking feedback, the output sine wave also attenuates 1/29 times while passing through the RC network, so the gain of inverting amplifier should be 29 in order to keep loop gain as unity.

- The unity loop gain and 360 degree phase shift are essential for the sustained oscillation.

- RC Oscillators are stable and provide a well-shaped sine wave output with the frequency being proportional to 1/RC and therefore, a wider frequency range is possible when using a variable capacitor.

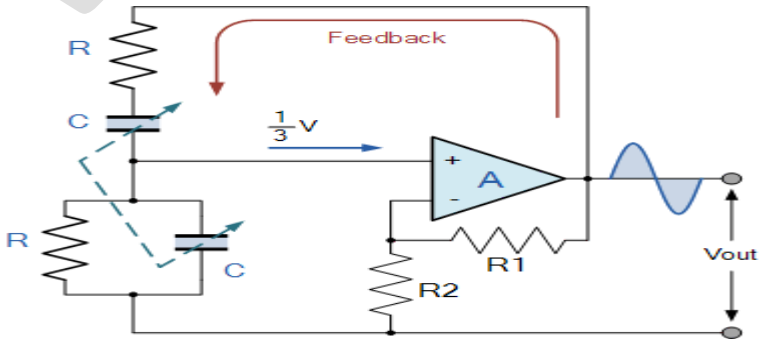
- However, RC Oscillators are restricted to frequency applications because at high frequency the reactance offered by the capacitor is very low so it acts as a short circuit.

Wien Bridge Oscillator



The Wien Bridge Oscillator is so called because the circuit is based on a frequency-selective form of the Wheatstone bridge circuit. The Wien Bridge oscillator is a two-stage RC coupled amplifier circuit that has good stability at its resonant frequency, low distortion and is very easy to tune making it a popular circuit as an audio frequency oscillator but the phase shift of the output signal is considerably different from the previous phase shift RC Oscillator.

The Wien Bridge Oscillator uses a feedback circuit consisting of a series RC circuit connected with a parallel RC of the same component values producing a phase delay or phase advance circuit depending upon the frequency. At the resonant frequency fr the phase shift is 0^o. Consider the circuit below.



The output of the operational amplifier is fed back to both the inputs of the amplifier. One part of the feedback signal is connected to the inverting input terminal (negative feedback) via the resistor divider network of R1 and R2 which allows the amplifiers voltage gain to be adjusted within narrow limits. The other part is fed back to the non-inverting input terminal (positive feedback) via the RC Wien Bridge network.

The RC network is connected in the positive feedback path of the amplifier and has zero phase shift a just one frequency. Then at the selected resonant frequency, (fr) the voltages applied to the inverting and non-inverting inputs will be equal and "in-phase" so the positive feedback will cancel out the negative feedback signal causing the circuit to oscillate.

The voltage gain of the amplifier circuit MUST be equal too or greater than three "Gain = 3" for oscillations to start because as we have seen above, the input is 1/3 of the output. This value, ($Av \geq 3$) is set by the feedback resistor network, R1 and R2 and for a non-inverting amplifier this is given as the ratio 1+(R1/R2).

Also, due to the open-loop gain limitations of operational amplifiers, frequencies above 1MHz are unachievable without the use of special high frequency op-amps.

Determine the maximum and minimum frequency of oscillations of a **Wien Bridge Oscillator** circuit having a resistor of 10kΩ and a variable capacitor of 1nF to 1000nF.

The frequency of oscillations for a Wien Bridge Oscillator is given as:

$$f_r = \frac{1}{2\pi RC}$$

Wien Bridge Oscillator Lowest Frequency

$$f_{min} = \frac{1}{2\pi(10k\Omega)\times(1000\times10^{-9})} = 15.9\,Hz$$

Wien Bridge Oscillator Highest Frequency

$$f_{max} = \frac{1}{2\pi(10k\Omega)\times(1\times10^{-9})} = 15{,}915\,Hz$$

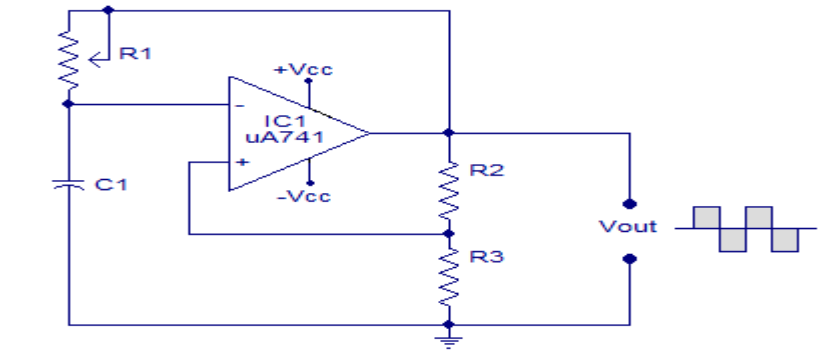
Wien Bridge Oscillator:

Then for oscillations to occur in a **Wien Bridge Oscillator** circuit the following conditions must apply.

- With no input signal a Wien Bridge Oscillator produces continuous output oscillations.
- The Wien Bridge Oscillator can produce a large range of frequencies.

- The Voltage gain of the amplifier must be greater than 3.
- The RC network can be used with a non-inverting amplifier.
- The input resistance of the amplifier must be high compared to R so that the RC network is not overloaded and alter the required conditions.
- The output resistance of the amplifier must be low so that the effect of external loading is minimised.
- Some method of stabilizing the amplitude of the oscillations must be provided. If the voltage gain of the amplifier is too small the desired oscillation will decay and stop. If it is too large the output will saturate to the value of the supply rails and distort.
- With amplitude stabilisation in the form of feedback diodes, oscillations from the Wien Bridge oscillator can continue indefinitely.

SQUARE WAVE GENERATOR USING OPAMP :



Square wave generator using uA741 www.circuitstoday.com

In the circuit diagram capacitor C1 and potentiometer R1 forms the timing part. Resistors R2 and R3 forms a voltage divider network which supplies a fixed fraction of the output voltage into the non-inverting pin of the opamp as a reference voltage.

Working of the square wave generator using uA741

Initially the voltage across the capacitor C1 will be zero and the output of the opamp will be high. As a result the capacitor C1 starts charging to positive voltage through potentiometer R1. When the C1 is charged to a level so that the voltage at the inverting terminal of the opamp is above the voltage at the non-inverting terminal, the output of the opamp swings to negative. The capacitor quickly discharges through R1 and then starts charging to negative voltage. When the C1 is charged to a negative voltage so that the voltage at the inverting input more negative than that of the non-inverting pin, the output of the opamp swings back to positive voltage. Now the capacitor quickly discharges the negative voltage through R1 and starts charging to positive voltage. This cycle is repeated endlessly and the result will a continuous square wave swinging between +Vcc and -Vcc at the output.

The time period of the output of the uA741 square wave generator can be expressed using the following equation:

$$T = 2 \times 2.303\ R_1C_1 \log_{10} \left(\frac{2R_3 + R_2}{R_2}\right) \text{ Second}$$

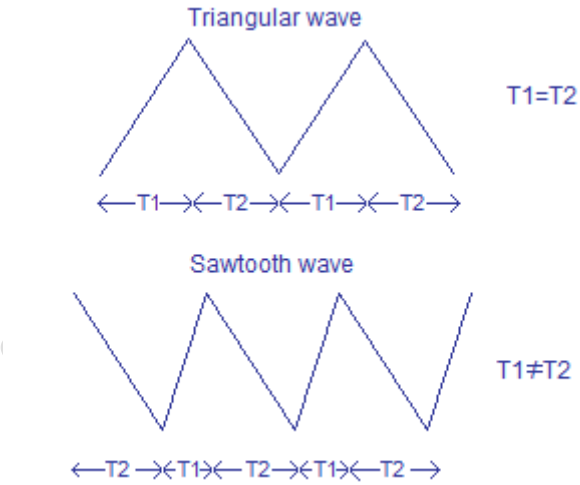
The common practice is to make the R3 equal to R2. Then the equation for the time period can be simplified as:

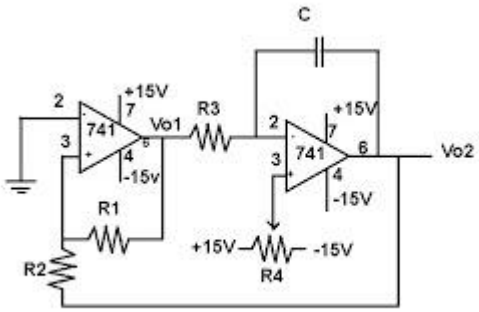
T=2.1976R1C1

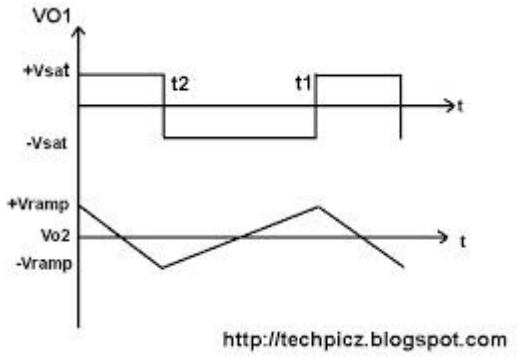
The frequency can be determined by the equation: ***F=1/T***

Sawtooth wave generator:

Difference between Traingular Wave & Sawtooth wave form





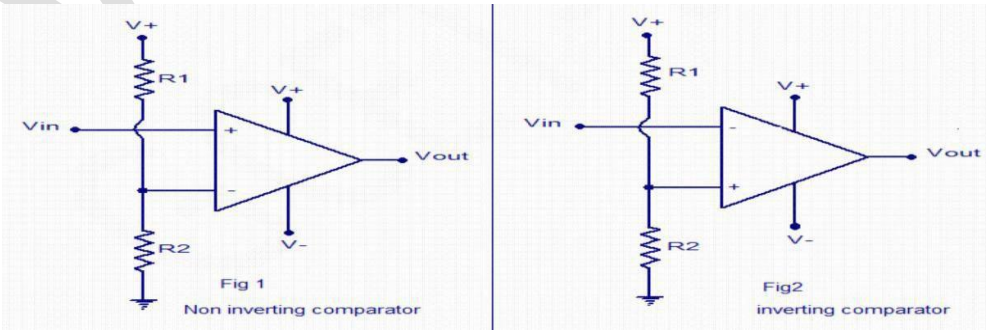


The difference between the triangular wave and sawtooth waveform is that the rise time of triangular wave is always equal to its fall of time while in saw tooth generator, rise time may be much higher than its fall of tim , vise versa . The triangular wave generator can be converted in to a sawtooth wave generator by injencting a variable dc voltage into the non inverting terminal of the integrator.

In this circuit a potentiometer is used (47K) . Use of the potentiometer is when the wiper moves towards -V ,the rise tim of the sawtooth become longerthan the fall time. If the wiper moves towards +V , the fall time becomes more than the rise time. Reason is when comparator output is at -ve saturaion. When wiper moves to -ve supply, a negative voltage is added to inverting terminal. This causes the potential difference across R1 decreases and hence the current through the resistor and capacitor decreases . Then slope of the output, I/C decreases and un tern rise time decreases. When the compartor output goes positive , due to presence of negative voltage at the inverting terminal, potential difference of across the resistor R1 increases and hebce Current increases. Then slope increases and fall time decreases. And obtained output as sawtooth wave.

COMPARATOR:

Voltage comparator is a circuit which compares two voltages and switches the output to either high or low state depending upon which voltage is higher. A voltage comparator based on opamp is shown here. Fig2.14 shows a voltage comparator in inverting mode and Fig shows a voltage comparator in non inverting mode.



Non inverting comparator:

In non inverting comparator the reference voltage is applied to the inverting input and the

voltage to be compared is applied to the non inverting input. Whenever the voltage to be compared (Vin) goes above the reference voltage , the output of the opamp swings to positive saturation (V+) and vice versa. Actually what happens is that, the difference between Vin and Vref, (Vin – Vref) will be a positive value and is amplified to infinity by the opamp. Since there is no feedback resistor Rf, the opamp is in open loop mode and so the voltage gain (Av) will be close to infinity. So the output voltage swings to the maximum possible value ie; V+. Remember the equation Av = 1 + (Rf/R1).

When the Vin goes below Vref, the reverse occurs.

Inverting comparator.

In the case of an inverting comparator, the reference voltage is applied to the non inverting input and voltage to be compared is applied to the inverting input. Whenever the input voltage (Vin) goes above the Vref, the output of the op-amp swings to negative saturation. Here the difference between two voltages (Vin-Vref) is inverted and amplified to infinity by the op-amp. Remember the equation Av = -Rf/R1. The equation for voltage gain in the inverting mode is Av = -Rf/R1.Since there is no feedback resistor, the gain will be close to infinity and the output voltage will be as negative as possible i.e., V-.

Practical voltage comparator circuit.

A practical non inverting comparator based on uA741 opamp is shown below. Here the reference voltage is set using the voltage divider network comprising of R1 and R2. The equation is Vref = (V+/ (R1 + R2)) x R2. Substituting the values given in the circuit diagram into this equation gives Vref = 6V. Whenever Vin goes above 6V, the output swings to ~+12V DC and vice versa. The circuit is powered from a +/- 12V DC dual supply.

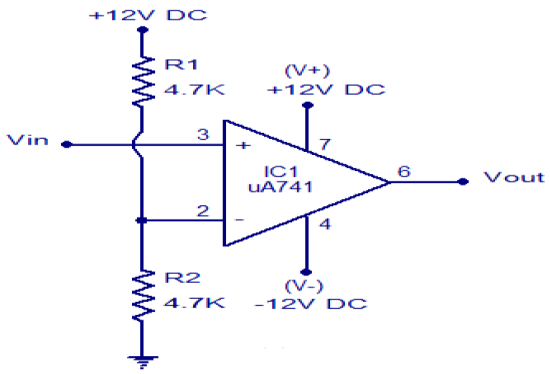
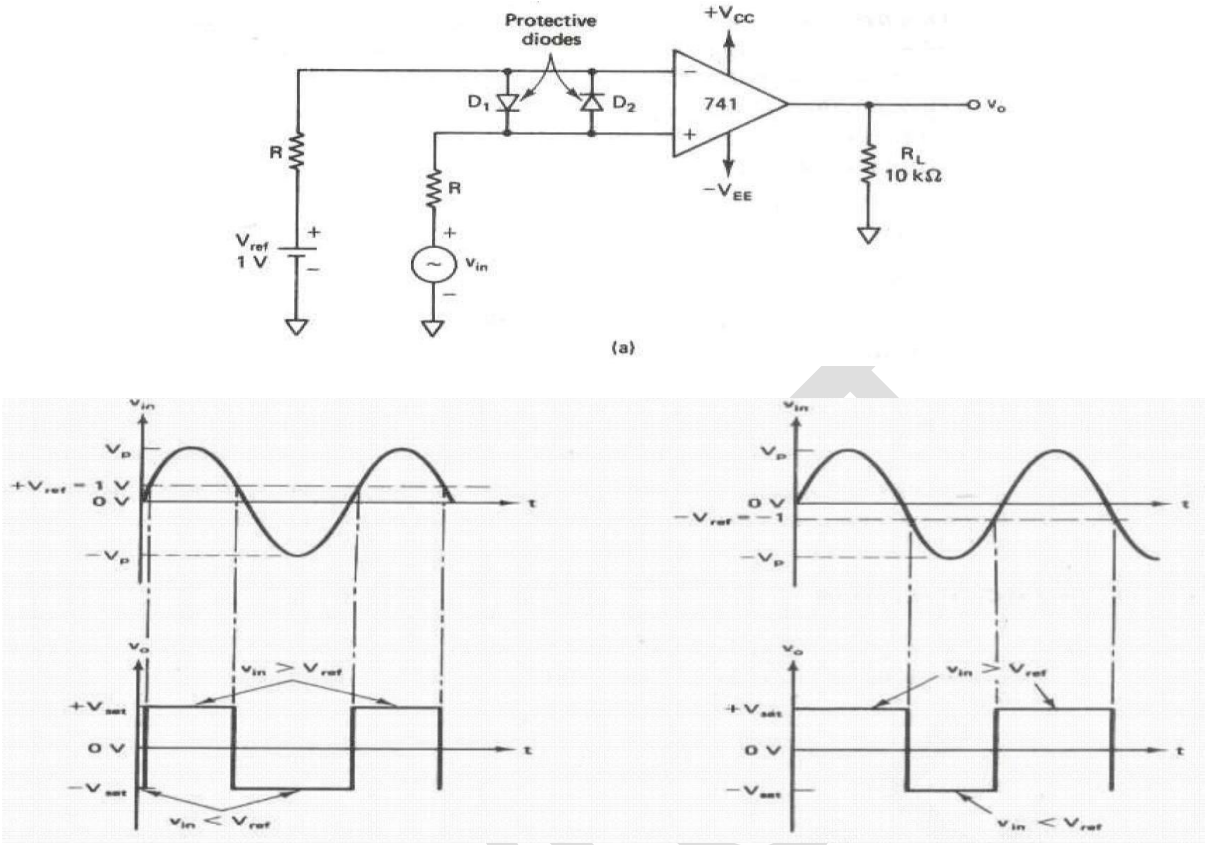


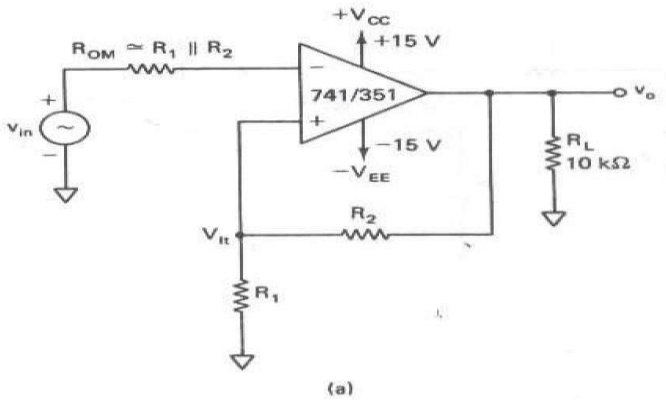
Fig 1.44 Circuit diagram of Practical voltage comparator.

OP-AMP VOLTAGE COMPARATOR :



SCHMITT TRIGGER:

Below fig shows an inverting comparator with +ve feed back. This circuit converts an irregular shaped wave forms to a square wave form or pulse. The circuit is known as schmitt trigger or squaring circuit. The i/p voltage being triggers the o/p Vo every time it exceeds certain voltage levels called the upper threshold voltage Vut and lower threshold voltage Vlt as shown in fig 1.45 (b).In fig 1.45 (a) these threshold voltages are obtained by using the voltage divider R1, R2, where the voltage across R1 is F/B to +ve i/p. The voltage across R1 is a variable reference, threshold voltage that depends on the value and polarity of the output voltage Vo. when Vo=+Vsat, the voltage across R1 is called the upper threshold voltage Vut.



The input voltage Vin must be slightly more positive then Vut in order to cause the out put Vo to switch from +Vsat to –Vsat.as long as Vin less then Vut,Vo is at +Vsat. using the voltage divider rule, On the other hand,when Vo=-Vsat, the voltage across R1 is referred to as the lower threshold voltage,Vlt.Vin must be slightly more negative than Vlt.in order to cause Vo to switch from-Vsat to +Vsat.in other words,for Vin values greater than Vlt,Vo is at – Vsat.Vlt is given by the following equation; Thus if the threshold voltages Vut and Vlt are made large than the input noise voltages, the positive fed back will eliminate the false output transitions.Also the +ve feedback because of its regenerative action will make Vo switch faster between +Vsat and – Vsat.

INTRODUCTION TO 555 TIMER:

One of the most versatile linear integrated circuits is the 555 timer. A sample of these applications includes mono-stable and astable multivibrators, dc-dc converters, digital logic probes, waveform generators, analog frequency meters and tachometers, temperature measurement and control, infrared transmitters, burglar and toxic gas alarms, voltage regulators, electric eyes, and many others.

The 555 is a monolithic timing circuit that can produce accurate and highly stable time delays or oscillation. The timer basically operates in one of the two modes: either as monostable (one-shot) multivibrator or as an astable (free running) multivibrator. The device is available as an 8-pin metal can, an 8-pin mini DIP, or a 14-pin DIP.

The SE555 is designed for the operating temperature range from -55°Cto + 125°C, while the NE555 operates over a temperature range of 0° to +70°C. The important features of the 555 timer are these: it operates on +5 to + 18 V supply voltage in both free-running (astable) and one-shot (monostable) modes; it has an adjustable duty cycle; timing is from microseconds through hours; it has a high current output; it can source or sink 200 mA; the output can drive TTL and has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature, or equivalently 0.005%/°C.

Like general-purpose op-amps, the 555 timer is reliable, easy to us, and low cost.

Pin 1: Ground.

All voltages are measured with respect to this terminal.

Pin 2: Trigger.

The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. The output is low if the voltage at this pin is greater than 2/3 VCC. However,when a negative-going pulse of amplitude larger than 1/3 VCC is applied to this pin, the comparator 2 output goes low, which in turn switches the output of the timer high. The output remains high as

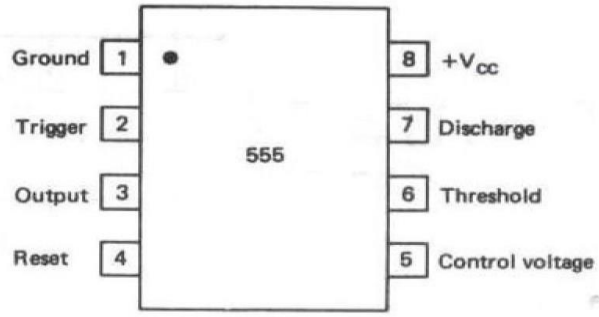
long as the trigger terminal is held at a low voltage.

Pin 3: Output.

There are two ways a load can be connected to the output terminal: either between pin 3 and ground (pin 1) or between pin 3 and supply voltage + VCC (pin 8). When the output is low, the load current flows through the load connected between pin 3 and + VCC into the output terminal and is called the sink current.

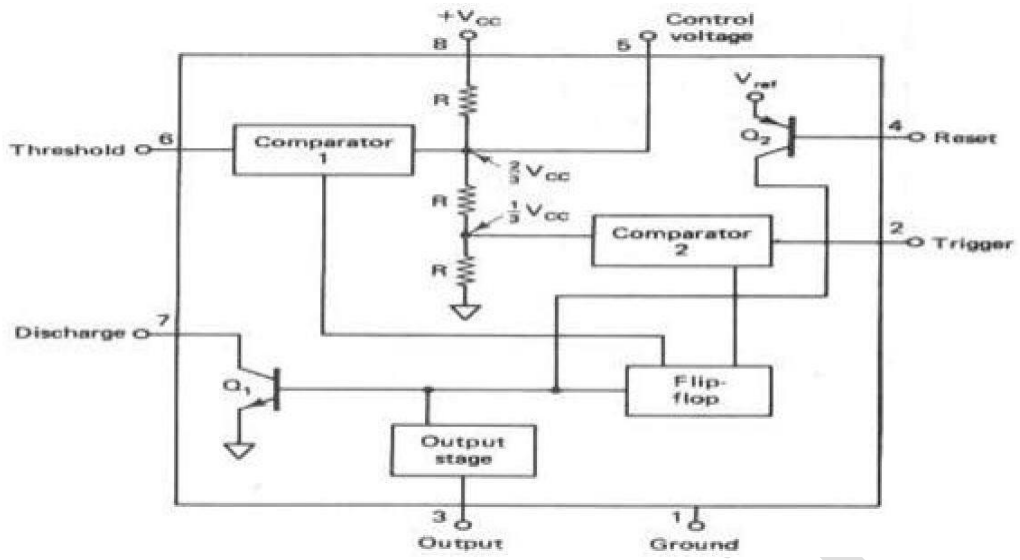
However, the current through the grounded load is zero when the output is low. For this reason, the load connected between pin 3 and + VCC is called that connected between pin 3 and ground is called the normally off load.

On the other hand, when the output is high, the current through the load connected between pin 3and + VCC (normally on load) is zero. However, the output terminal supplies current to the normally off load. This current is called the source current. The maximum value of sink or source current is 200 mA.



Pin 4: Reset.

The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to + VCC to avoid any possibility of false triggering.



Pin 5: Control voltage.

An external voltage applied to this terminal changes the threshold as well as the trigger voltage. In other words, by imposing a voltage on this pin or by connecting a pot between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with a 0.01-μF capacitor to prevent any noise problems.

Pin 6: Threshold. This is the non-inverting input terminal of comparator 1, which monitors the voltage across the external capacitor. When the voltage at this pin is threshold voltage 2/3 V, the output of comparator 1 goes high, which in turn switches the output of the timer low.

Pin 7: Discharge. This pin is connected internally to the collector of transistor Q1, as shown in Figure 2.1(b). When the output is high, Q1 is off and acts as an open circuit to the external capacitor C connected across it. On the other hand, when the output is low, Q1 is saturated and acts as a short circuit, shorting out the external capacitor C to ground.

Pin 8: + VCC.

The supply voltage of +5 V to +18 is applied to this pin with respect to ground (pin1).

FUNCTIONAL BLOCK DIAGRAM OF 555 TIMER:

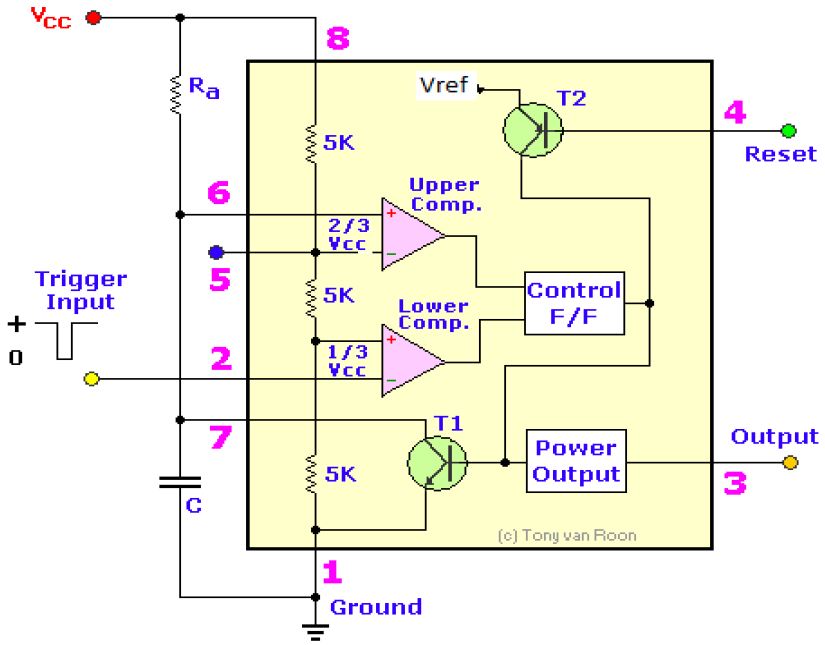


Fig 2.1(b) Block diagram of timer

THE 555 AS A MONOSTABLE MULTIVIBRATOR

A monostable multivibrator, often called a one-shot multivibrator, is a pulse- generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer.

In a stable or standby state the output of the circuit is approximately zero or at logic- low level. When an external trigger pulse is applied, the output is forced to go high (≈VCC). The time the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats.

The monostable circuit has only one stable state (output low), hence the name mono-stable. Normally, the output of the mono- stable multivibrator is low. Fig 2.2 (a) shows the 555 configured for monostable operation. To better explain the circuit's operation, the internal block diagram is included in Fig 2.2(b).

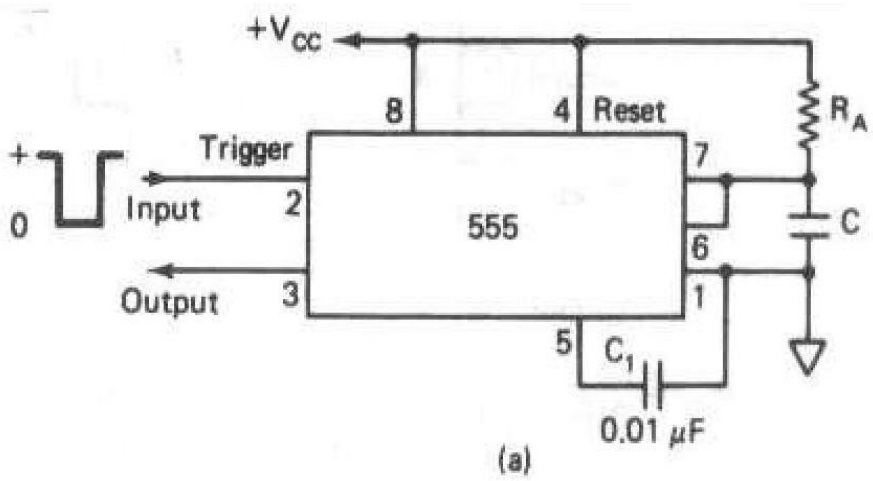


Figure 2.2(a) IC555 as Monostable Multivibrator

Mono-stable operation:

According to Fig 2.2(b), initially when the output is low, that is, the circuit is in a stable state, transistor Q is on and capacitor C is shorted out to ground. However, upon application of a negative trigger pulse to pin 2, transistor Q is turned off, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up toward Vcc through RA.

However, when the voltage across the capacitor equals 2/3 Va., comparator I 's output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time, the output of the flip-flop turns transistor Q on, and hence capacitor C rapidly discharges through the transistor.

The output of the monostable remains low until a trigger pulse is again applied. Then the cycle repeats. Figure 4-2(c) shows the trigger input, output voltage, and capacitor voltage waveforms. As shown here, the pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also, the trigger pulse must be a negative-going input signal with amplitude larger than 1/3 the time during which the output remains high is given by where

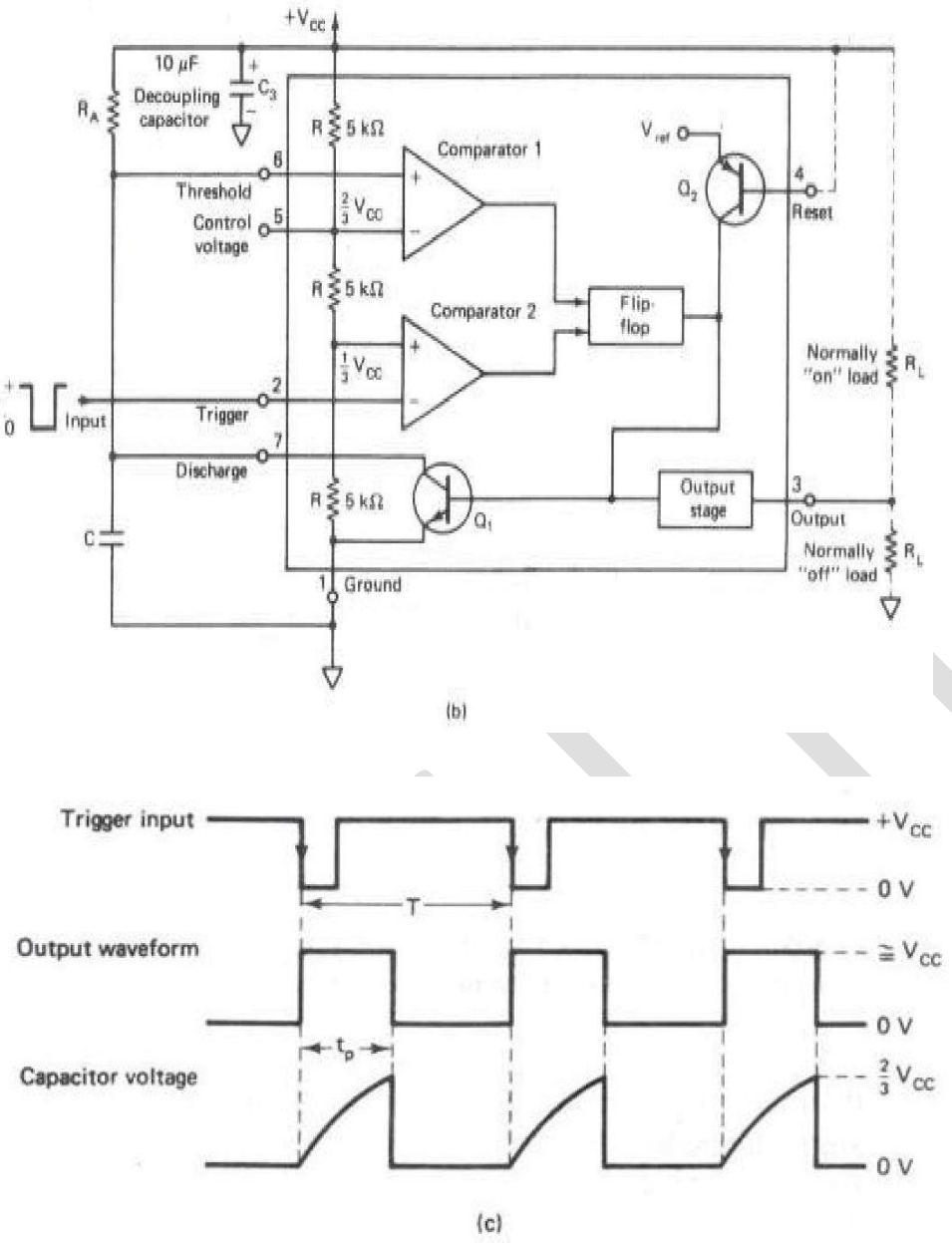


Fig.2.2 (b) 555 connected as a Monostable Multivibrator (c) input and output waveforms

Where RA is in ohms and C is in farads. Figure 2.2(c) shows a graph of the various combinations of RA and C necessary to produce desired time delays. Note that this graph can only be used as a guideline and gives only the approximate value of RA and C for a given time delay. Once triggered, the circuit's output will remain in the high state until the set time 1, elapses. The output will not change its state even if an input trigger is applied again during this time interval T. However, the circuit can be reset during the timing cycle by applying a negative pulse to the reset terminal. The output will then remain in the low state until a trigger is again applied.

Often in practice a decoupling capacitor (10 F) is used between + (pin 8) and ground (pin

1) to eliminate unwanted voltage spikes in the output waveform. Sometimes, to prevent any possibility of mistriggering the monostable multivibrator on positive pulse edges, a wave shapingcircuit consisting of R, C2, and diode D is connected between the trigger input pin 2 and pin 8, as shown in Figure 4-3. The values of R and C2 should be selected so that the time constant RC2 is smaller than the output pulse width.

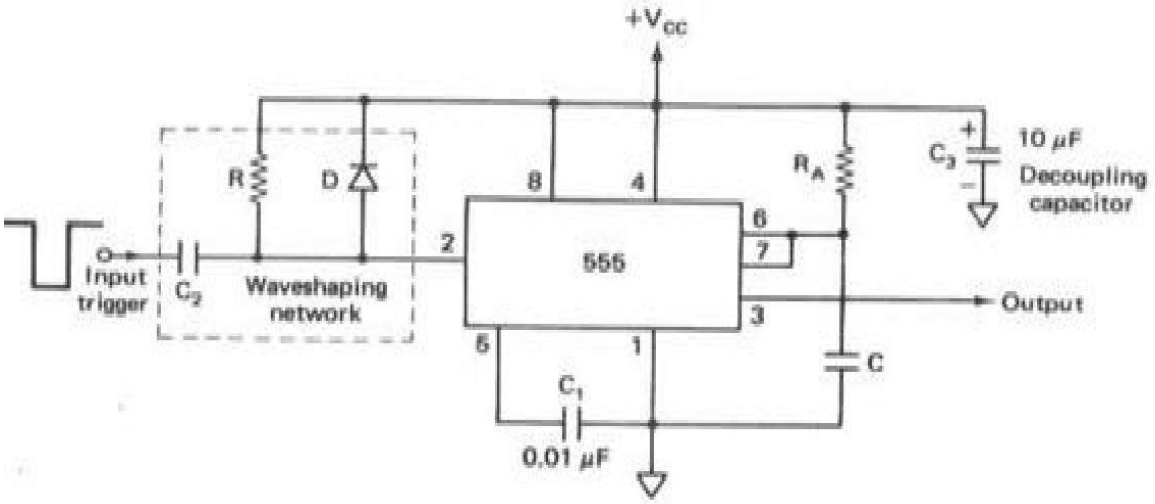


Fig.2.3 Monostable Multivibrator with wave shaping network to prevent +ve pulse edge triggering

Monostable Multivibrator Applications

(a) Frequency divider: The monostable multivibrator of Figure 2.2(a) can be used as a frequency divider by adjusting the length of the timing cycle tp, with respect to the tine period T of the trigger input signal applied to pin 2. To use monostable multivibrator as a divide-by-2 circuit, the timing interval tp must be slightly larger than the time period T of the trigger input signal, as shown in Figure 2.4. By the same concept, to use the monostable multivibrator as a divide-by-3 circuit, tp must be slightly larger than twice the period of the input trigger signal, and so on. The frequency-divider application is possible because the monostable multivibrator cannot be triggered during the timing cycle.

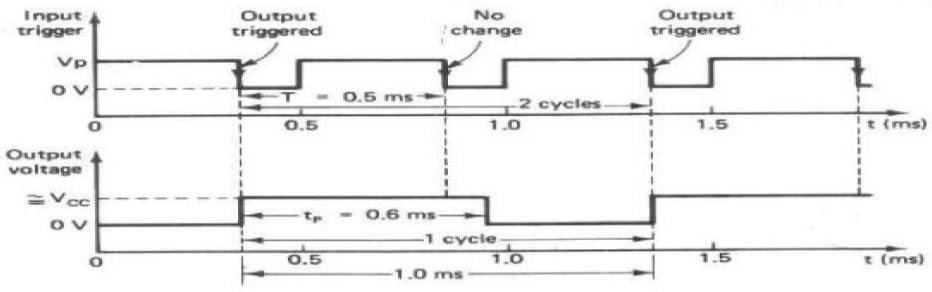


Fig 2.4 input and output waveforms of a monostable multi vibrator as a divide-by-2 network

(b) Pulse stretcher: This application makes use of the fact that the output pulse width (timing interval) of the rnonostable multivibrator is of longer duration than the negative pulse width of the input trigger. As such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name pulse stretcher. Often, narrow-pulse- width signals are not suitable for driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but is not visible to the eye because its on time is infinitesimally small compared to its off time. The 555 pulse stretcher can be used to remedy this problem

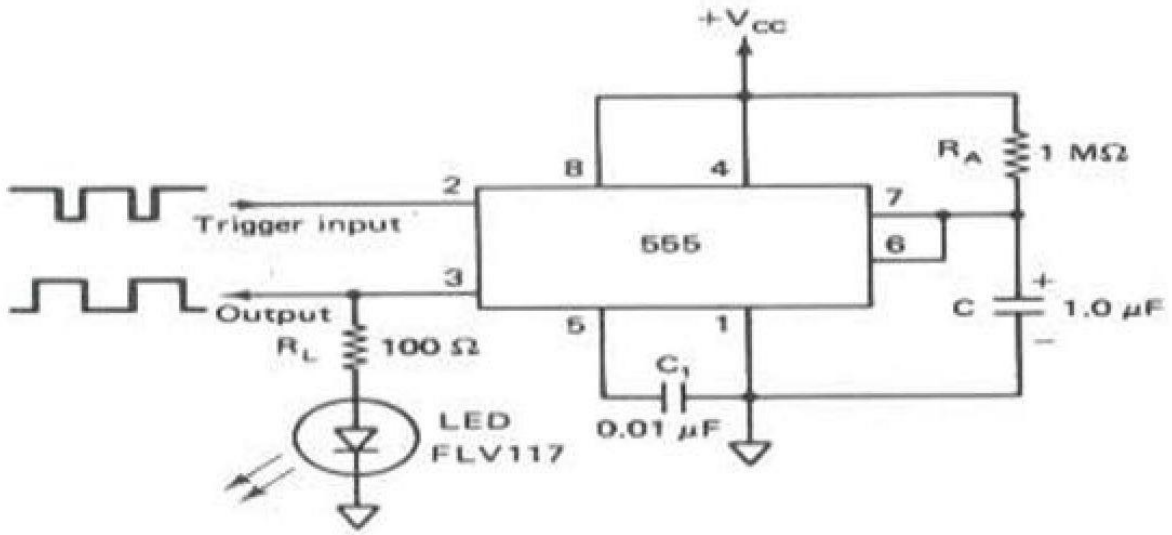


Fig 2.5 Monostable multi vibrator as a Pulse stretcher

Figure 2.5 shows a basic monostable used as a pulse stretcher with an LED indicator at the output. The LED will be on during the timing interval tp = 1.1RAC, which can be varied by changing the value of RA and/or C.

555 AS AN ASTABLE MULTIVIBRATOR:

The 555 as an Astable Multivibrator, often called a free-running multivibrator, is a rectangular-wave-generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determined by the two resistors and a capacitor, which are externally connected to the 555 timer. Fig 4-6(a) shows the 555 timer connected as an astable multivibrator. Initially, when the output is high, capacitor C starts charging toward V through RA and R8. However as soon as voltage across the capacitor equals 2/3 Vcc, comparator I triggers the flip flop, and the output switches low. Now capacitor C starts discharging through R8 and transistor Q. When the voltage across C equals 1/3 comparator 2's

output triggers the flip-flop, and the output goes high. Then the cycle repeats.

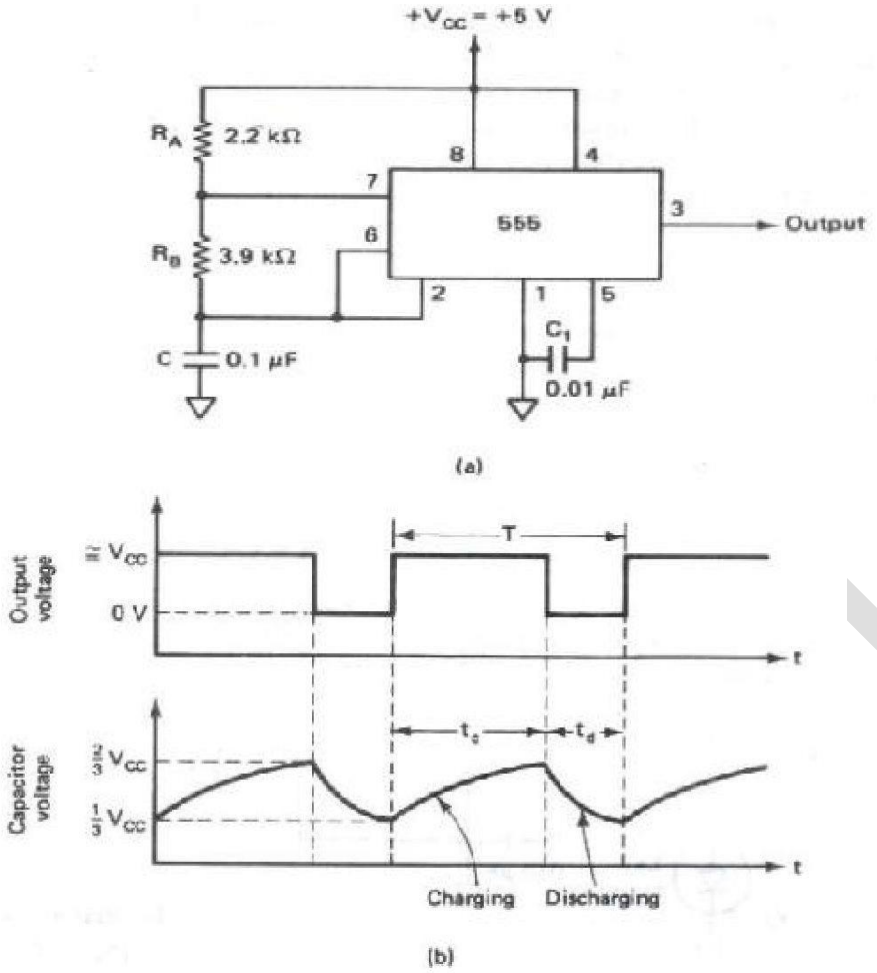


Fig 4-6 The 555 as a Astable Multivibrator (a)Circuit(b)Voltage across Capacitor and O/P waveforms.

The output voltage and capacitor voltage waveforms are shown in Figure 2.6(b). As shown in this figure, the capacitor is periodically charged and discharged between 2/3 Vcc and 1/3 V, respectively. The time during which the capacitor charges from 1/3 V to 2/3 V. is equal to the time the output is high and is given by

$$t_C = 0.69(R_A + R_B)C$$

where RA and R3 are in ohms and C is in farads. Similarly, the time during which the capacitor discharges from 2/3 V to 1/3 V is equal to the time the output is low and is given by

$$t_d = 0.69(R_B)C$$

where RB is in ohms and C is in farads. Thus the total period of the output waveform is

$$T = t_C + t_d = 0.69(R_A + 2R_B)C$$

This, in turn, gives the frequency of oscillation as

$$f_o = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

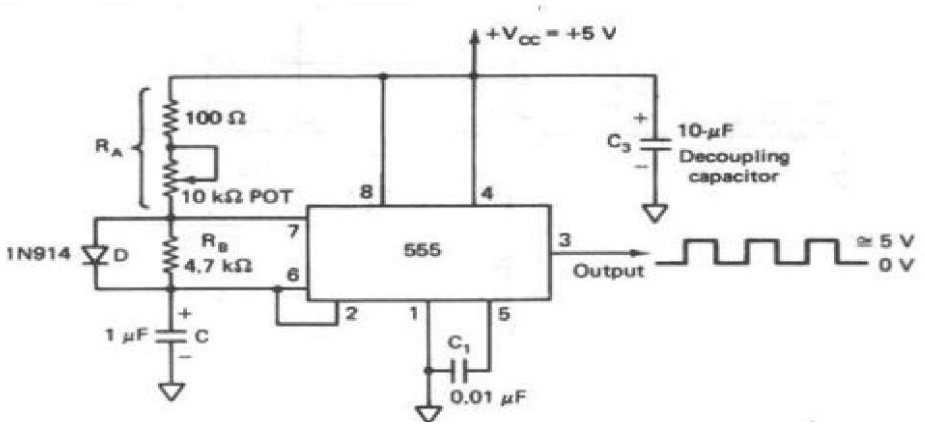
Above equation indicates that the frequency fo is independent of the supply voltage V. Often the term duty cycle is used in conjunction with the astable multivibrator . The duty cycle is the ratio of the time t during which the output is high to the total time period T. It is generally expressed as a percentage. In equation form,

$$\%\, duty\, cycle = \frac{t_C}{T} \times 100$$

$$= \frac{R_A + 2R_B}{R_A + 2R_B} \times 100$$

Astable Multivibrator Applications:

Square-wave oscillator: Without reducing RA = 0 , the astable multivibrator can be used to produce a square wave output simply by connecting diode D across resistor RB, as shown in Figure 4-7. The capacitor C charges through RA and diode D to approximately 2/3 Vcc and discharges through RB and terminal 7 until the capacitor voltage equals approximately 1/3 Vcc; then the cycle repeats. To obtain a square wave output (50% duty cycle), RA must be a combination of a fixed resistor and potentiometer so that the potentiorneter can be adjusted for the exact square wave.



Free-running ramp generator: The astable multivibrator can be used as a free-running ramp generator when resistors RA and R3 are replaced by a current mirror. Figure 2.8(a) shows an astable multivibrator configured to perform this function. The current mirror starts charging capacitor C toward Vcc at a constant rate.

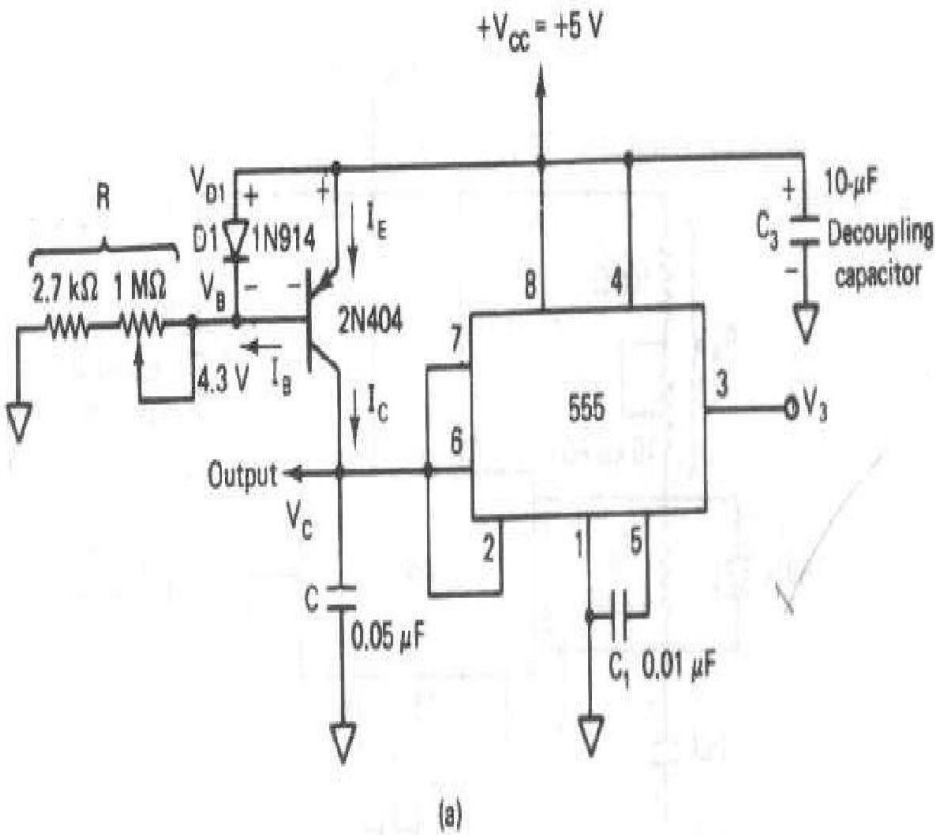
When voltage across C equals 2/3 Vcc, comparator 1 turns transistor Q on, and C

rapidly discharges through transistor Q. However, when the discharge voltage across C is approximately equal to 1/3 Vcc, comparator 2 switches transistor Q off, and then capacitor C starts charging up again. Thus the charge— discharge cycle keeps repeating. The discharging time of the capacitor is relatively negligible compared to its charging time; hence, for all practical purposes, the time period of the ramp waveform is equal to the charging time and is approximately given by

$$T = \frac{V_{cc}C}{3I_C}$$

Where I = (Vcc — VBE)/R = constant current in amperes and C is in farads. Therefore, the free running frequency of the ramp generator is

$$f_o = \frac{3I_C}{V_{cc}C}$$



(a)

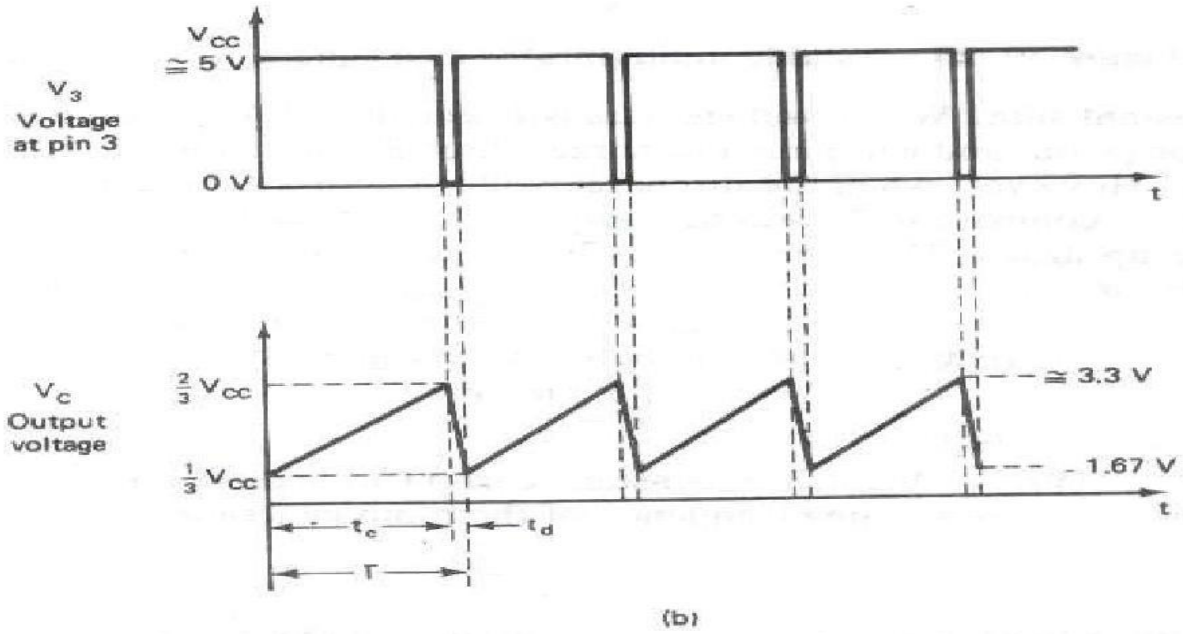


Fig 2.8(a) Free Running ramp generator (b) Output waveform.

PHASE-LOCKED LOOPS:

The phase-locked loop principle has been used in applications such as FM (frequency modulation) stereo decoders, motor speed controls, tracking filters, frequency synthesized transmitters and receivers, FM demodulators, frequency shift keying (FSK) decoders, and a generation of local oscillator frequencies in TV and in FM tuners.

Today the phase-locked loop is even available as a single package, typical examples of which include the Signetics SE/NE 560 series (the 560, 561, 562, 564, 565, and 567). However, for more economical operation, discrete ICs can be used to construct a phase-locked loop.

Block Schematic and Operating Principle

Figure 2.10 shows the phase-locked loop (PLL) in its basic form. As illustrated in this figure, the phase-locked loop consists of (1) a phase detector, (2) a low-pass filter, and, (3) a voltage controlled oscillator

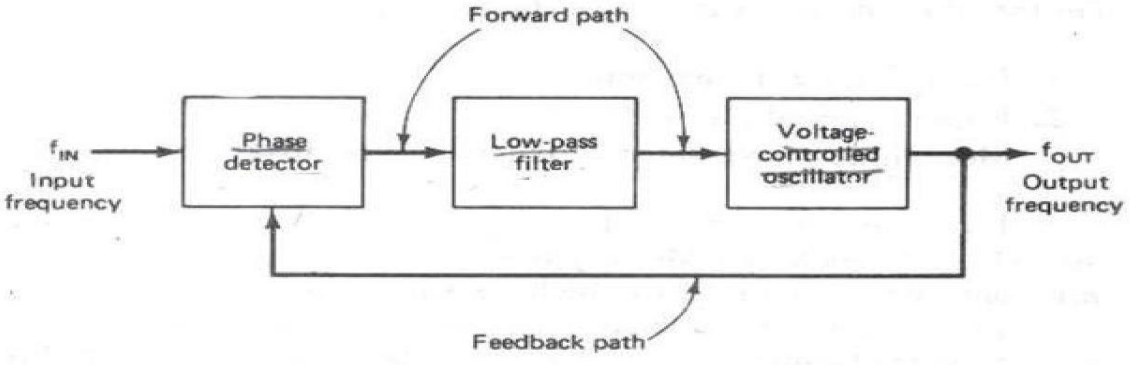


Fig 2.10 Block Diagram of Phase Locked Loop

The phase detectors or comparator compares the input frequency fIN with the feedback frequency fOUT.. The output voltage of the phase detector is a dc voltage and therefore is often referred to as the error voltage. The output of the phase is then applied to the low-pass filter, which removes the high-frequency noise and produces a dc level.

This dc level, in turn, is the input to the voltage-controlled oscillator (VCO). The filter also helps in establishing the dynamic characteristics of the PLL circuit. The output frequency of the VCO is directly proportional to the input dc level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequencies. In short, the phase-locked loop goes through three states: free- running, capture, and phase lock. Before the input is applied, the phase-locked loop is in the free-running state. Once the input frequency is applied, the VCO frequency starts to change and the phase-locked loop is said to be in the capture mode. The VCO frequency continues to change until it equals the input frequency, and the phase- locked loop is then in the phase-locked state. When phase locked, the loop tracks any change in the input frequency through its repetitive action. Before studying the specialized phase-locked-loop IC, we shall consider the discrete phase-locked loop, which may be assembled by combining a phase detector, a low-pass filter, and a voltage-controlled oscillator.

(a) Phase detector:

The phase detector compares the input frequency and the VCO frequency and generates a dc voltage that is proportional to the phase difference between the two frequencies. Depending on the analog or digital phase detector used, the PLL is either called an analog or digital type, respectively. Even though most of the monolithic PLL integrated circuits use analog phase detectors, the majority of discrete phase detectors in use are of the digital type mainly because of its simplicity.

A double-balanced mixer is a classic example of an analog phase detector.

On the other hand,examples of digital phase detectors are these:

1. Exclusive-OR phase detector
2. Edge-triggered phase detector
3. Monolithic phase detector (such as type 4044)

The following fig 2.11 shows Exclusive-OR phase detector:

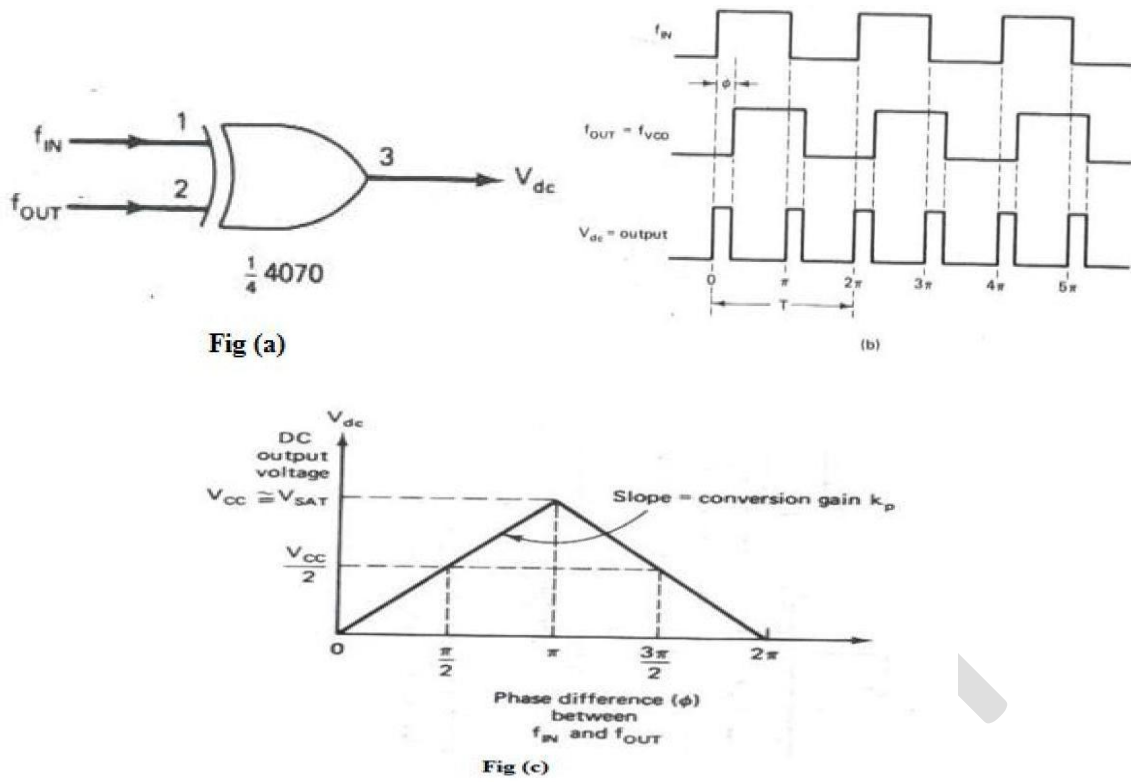


Fig 2.11 (a) Exclusive-OR phase detector: connection and logic diagram. (b) Input and output waveforms. (c) Average output voltage versus phase difference between fIN and fOUT curve.

(b) Low-pass filter.

The function of the low-pass filter is to remove the high-frequency components in the output of the phase detector and to remove high-frequency noise.

More important, the 1ow-pass filter controls the dynamic characteristics of the phase-locked loop. These characteristics include capture and lock ranges, bandwidth, and transient response. The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency fIN. An equivalent term for lock range is tracking range. On the other hand, the capture range is the frequency range in which the PLL acquires phase lock. Obviously, the capture range is always smaller than the lock range.

(c) Voltage-controlled oscillator:

A third section of the PLL is the voltage-controlled oscillator. The VCO generates an output frequency that is directly proportional to its input voltage. Typical example of VCO is Signetics NE/SE 566 VCO, which provides simultaneous square wave and triangular wave outputs as a function of input voltage. The block diagram of the VCO is shown in Fig 2.12. The frequency of oscillations is determined by three external R1 and capacitor C1 and the voltage VC applied to the control terminal 5.

The triangular wave is generated by alternatively charging the external capacitor C1 by

one current source and then linearly discharging it by another. The charging and discharging levels are determined by Schmitt trigger action. The schmitt trigger also provides square wave output. Both the wave forms are buffered so that the output impedance of each is 50 ohms.

In this arrangement the R1C1 combination determines the free running frequency and the control voltage VC at pin 5 is set by voltage divider formed with R2 and R3. The initial voltage VC at pin 5 must be in the range

$$\frac{3}{4}(+V) \leq V_C \leq +V$$

Where +V is the total supply voltage.The modulating signal is ac coupled with the capacitor C and must be <3 VPP. The frequency of the output wave forms is approximated by

$$f_O \cong \frac{2(+V - V_C)}{R_1 C_1 (+V)}$$

where R1should be in the range 2KΩ < R1< 20KΩ. For affixed VC and constant C1, the frequency fO can be varied over a 10:1 frequency range by the choice of R1 between 2KΩ < R1< 20KΩ.

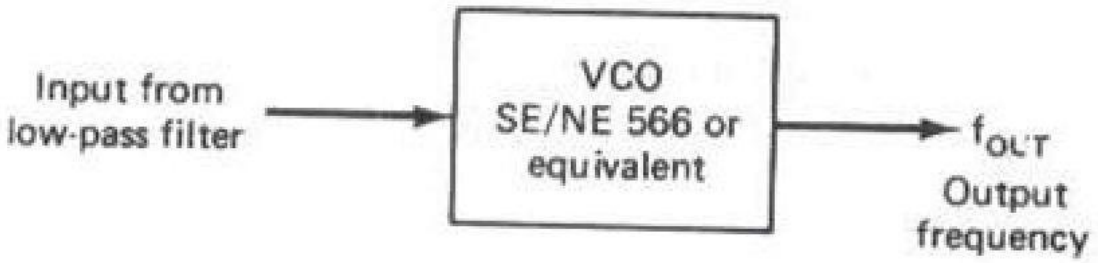


Fig 2.12: VCO Block Diagram

MONOLITHIC PHASE LOCK LOOPS IC 565:

Monolithic PLLs are introduced by signetics as SE/NE 560 series and by national semiconductors LM 560 series.

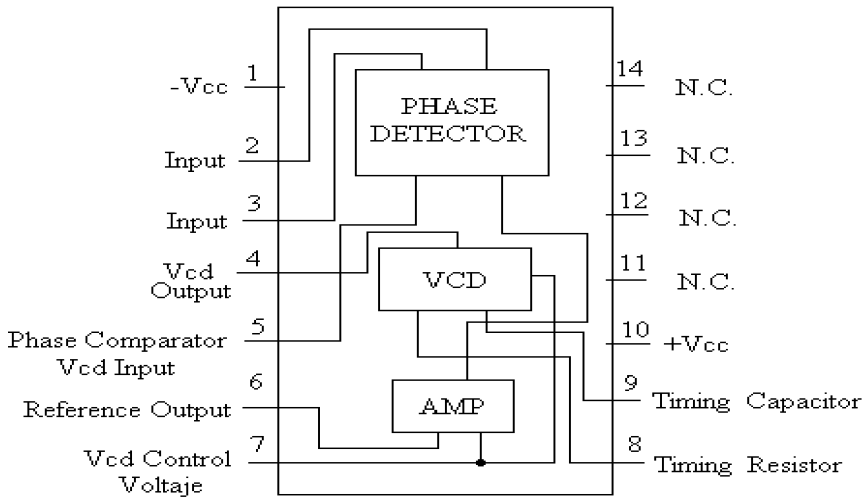


Fig 2.13 Pin configuration of IC 565

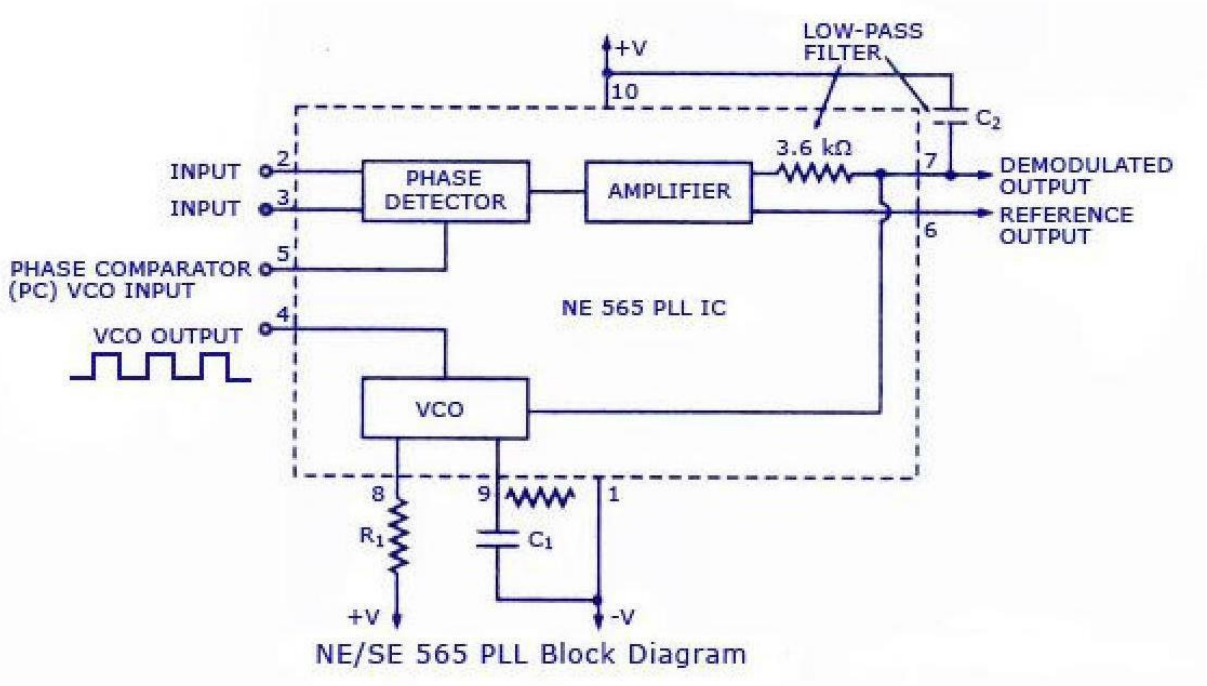


Fig 2.14 Block Diagram of IC 565

Fig 2.13 and 2.14 shows the pin diagram and block diagram of IC 565 PLL. It consists of phase detector, amplifier, low pass filter and VCO.As shown in the block diagram the phase locked feedback loop is not internally connected. Therefore, it is necessary to connect output of VCO to the phase comparator input, externally. In frequency multiplication applications a digital frequency divider is inserted into the loop i.e., between pin 4 and pin 5. The centre frequency of the PLL is determined by the free-running frequency of the VCO and it is given by

$$f_o = \frac{1.2}{4R_1C_1}$$

Where R1 and C1 are an external resistor and capacitor connected to pins 8 and 9, respectively. The values of R1 and C1 are adjusted such that the free running frequency will be at the centre of the input frequency range. The values of R1 are restricted from 2 kΩ to 20 kΩ,but a capacitor can have any value. A capacitor C2 connected between pin 7 and the positive supply forms a first order low pass filter with an internal resistance of 3.6 kΩ. The value of filter capacitor C2 should be larger enough to eliminate possible demodulated output voltage at pin 7 in order to stabilize the VCO frequency

The PLL can lock to and track an input signal over typically ±60% bandwidth w.r.t fo as the center frequency. The lock range fL and the capture range fC of the PLL are given by the following equations.

$$f_L = \pm\frac{8f_0}{V}$$

Where fo=free running frequency

V=(+V)-(-V)Volts

And

$$f_C = \pm\sqrt{\frac{f_L}{2\pi(3.6)10^3C_2}}$$

From above equation the lock range increases with an increase in input voltage but decrease with increase in supply voltage. The two inputs to the phase detector allows direct coupling of an input signal, provided that there is no dc voltage difference between the pins and the dc resistances seen from pins 2 and 3 are equal.

Wide Bandwidth Precision Analog Multiplier

Features

- Wide Bandwidth: 10mhz Typ
- □0.5% Max Four-Quadrant Accuracy
- Internal Wide-Bandwidth Op Amp
- Easy To Use
- Low Cost

Applications

- Precision Analog Signal Processing
- Modulation And Demodulation
- Voltage-Controlled Amplifiers
- Video Signal Processing
- Voltage-Controlled Filters And Oscillators

DESCRIPTION

The MPY634 is a wide bandwidth, high accuracy, four- quadrant analog multiplier. Its accurately laser-trimmed multiplier characteristics make it easy to use in a wide variety of applications with a minimum of external parts, often eliminating all external trimming. Its differential X, Y, and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter, and other functions while maintain- ing high accuracy.

The wide bandwidth of this new design allows signal processing at IF, RF, and video frequencies. The internal output amplifier of the MPY634 reduces design complexity compared to other high frequency mul- tipliers and balanced modulator circuits. It is capable of performing frequency mixing, balanced modula- tion, and demodulation with excellent carrier rejection.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user-selected scale factors from 0.1 to 10 using external feedback resistors.

UNIT-5

ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS

INTRODUCTION:

4-channel stereo multiplexed analog-to-digital converter WM8775SEDS made by Wolfson Microelectronics placed on an X-Fi Fatal1ty Pro sound card. An analog-to-digital converter (ADC, A/D, or A to D) is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

The conversion involves quantization of the input, so it necessarily introduces a small amount of error. Instead of doing a single conversion, an ADC often performs the conversions ("samples" the input) periodically. The result is a sequence of digital values that have been converted from a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal.

An ADC is defined by its bandwidth (the range of frequencies it can measure) and its signal to noise ratio (how accurately it can measure a signal relative to the noise it introduces). The actual bandwidth of an ADC is characterized primarily by its sampling rate, and to a lesser extent by how it handles errors such as aliasing. The dynamic range of an ADC is influenced by many factors, including the resolution (the number of output levels it can quantize a signal to), linearity and accuracy (how well the quantization levels match the true analog signal) and jitter (small timing errors that introduce additional noise). The dynamic range of an ADC is often summarized in terms of its effective number of bits (ENOB), the number of bits of each measure it returns that are on average not noise. An ideal ADC has an ENOB equal to its resolution. ADCs are chosen to match the bandwidth and required signal to noise ratio of the signal to be quantized. If an ADC operates at a sampling rate greater than twice the bandwidth of the signal, then perfect reconstruction is possible given an ideal ADC and neglecting quantization error. The presence of quantization error limits the dynamic range of even an ideal ADC, however, if the dynamic range of the ADC exceeds that of the input signal, its effects may be neglected resulting in an essentially perfect digital representation of the input signal.

An ADC may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. However, some non-electronic or only partially electronic devices, such as rotary encoders, can also be considered ADCs. The digital output may use different coding schemes. Typically the digital output will be a two's complement binary number that is proportional to the input, but there are other possibilities. An encoder, for example, might output a Gray code.

SPECIFICATIONS:

i) Resolution:

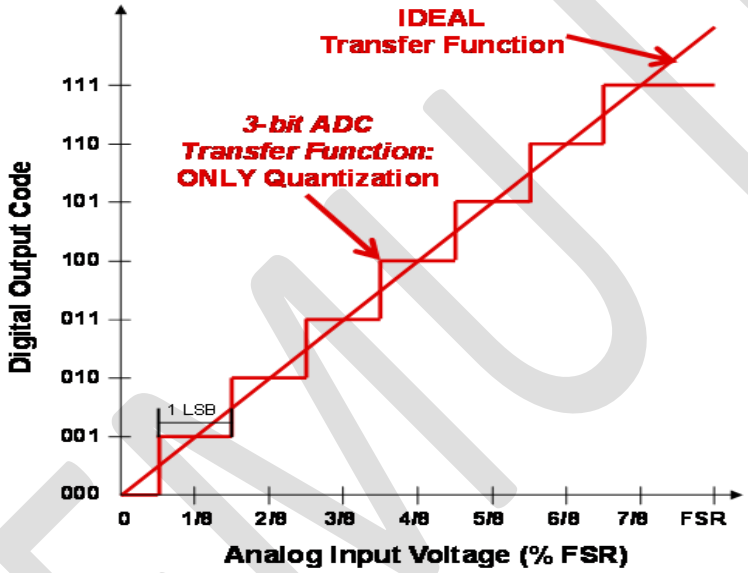


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Fig. 1. An 8-level ADC coding scheme.

The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. The resolution determines the magnitude of the quantization error and therefore determines the maximum possible average signal to noise ratio for an ideal ADC without the use of oversampling. The values are usually stored electronically in binary form, so the resolution is usually expressed in bits. In consequence, the number of discrete values available, or "levels", is assumed to be a power of two. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since $2^8 = 256$. The values can represent the ranges from 0 to 255 (i.e. unsigned integer) or from −128 to 127 (i.e. signed integer), depending on the application.

Resolution can also be defined electrically, and expressed in volts. The minimum change in voltage required to guarantee a change in the output code level is called the least significant bit (LSB) voltage. The resolution *Q* of the ADC is equal to the LSB voltage. The voltage resolution of an ADC is equal to its overall voltage measurement range divided by the number of discrete values:

$$Q = E_{FSR}/2^M$$

where *M* is the ADC's resolution in bits and E_{FSR} is the full scale voltage range (also called 'span'). E_{FSR} is given by

$$E_{FSR} = V_{RefHi} - V_{RefLow}$$

where V_{RefHi} and V_{RefLow} are the upper and lower extremes, respectively, of the voltages that can be coded.

Normally, the number of voltage intervals is given by

$$N = 2^M$$

where *M* is the ADC's resolution in bits.

That is, one voltage interval is assigned in between two consecutive code levels.

Example:

- Coding scheme as in figure 1 (assume input signal x(t) = Acos(t), A = 5V)
- Full scale measurement range = -5 to 5 volts
- ADC resolution is 8 bits: $2^8 = 256$ quantization levels (codes)
- ADC voltage resolution, $Q = (10\ V - 0\ V) / 256 = 10\ V / 256 \approx 0.039\ V \approx 39\ mV$.

In practice, the useful resolution of a converter is limited by the best signal-to-noise ratio (SNR) that can be achieved for a digitized signal. An ADC can resolve a signal to only a certain number of bits of resolution, called the effective number of bits (ENOB). One effective bit of resolution changes the signal-to-noise ratio of the digitized signal by 6 dB, if the resolution is limited by the ADC. If a preamplifier has been used prior to A/D conversion, the noise introduced by the amplifier can be an important contributing factor towards the overall SNR.

ii) Quantization error:

Quantization error is the noise introduced by quantization in an ideal ADC. It is a rounding error between the analog input voltage to the ADC and the output digitized value. The noise is non-linear and signal-dependent.

In an ideal analog-to-digital converter, where the quantization error is uniformly distributed between −1/2 LSB and +1/2 LSB, and the signal has a uniform distribution covering all quantization levels, the Signal-to-quantization-noise ratio (SQNR) can be calculated from

$$\mathrm{SQNR} = 20\log_{10}(2^Q) \approx 6.02 \cdot Q \text{ dB}$$

Where Q is the number of quantization bits. For example, a 16-bit ADC has a maximum signal-to-noise ratio of 6.02 × 16 = 96.3 dB, and therefore the quantization error is 96.3 dB below the maximum level. Quantization error is distributed from DC to the Nyquist frequency, consequently if part of the ADC's bandwidth is not used (as in oversampling), some of the quantization error will fall out of band, effectively improving the SQNR. In an oversampled system, noise shaping can be used to further increase SQNR by forcing more quantization error out of the band.

iii) Sampling rate

The analog signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal. The rate of new values is called the *sampling rate* or sampling frequency of the converter.

A continuously varying band limited signal can be sampled (that is, the signal values at intervals of time T, the sampling time, are measured and stored) and then the original signal can be *exactly* reproduced from the discrete-time values by an interpolation formula. The accuracy is limited by quantization error. However, this faithful reproduction is only possible if the sampling rate is higher than twice the highest frequency of the signal. This is essentially what is embodied in the Shannon-Nyquist sampling theorem.

Since a practical ADC cannot make an instantaneous conversion, the input value must necessarily be held constant during the time that the converter performs a conversion (called the *conversion time*). An input circuit called a sample and hold performs this task—in most cases by using a capacitor to store the analog voltage at the input, and using an electronic switch or gate to disconnect the capacitor from the input. Many ADC integrated circuits include the sample and hold subsystem internally.

iv) Aliasing

An ADC works by sampling the value of the input at discrete intervals in time. Provided that the input is sampled above the Nyquist rate, defined as twice the highest frequency of interest, then all frequencies in the signal can be reconstructed. If frequencies above half the Nyquist rate

are sampled, they are incorrectly detected as lower frequencies, a process referred to as aliasing. Aliasing occurs because instantaneously sampling a function at two or fewer times per cycle results in missed cycles, and therefore the appearance of an incorrectly lower frequency. For example, a 2 kHz sine wave being sampled at 1.5 kHz would be reconstructed as a 500 Hz sine wave.

To avoid aliasing, the input to an ADC must be low-pass filtered to remove frequencies above half the sampling rate. This filter is called an anti-aliasing filter, and is essential for a practical ADC system that is applied to analog signals with higher frequency content. In applications where protection against aliasing is essential, oversampling may be used to greatly reduce or even eliminate it.

Although aliasing in most systems is unwanted, it should also be noted that it can be exploited to provide simultaneous down-mixing of a band-limited high frequency signal (see under sampling and frequency mixer). The alias is effectively the lower heterodyne of the signal frequency and sampling frequency.

Oversampling

Signals are often sampled at the minimum rate required, for economy, with the result that the quantization noise introduced is white noise spread over the whole pass band of the converter. If a signal is sampled at a rate much higher than the Nyquist rate and then digitally filtered to limit it to the signal bandwidth there are the following advantages:

- Digital filters can have better properties (sharper rolloff, phase) than analogue filters, so a sharper anti-aliasing filter can be realised and then the signal can be downsampled giving a better result
- A 20-bit ADC can be made to act as a 24-bit ADC with 256× oversampling
- The signal-to-noise ratio due to quantization noise will be higher than if the whole available band had been used. With this technique, it is possible to obtain an effective resolution larger than that provided by the converter alone
- The improvement in SNR is 3 dB (equivalent to 0.5 bits) per octave of oversampling which is not sufficient for many applications. Therefore, oversampling is usually coupled with noise shaping (see sigma-delta modulators). With noise shaping, the improvement is 6L+3 dB per octave where L is the order of loop filter used for noise shaping. e.g. – a 2nd order loop filter will provide an improvement of 15 dB/octave.

Oversampling is typically used in audio frequency ADCs where the required sampling rate (typically 44.1 or 48 kHz) is very low compared to the clock speed of typical transistor circuits (>1 MHz). In this case, by using the extra bandwidth to distribute quantization error onto out of band frequencies, the accuracy of the ADC can be greatly increased at no cost. Furthermore, as any aliased signals are also typically out of band, aliasing can often be completely eliminated using very low cost filters.

v) Monotonicity

Differential nonlinearity (acronym DNL) is a term describing the deviation between two analog values corresponding to adjacent input digital values. It is an important specification for measuring error in a digital-to-analog converter (DAC); the accuracy of a DAC is mainly determined by this specification. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one Least Significant Bit (LSB) apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. For example, a DAC with a 1.5 LSB output change for a 1 LSB digital code change exhibits 1⁄2 LSB differential non-linearity. Differential non-linearity may be expressed in fractional bits or as a percentage of full scale. A differential non-linearity greater than 1 LSB may lead to a non-monotonic transfer function in a DAC.[1] It is also known as a missing code.

vi) Linearity

Differential linearity refers to a constant relation between the change in the output and input. For transducers if a change in the input produces a uniform step change in the output the transducer possess differential linearity. Differential linearity is desirable and is inherent to a system such as a single-slope analog-to-digital converter used in nuclear instrumentation.

vii) Settling Time

The settling time of an amplifier or other output device is the time elapsed from the application of an ideal instantaneous step input to the time at which the amplifier output has entered and remained within a specified error band, usually symmetrical about the final value. Settling time includes a very brief propagation delay, plus the time required for the output to slew to the vicinity of the final value, recover from the overload condition associated with slew, and finally settle to within the specified error.

DIGITAL-TO-ANALOG CONVERTER:

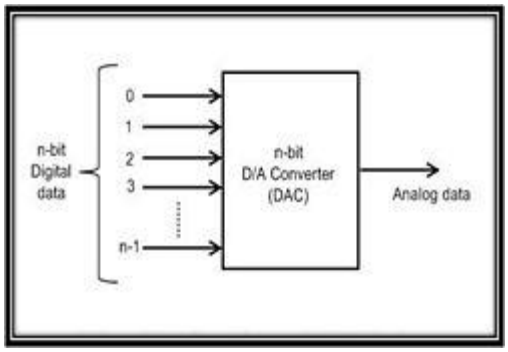


Fig.2.A simplified functional diagram of an 8-bit DAC

In electronics, a digital-to-analog converter (DAC, D/A, D2A or D-to-A) is a function that converts digital data (usually binary) into an analog signal (current, voltage, or electric charge). An analog-to-digital converter (ADC) performs the reverse function. Unlike analog signals, digital data can be transmitted, manipulated, and stored without degradation, albeit with more complex equipment. But a DAC is needed to convert the digital signal to analog to drive an earphone or loudspeaker amplifier in order to produce sound (analog air pressure waves).

DACs and their inverse, ADCs, are part of an enabling technology that has contributed greatly to the digital revolution. To illustrate, consider a typical long-distance telephone call. The caller's voice is converted into an analog electrical signal by a microphone, then the analog signal is converted to a digital stream by an ADC. The digital stream is then divided into packets where it may be mixed with other digital data, not necessarily audio. The digital packets are then sent to the destination, but each packet may take a completely different route and may not even arrive at the destination in the correct time order. The digital voice data is then extracted from the packets and assembled into a digital data stream. A DAC converts this into an analog electrical signal, which drives an audio amplifier, which in turn drives a loudspeaker, which finally produces sound.

There are several DAC architectures; the suitability of a DAC for a particular application is determined by six main parameters: physical size, power consumption, resolution, speed, accuracy, cost. Due to the complexity and the need for precisely matched components, all but the most specialist DACs are implemented as integrated circuits (ICs). Digital-to-analog conversion can degrade a signal, so a DAC should be specified that has insignificant errors in terms of the application.

DACs are commonly used in music players to convert digital data streams into analog audio signals. They are also used in televisions and mobile phones to convert digital video data

into analog video signals which connect to the screen drivers to display monochrome or color images. These two applications use DACs at opposite ends of the speed/resolution trade-off. The audio DAC is a low speed high resolution type while the video DAC is a high speed low to medium resolution type. Discrete DACs would typically be extremely high speed low resolution power hungry types, as used in military radar systems. Very high speed test equipment, especially sampling oscilloscopes, may also use discrete DACs.

APPLICATIONS

Most modern audio signals are stored in digital form (for example MP3s and CDs) and in order to be heard through speakers they must be converted into an analog signal. DACs are therefore found in CD players, digital music players, and PC sound cards. Specialist standalone DACs can also be found in high-end hi-fi systems. These normally take the digital output of a compatible CD player or dedicated transport (which is basically a CD player with no internal DAC) and convert the signal into an analog line-level output that can then be fed into an amplifier to drive speakers.Similar digital-to-analog converters can be found in digital speakers such as USB speakers, and in sound cards.

In VoIP (Voice over IP) applications, the source must first be digitized for transmission, so it undergoes conversion via an analog-to-digital converter, and is then reconstructed into analog using a DAC on the receiving party's end.

Fig.3. Top-loading CD player and external digital-to-analog converter.

Video sampling tends to work on a completely different scale altogether thanks to the highly nonlinear response both of cathode ray tubes (for which the vast majority of digital video foundation work was targeted) and the human eye, using a "gamma curve" to provide an appearance of evenly distributed brightness steps across the display's full dynamic range - hence the need to use RAMDACs in computer video applications with deep enough colour resolution to

make engineering a hardcoded value into the DAC for each output level of each channel impractical (e.g. an Atari ST or Sega Genesis would require 24 such values; a 24-bit video card would need 768...). Given this inherent distortion, it is not unusual for a television or video projector to truthfully claim a linear contrast ratio (difference between darkest and brightest output levels) of 1000:1 or greater, equivalent to 10 bits of audio precision even though it may only accept signals with 8-bit precision and use an LCD panel that only represents 6 or 7 bits per channel.

Video signals from a digital source, such as a computer, must be converted to analog form if they are to be displayed on an analog monitor. As of 2007, analog inputs were more commonly used than digital, but this changed as flat panel displays with DVI and/or HDMI connections became more widespread.[citation needed] A video DAC is, however, incorporated in any digital video player with analog outputs. The DAC is usually integrated with some memory (RAM), which contains conversion tables for gamma correction, contrast and brightness, to make a device called a RAMDAC.

A device that is distantly related to the DAC is the digitally controlled potentiometer, used to control an analog signal digitally.

DAC TYPES

The most common types of electronic DACs are:

i) Weighted Resistor DAC

The binary-weighted DAC, which contains individual electrical components for each bit of the DAC connected to a summing point. These precise voltages or currents sum to the correct output value. This is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual voltage or current. Such high-precision components are expensive, so this type of converter is usually limited to 8-bit resolution or less.

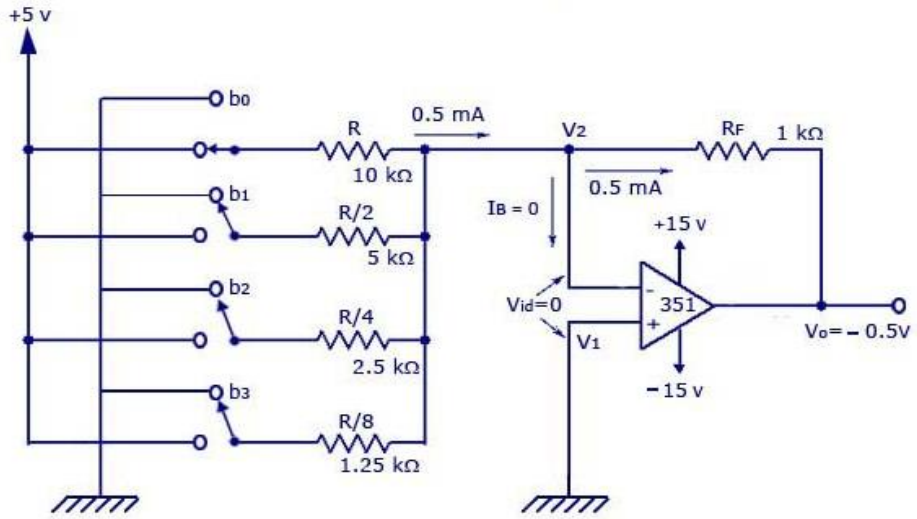


Fig.4. Weighted Resistor DAC

We know that, a 4-bit converter will have $2^4 = 16$ combinations of output. Thus, a corresponding 16 outputs of analog will also be present for the binary inputs.

Four switches from b0 to b3 are available to simulate the binary inputs: in practice, a 4-bit binary counter such as a 7493 can also be used.

Working

The circuit is basically working as a current to voltage converter.

- b0 is closed

It will be connected directly to the +5V.

Thus, voltage across R = 5V

Current through R = 5V/10kohm = 0.5mA

Current through feedback resistor, Rf = 0.5mA (Since, Input bias current, I_B is negligible)

Thus, output voltage = -(1kohm)*(0.5mA) = -0.5V

- b1 is closed, b0 is open

R/2 will be connected to the positive supply of the +5V.

Current through R will become twice the value of current (1mA) to flow through Rf.

Thus, output voltage also doubles.

- b0 and b1 are closed

Current through Rf = 1.5mA

Output voltage = -(1kohm)*(1.5mA) = -1.5V

Thus, according to the position (ON/OFF) of the switches (bo-b3), the corresponding "binary-weighted" currents will be obtained in the input resistor. The current through Rf will be the sum of

these currents. This overall current is then converted to its proportional output voltage. Naturally, the output will be maximum if the switches (b0-b3) are closed

V0 = -Rf *([b0/R][b1/(R/2)][b2/(R/4)][b3/(R/8)]) – where each of the inputs b3, b2, b1, and b0 may either be HIGH (+5V) or LOW (0V).

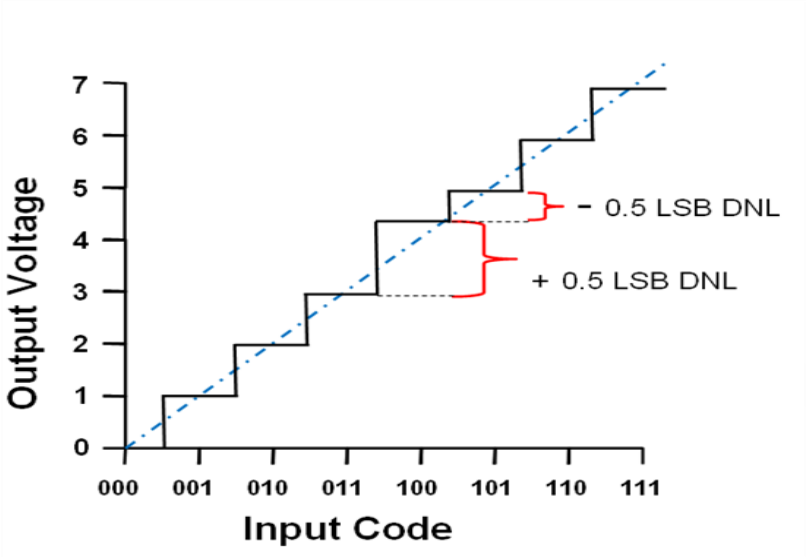


Fig.5. Transfer characteristics of 3 bit DAC

ii).R-2R Ladder DAC

The R-2R ladder DAC which is a binary-weighted DAC that uses a repeating cascaded structure of resistor values R and 2R. This improves the precision due to the relative ease of producing equal valued-matched resistors (or current sources). However, wide converters perform slowly due to increasingly large RC-constants for each added R-2R link.

- V_{ref} is nothing but the input binary value reference voltage, that is for binary 1, V_{ref}=5V and for binary 0, V_{ref}=0V.
- For 0001 only $D_0=V_{ref}$, all other inputs are at 0V and can be treated as ground. So finally $V_{ref}/16$ volt is appearing as the input to op amp. This value gets multiplied by the gain of op amp circuit – (R_f/R_i).
- If we proceed in this manner (Thevenin equivalent reduction), we will get

$$V_{out} = -\frac{R_f}{R_i} V_{ref}\left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2}\right]$$

- Note that you can build a DAC with any number of bits you want, by simply enlarging the resistor network, by adding more R-2R resistor branches.

- In this circuit the 7493 IC simply provides digital inputs to DAC. It is a counter IC and not an integral part of the DAC circuit. You can apply any combinations of binary inputs to $D_3D_2D_1D_0$

  A D/A converter with R and 2R resistors is shown in the figure below.

  As in the binary-weighted resistors method, the binary inputs are applied by the switches (b0-b3), and the output is proportional to the binary inputs. Binary inputs can be either in the HIGH (+5V) or LOW (0V) state. Let b3 be the most significant bit and thus is connected to the +5V and all the other switches are connected to the ground.

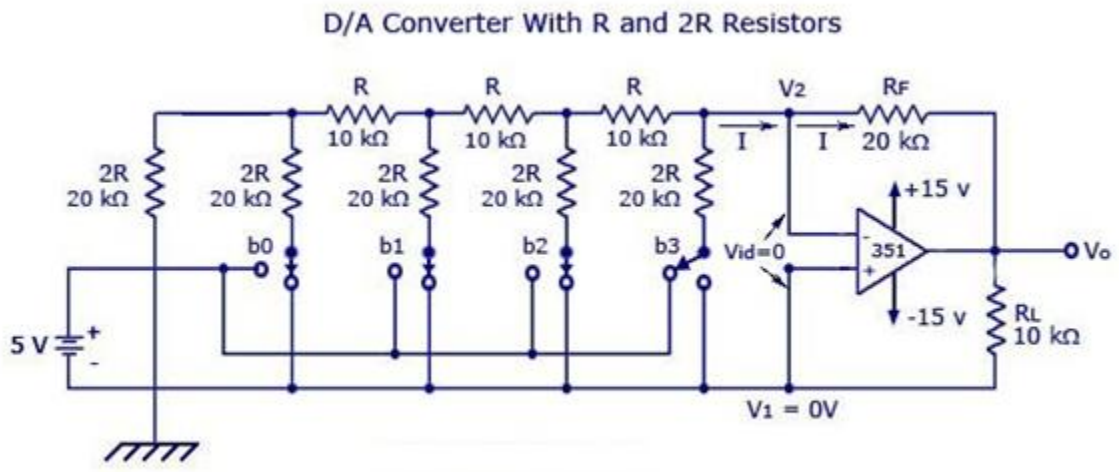


Fig.6. *R-2R Ladder DAC*

Thus, according to Thevenin's equivalent resistance, R_{TH},

R_{TH} = [{[(2RII2R + R)} II2R] + R}II2R] + R = 2R = 20kOhms.

Current through 2R connected to +5V = 5V/20KΩ = 0.25 mA

The current will be the same as that in Rf.

V_o = -(20KΩ)*(0.25mA) = -5V.

Output voltage equation is given below:

$$V_O = -V_{CC}R_f\left[\left(\frac{b_3}{2R}\right) + \left(\frac{b_2}{4R}\right) + \left(\frac{b_1}{8R}\right) + \left(\frac{b_0}{16R}\right)\right]$$

ii) Inverted R-2R Ladder DAC

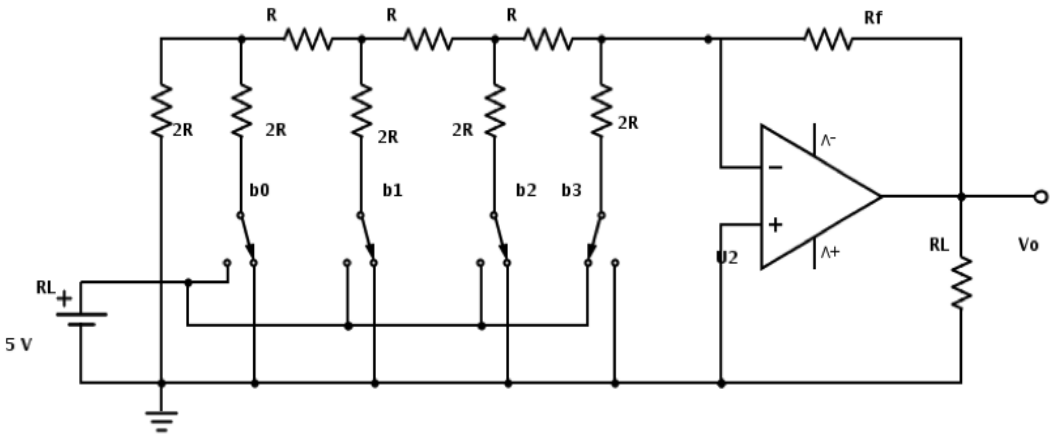


Fig.7. *Inverted R-2R Ladder DAC*

- The pulse-width modulator, the simplest DAC type. A stable current or voltage is switched into a low-pass analog filter with a duration determined by the digital input code. This technique is often used for electric motor speed control, but has many other applications as well.
- Oversampling DACs or interpolating DACs such as the delta-sigma DAC, use a pulse density conversion technique. The oversampling technique allows for the use of a lower resolution DAC internally. A simple 1-bit DAC is often chosen because the oversampled result is inherently linear. The DAC is driven with a pulse-density modulated signal, created with the use of a low-pass filter, step nonlinearity (the actual 1-bit DAC), and negative feedback loop, in a technique called delta-sigma modulation. This results in an effective high-pass filter acting on the quantization (signal processing) noise, thus steering this noise out of the low frequencies of interest into the megahertz frequencies of little interest, which is called noise shaping. The quantization noise at these high frequencies is removed or greatly attenuated by use of an analog low-pass filter at the output (sometimes a simple RC low-pass circuit is sufficient). Most very high resolution DACs (greater than 16 bits) are of this type due to its high linearity and low cost. Higher oversampling rates can relax the specifications of the output low-pass filter and enable further suppression of quantization noise. Speeds of greater than 100 thousand samples per second (for example, 192 kHz) and resolutions of 24 bits are attainable with delta-sigma DACs. A short comparison with pulse-width modulation shows that a 1-bit DAC with a simple first-order integrator would have to run at 3 THz (which is physically unrealizable) to achieve 24 meaningful bits of resolution, requiring a higher-order low-pass filter in the noise-shaping loop. A single integrator is a low-pass filter with a frequency response inversely proportional to frequency and using one such integrator in the noise-shaping loop is a first order delta-sigma modulator. Multiple

higher order topologies (such as MASH) are used to achieve higher degrees of noise-shaping with a stable topology.

HIGH SPEED SAMPLE AND HOLD CIRCUITS

Introduction:

Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits. The simplest S/H circuit in MOS technology is shown in Figure 1, where Vin is the input signal, M1 is an MOS transistor operating as the sampling switch, Ch is the hold capacitor, ck is the clock signal, and Vout is the resulting sample-and-hold output signal.

As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward.

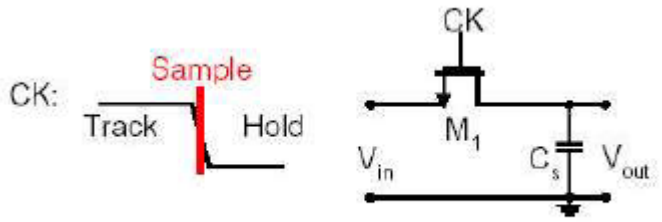


Fig.8. *Simplest sample and hold circuit in MOS technology*

Whenever As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever ck is high, the MOS switch is on, which in turn allows Vout to track Vin. On the other hand, when ck is low, the MOS switch is off. During this time, Ch will keep Vout equal to the value of Vin at the instance when ck goes low.

Unfortunately, in reality, the performance of this S/H circuit is not as ideal as described above. The two major types of errors occur. They are charge injection and clock feed through, that are associated with this S/H implementation. Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through. Alternative CMOS Sample-and-Hold Circuits:

This section covers three alternative CMOS S/H circuits that are developed with the Intention to minimize charge injection and/or clock feed through. Series Sampling:
The S/H circuit of Figure 1 is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled. On the other hand, the S/H circuit shown in Figure 2 is referred to as series sampling because the hold capacitor is in series with the signal.

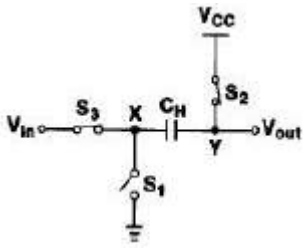


Fig.9. *Series sampling*

When the circuit is in sample mode, both switches S2 and S3 are on, while S1 is off. Then,S2 is turned off first, which means Vout is equal to VCC (or VDD for most circuits) and the voltage drop across Ch will be VCC – Vin. Subsequently, S3 is turned off and S1 is turned on simultaneously. By grounding node X, Vout is now equal to VCC – Vin, and the drop from VCC to VCC – Vin is equal to the instantaneous value of the input.

As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage. Since the hold capacitor is in series with the signal, series sampling can isolate the common mode levels of the input and the output. This is one advantage of series sampling over parallel sampling. In addition, unlike parallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behavior because S2 is turned off before S3.

Thus, the fact that the gate-to-source voltage, V_{GS}, of S2 is constant means that charge injection coming from S2 is also constant (as opposed to being signal-dependent), which means this error can easily eliminated through differential operation.

On the other hand, series sampling suffers from the nonlinearity of the parasitic capacitance at node Y. This parasitic capacitance introduces distortion to the sample-and hold value, thus mandating that Ch be much larger than the parasitic capacitance. On top of this disadvantage, the settling time of the S/H circuit during hold mode is longer for series sampling than for parallel sampling. The reason for this is because the value of Vout in series sampling is being reset to VCC (or VDD) for every sample, but this is not the case for parallel sampling.

Switched Op-Amp Based Sample-and-Hold Circuit:

This S/H technique takes advantage of the fact that when a MOS transistor is in the saturation region, the channel is pinched off and disconnected from the drain. Therefore, if the hold capacitor is connected to the drain of the MOS transistor, charge injection will only go to the source junction, leaving the drain unaffected. Based on this concept, a switched op amp

(SOP) based S/H circuit, as shown in Figure 3.

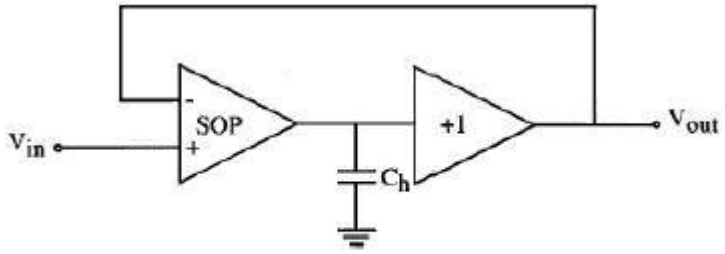
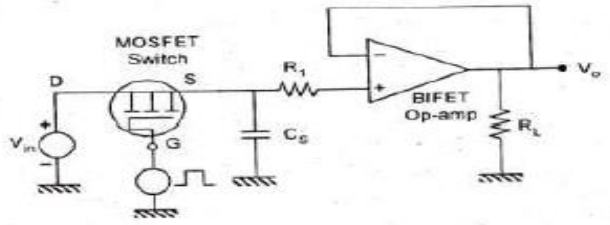


Fig.10. *Switched op-amp based sample and hold circuit*

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP. In addition, the SOP is shut off and its output is held at high impedance, allowing the charge on Ch to be preserved throughout the hold mode. On the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on Ch to the output of the S/H circuit. With the increasing demand for high-resolution and high-speed in date acquisition systems, the performance of the S/H circuits is becoming more and more important.

This is especially true in ADCs since the performance of S/H circuits greatly affects the speed and accuracy of ADCs. The fastest S/H circuits operate in open loop, but when such circuits are implemented in CMOS technology, their accuracy is low. S/H circuits that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits. As a result, better and faster S/H circuits must be developed.At the same time, the employment of low-voltage in VLSI technology requires that theanalog circuits be low-voltage as well. As a result of this, new researches in analog circuits are

now shifted from voltage-mode to current-mode. The advantages of current mode circuits include low-voltage, low-power, and high-speed. Therefore, future researches of S/H circuit should also shift toward current-mode S/H techniques.



The above figure shows a sample and hold circuit with MOSFET as Switch acting as a sampling device and also consists of a holding capacitor Cs to store the sample values until the next sample comes in. This is a high speed circuit as it is apparent that CMOS switch has a very negligible propagation delay.

Sample-and-hold (S/H) is an important analog building block that has many applications. The simplest S/H circuit can be constructed using only one MOS transistor and one hold capacitor.

However, due to the limitations of the MOS transistor switches, errors due to charge injection and clock feed through restrict the performance of S/H circuits. As a result, different S/H techniques and architectures are developed with the intention to reduce or eliminate these errors. Three of these alternative S/H circuits: series sampling, SOP based S/H circuit, and bottom plate S/H circuit with bootstrapped switch, more new S/H techniques and architectures need to be proposed in order to meet the increasing demand for high-speed, low-power, and low voltage for data acquisition systems.

DIGITAL-TO-ANALOG CONVERTER:

DACs are very important to system performance. The most important characteristics of these devices are:

Resolution

The number of possible output levels the DAC is designed to reproduce. This is usually stated as the number of bits it uses, which is the base two logarithm of the number of levels. For instance a 1 bit DAC is designed to reproduce 2 (2^1) levels while an 8 bit DAC is designed for 256 (2^8) levels. Resolution is related to the effective number of bits which is a measurement of the actual resolution attained by the DAC. Resolution determines color depth in video applications and audio bit depth in audio applications.

Maximum sampling rate

A measurement of the maximum speed at which the DACs circuitry can operate and still produce the correct output. As stated in the Nyquist–Shannon sampling theorem defines a relationship between the sampling frequency and bandwidth of the sampled signal.

Monotonicity

The ability of a DAC's analog output to move only in the direction that the digital input moves (i.e., if the input increases, the output doesn't dip before asserting the correct output.) This characteristic is very important for DACs used as a low frequency signal source or as a digitally programmable trim element.

Total harmonic distortion ***and noise (THD+N)***

A measurement of the distortion and noise introduced to the signal by the DAC. It is expressed as a percentage of the total power of unwanted harmonic distortion and noise that accompany the desired signal. This is a very important DAC characteristic for dynamic and small signal DAC applications.

Dynamic range

A measurement of the difference between the largest and smallest signals the DAC can reproduce expressed in decibels. This is usually related to resolution and noise floor.

Other measurements, such as phase distortion and jitter, can also be very important for some applications, some of which (e.g. wireless data transmission, composite video) may even *rely* on accurate production of phase-adjusted signals.

Linear PCM audio sampling usually works on the basis of each bit of resolution being equivalent to 6 decibels of amplitude (a 2x increase in volume or precision).

Non-linear PCM encodings (A-law / μ-law, ADPCM, NICAM) attempt to improve their effective dynamic ranges by a variety of methods - logarithmic step sizes between the output signal strengths represented by each data bit (trading greater quantization distortion of loud signals for better performance of quiet signals)

DAC figures of merit

- Static performance:
- Differential nonlinearity (DNL) shows how much two adjacent code analog values deviate from the ideal 1 LSB step.[2]

- Integral nonlinearity (INL) shows how much the DAC transfer characteristic deviates from an ideal one. That is, the ideal characteristic is usually a straight line; INL shows how much the actual voltage at a given code value differs from that line, in LSBs (1 LSB steps).
- Gain
- Offset
- Noise is ultimately limited by the thermal noise generated by passive components such as resistors. For audio applications and in room temperatures, such noise is usually a little less than 1 μV (microvolt) of white noise. This limits performance to less than 20~21 bits even in 24-bit DACs.
- Frequency domain performance
- Spurious-free dynamic range (SFDR) indicates in dB the ratio between the powers of the converted main signal and the greatest undesired spur.
- Signal-to-noise and distortion ratio (SNDR) indicates in dB the ratio between the powers of the converted main signal and the sum of the noise and the generated harmonic spurs.
- i-th harmonic distortion (HDI) indicates the power of the i-th harmonic of the converted main signal
- Total harmonic distortion (THD) is the sum of the powers of all HDI

- If the maximum DNL error is less than 1 LSB, then the D/A converter is guaranteed to be monotonic. However, many monotonic converters may have a maximum DNL greater than 1 LSB.
- Time domain performance:
- Glitch impulse area (glitch energy)
- Response uncertainty
- Time nonlinearity (TNL)

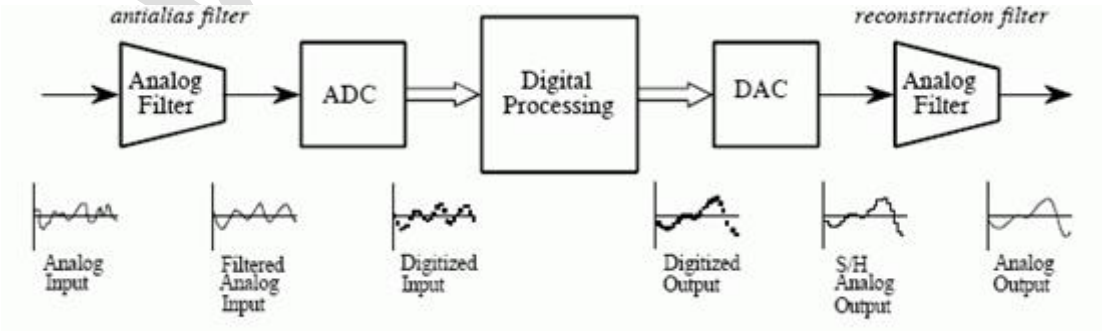


Fig.11. *Complete analog to digital and digital to analog converter*

Analog-to-Digital Conversion

This is a sample of the large number of analog-to-digital conversion methods. The basic principle of operation is to use the comparator principle to determine whether or not to turn on a particular bit of the binary number output. It is typical for an ADC to use a digital-to-analog converter (DAC) to determine one of the inputs to the comparator.

Digital Ramp ADC

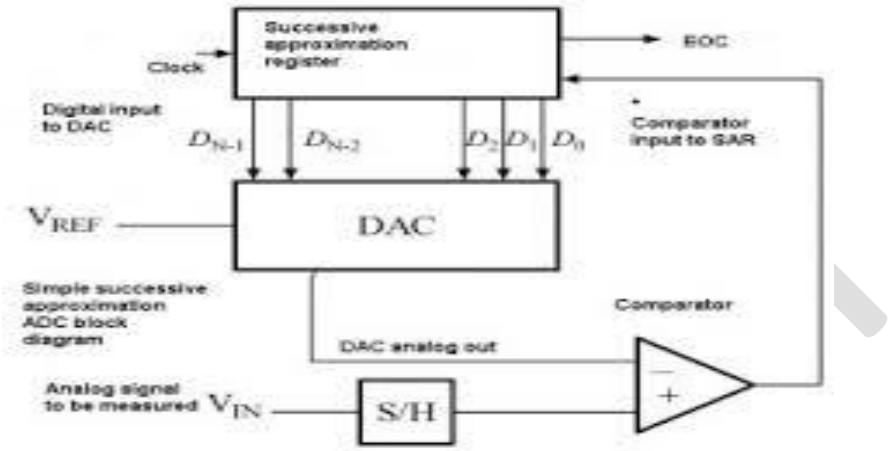


Fig.12. Digital Ramp ADC

Conversion from analog to digital form inherently involves comparator action where the value of the analog voltage at some point in time is compared with some standard. A common way to do that is to apply the analog voltage to one terminal of a comparator and trigger a binary counter which drives a DAC. The output of the DAC is applied to the other terminal of the comparator. Since the output of the DAC is increasing with the counter, it will trigger the comparator at some point when its voltage exceeds the analog input. The transition of the comparator stops the binary counter, which at that point holds the digital value corresponding to the analog voltage.

Successive Approximation ADC

A successive approximation A/D converter consists of a comparator, a successive approximation register (SAR), output latches, and a D/A converter. The circuit diagram is shown below.

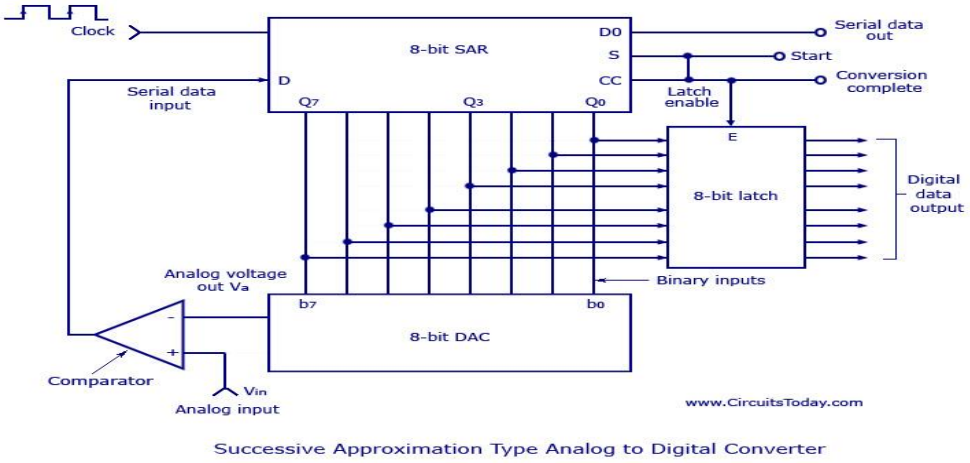


Fig.13. Successive Approximation Type Analog to Digital Converter

The main part of the circuit is the 8-bit SAR, whose output is given to an 8-bit D/A converter. The analog output V_a of the D/A converter is then compared to an analog signal V_{in} by the comparator. The output of the comparator is a serial data input to the SAR. Till the digital output (8 bits) of the SAR is equivalent to the analog input V_{in}, the SAR adjusts itself. The 8-bit latch at the end of conversation holds onto the resultant digital data output.

Working

At the start of a conversion cycle, the SAR is reset by making the start signal (S) high. The MSB of the SAR (Q7) is set as soon as the first transition from LOW to HIGH is introduced. The output is given to the D/A converter which produces an analog equivalent of the MSB and is compared with the analog input V_{in}.

If comparator output is LOW, D/A output will be greater than V_{in} and the MSB will be cleared by the SAR. If comparator output is HIGH, D/A output will be less than V_{in} and the MSB will be set to the next position (Q7 to Q6) by the SAR.

According to the comparator output, the SAR will either keep or reset the Q6 bit. This process goes on until all the bits are tried. After Q0 is tried, the SAR makes the conversion complete (CC) signal HIGH to show that the parallel output lines contain valid data. The CC signal in turn enables the latch, and digital data appear at the output of the latch. As the SAR determines each bit, digital data is also available serially. As shown in the figure above, the CC signal is connected to the start conversion input in order to convert the cycle continuously.

The biggest advantage of such a circuit is its high speed. It may be more complex than an A/D converter, but it offers better resolution.

The successive approximation ADC is much faster than the digital ramp ADC because it use converge on the value closest to the input voltage. A comparator and a DAC are used in the process.

Advantages:

1 Conversion time is very small.

2 Conversion time is constant and independent of the amplitude of the analog input signal VA.

Disadvantages:

1 Circuit is complex.

2 The conversion time is more compared to flash type ADC.

Flash ADC

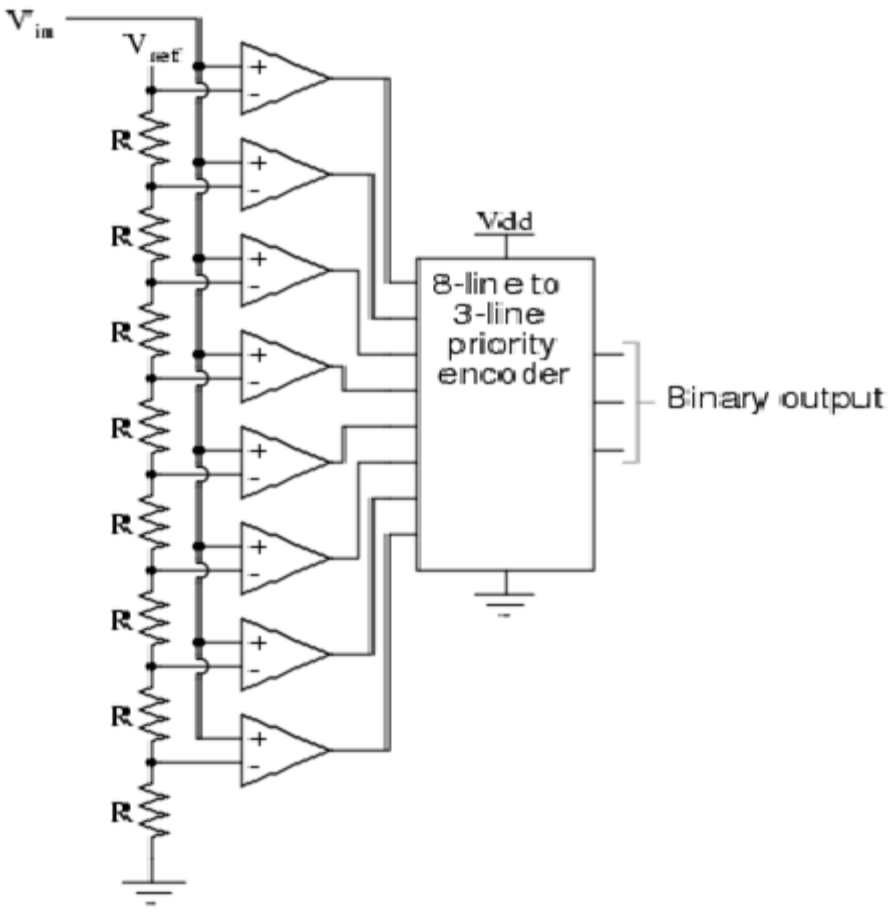


Fig14. *Flash comparator type ADC*

Illustrated is a 3-bit flash ADC with resolution 1 volt (after Tocci). The resistor net and comparators provide an input to the combinational logic circuit, so the conversion time is just the propagation delay through the network - it is not limited by the clock rate or some convergence sequence. It is the fastest type of ADC available, but requires a comparator for each value of output (63 for 6-bit, 255 for 8-bit, etc.) Such ADCs are available in IC form up to 8-bit and 10-bit flash ADCs (1023 comparators) are planned. The encoder logic executes a truth table to convert the ladder of inputs to the binary number output.

COUNTER TYPE ADC

The counter type ADC is constructed using a binary counter, DAC and a comparator. The output voltage of a DAC is VD which is equivalent to corresponding digital input to DAC. The following figure shows the n-bit counter type ADC.

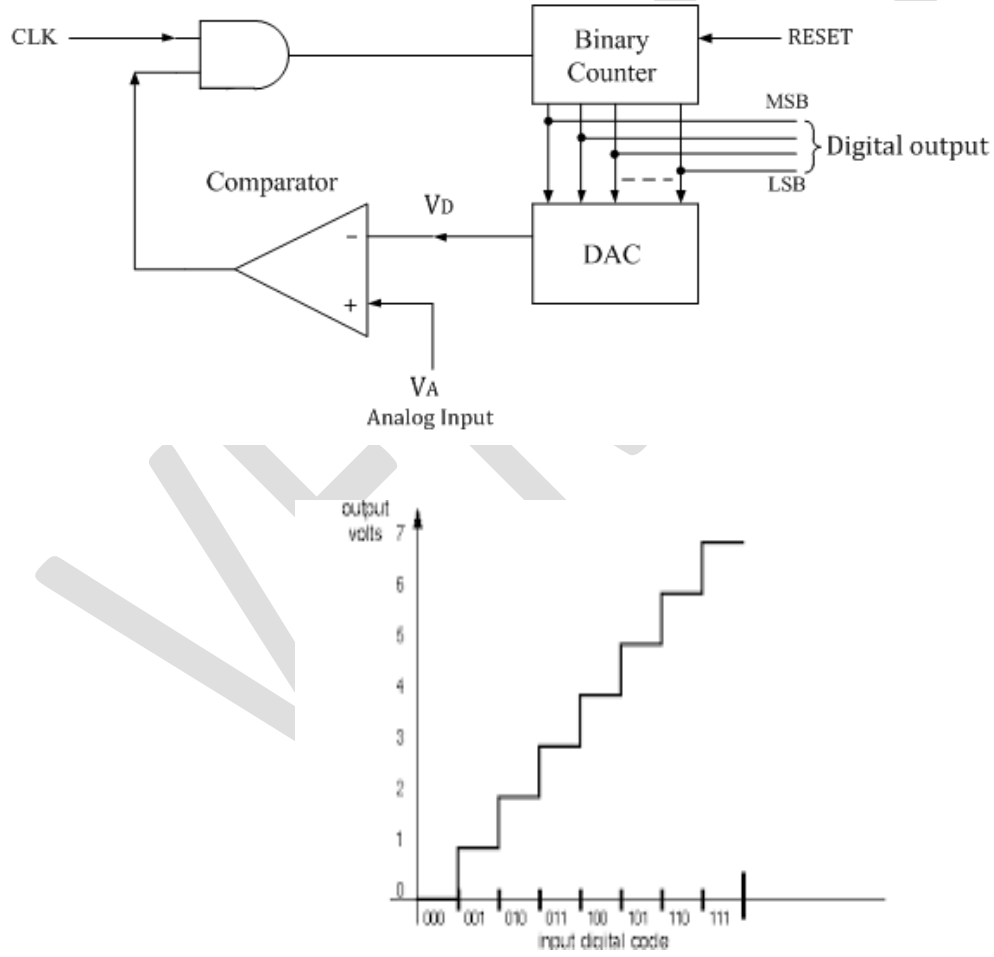


Fig .15. Counter type ADC

Operation:

The n-bit binary counter is initially set to 0 by using reset command. Therefore the digital output is zero and the equivalent voltage VD is also 0V. When the reset command is removed, the clock pulses are allowed to go through AND gate and are counted by the binary counter. The D to A converter (DAC) converts the digital output to an analog voltage and applied as the inverting input to the comparator. The output of the comparator enables the AND gate to pass the clock. The number of clock pulses increases with time and the analog input voltage VD is a rising staircase waveform as shown in figure below.

Integrating type ADC

Integrating analog-to-digital converters (ADCs) provide high resolution and can provide good line frequency and noise rejection. Having started with the ubiquitous 7106, these converters have been around for quite some time. The integrating architecture provides a novel yet straightforward approach to converting a low bandwidth analog signal into its digital representation. These type of converters often include built-in drivers for LCD or LED displays and are found in many portable instrument applications, including digital panel meters and digital multi-meters.

Single-Slope ADC Architecture

The simplest form of an integrating ADC uses a single-slope architecture (Figures 1a and 1b). Here, an unknown input voltage is integrated and the value compared against a known reference value. The time it takes for the integrator to trip the comparator is proportional to the unknown voltage (TINT/VIN). In this case, the known reference voltage must be stable and accurate to guarantee the accuracy of the measurement.

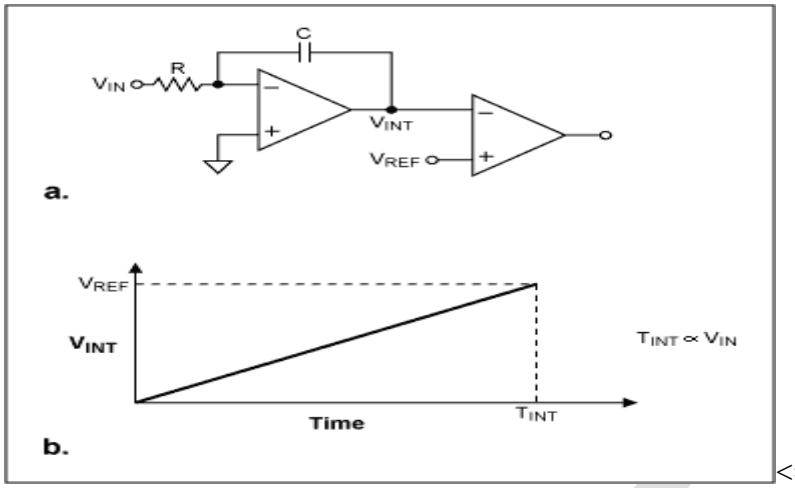


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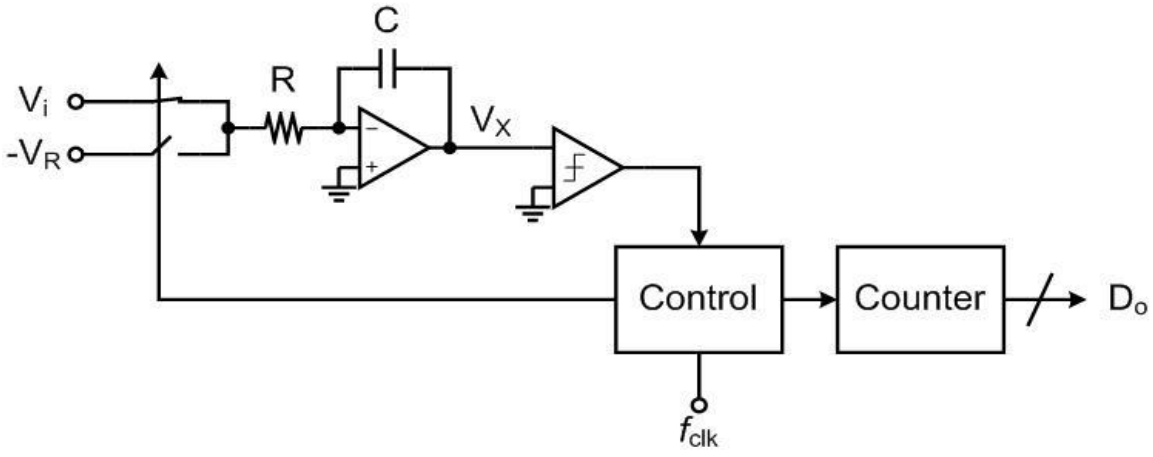
Fig .16. *Single-slope architecture ADC*

One drawback to this approach is that the accuracy is also dependent on the tolerances of the integrator's R and C values. Thus in a production environment, slight differences in each component's value change the conversion result and make measurement repeatability quite difficult to attain. To overcome this sensitivity to the component values, the dual-slope integrating architecture is used.

Dual-Slope ADC Architecture

A dual-slope ADC (DS-ADC) integrates an unknown input voltage (V_{IN}) for a fixed amount of time (T_{INT}), then "de-



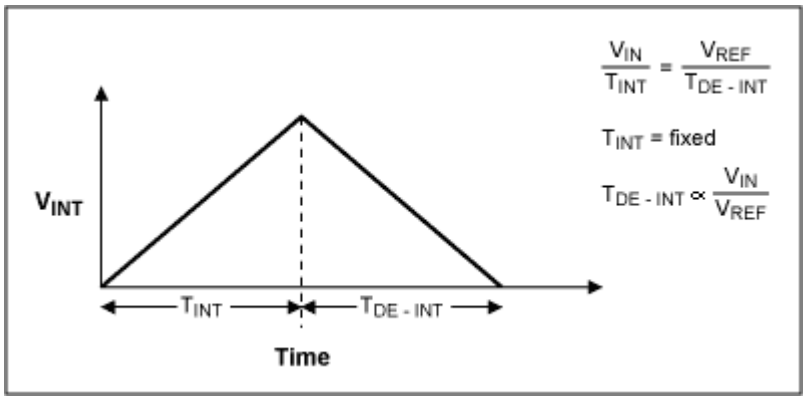


Fig .17. *Dual-slope integration.*

The key advantage of this architecture over the single-slope is that the final conversion result is insensitive to errors in the component values. That is, any error introduced by a component valueduring the integrate cycle will be cancelled out during the de-integrate phase.

From this equation, we see that the de-integrate time is proportional to the ratio of V_{IN} / V_{REF}
In the dual-slope converter, an integrator circuit is driven positive and negative in alternating cycles to ramp down and then up, rather than being reset to 0 volts at the end of every cycle. In one direction of ramping, the integrator is driven by the positive analog input signal (producing a negative, variable rate of output voltage change, or output *slope*) for a fixed amount of time, as measured by a counter with a precision frequency clock.

Then, in the other direction, with a fixed reference voltage (producing a fixed rate of output voltage change) with time measured by the same counter. The counter stops counting when the integrator's output reaches the same voltage as it was when it started the fixed-time portion of the cycle. The amount of time it takes for the integrator's capacitor to discharge back to its original output voltage, as measured by the magnitude accrued by the counter, becomes the digital output of the ADC circuit.

Question IES 2011:

With a block diagram, explain the function of a dual slope DVM.

A dual slope integrating type of A/D converter has an integrating capacitor of 0.1 uF and a resistance of 100 k ohm. the reference voltage is 2 V and the output of the integrator is not to exceed 10 V. What is the maximum time required for the output voltage to be integrated?

Answer: DVM is essentially an Analog to digital converter (A/D) with a digital display.

It uses dual slope integrating type A/D converter as explained above.

Maximum time taken by integrator = R * C = .01 sec = 10 ms

relative value corresponding to 10 V = 5 * 10 ms = 50 ms.

Over sampling ADC: This application note describes utilizing oversampling and averaging to increase the Resolution and SNR of analog-to-digital conversions. Oversampling and averaging can increase the solution of a measurement without resorting to the cost and complexity of using expensive off-chip ADCs.

This application note discusses how to increase the resolution of analog-to-digital (ADC)measurements by oversampling and averaging. Additionally, more in-depth analysis of ADC noise, types ofADC noise optimal for oversampling techniques, and example code utilizing oversampling and averaging is provided in appendices A, B, and C respectively at the end of this document.

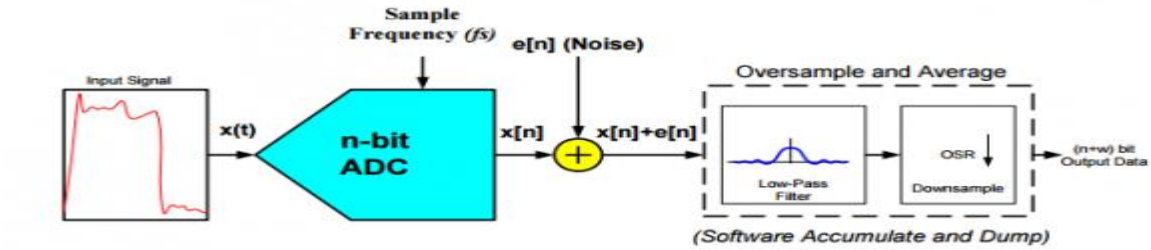


Fig.18. Over sampling ADC