LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

Name : R.RANI

Designation: Associate Professor

Department: Electronics & Communication Engineering

College: VEMU INSTITUTE OF TECHNOLOGY

COURSE OUTCOMES

C314.1	**Explain the characteristics of differential & operational amplifiers**
C314.2	Analyze Negative Feedback and its frequency response of Op-amp.
C314.3	Acquire the knowledge to design linear applications of op amps and also active filters
C314.4	Design circuits using Op- amp to generate sinusoidal & non sinusoidal wave forms and explain the operations of 555timer and PLL.
C314.5	Analyze data converters (ADC and DAC) Circuits using Op amps.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

B. Tech III-I Sem. (ECE) **L T P C**

3 1 0 3

15A04503 LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

- **Course Objectives:**
  - ☐ Design of OPAMPS, Classification of OPAMPs.
  - ☐ To study and design various linear applications of OPAMPs.
  - ☐ To study and design various non linear applications of OPAMPs
- **Course Outcomes:**
- Understand the basic building blocks of linear integrated circuits and its characteristics.
- Analyze the linear, non-linear and specialized applications of operational amplifiers.
- Understand the theory of ADC and DAC.
- Realize the importance of Operational Amplifier.

- **UNIT – I**

  Differential Amplifiers: Differential amplifier configurations, Balanced and unbalanced output differential amplifiers, current mirror, level Translator.

  Operational amplifiers: Introduction, Block diagram, Ideal op-amp, Equivalent Circuit Voltage Transfer curve, open loop op-amp configurations. Introduction to dual OP-AMP TL082 as a general purpose JFET-input Operational Amplifier.

- **UNIT-II**

  Introduction, feedback configurations, voltage series feedback, voltage shunt feedback

  and differential amplifiers, properties of Practical op-amp.

  Frequency response: Introduction, compensating networks, frequency response of internally compensated op-amps and non compensated op-amps, High frequency opamp equivalent circuit, open loop gain Vs frequency, closed loop frequency response, circuit stability, slew rate.

- **UNIT-III**

  DC and AC amplifiers, peaking amplifier, summing, scaling and averaging amplifiers, instrumentation amplifier, voltage to current converter, current to voltage converter, integrator, differentiator, active filters, First, Second and Third order Butterworth filter and its frequency response, Tow-Thomas biquad filter.

- **UNIT-IV**

  Oscillators, Phase shift and wein bridge oscillators, Square, triangular and saw tooth wave generators, Comparators, zero crossing detector, Schmitt trigger, characteristics and limitations.

- **Specialized applications:** 555 timer IC (monostable&astable operation) & its applications, PLL, operating principles, onolithic PLL, applications, analog multiplier and phase detection, Wide bandwidth precision analog multiplier MPY634 and its
- applications.

- **UNIT V**

Analog and Digital Data Conversions, D/A converter – specifications – weighted resistor type, R-2R Ladder type, Voltage Mode and Current-Mode R -2R Ladder types - switches for D/A converters, high speed sample-and-hold circuits, A/D Converters – specifications – Flash type – Successive Approximation type – Single Slope type – Dual Slope type – A/D Converter using Voltage-to-Time Conversion –Over-sampling A/D Converters.

UNIT-I

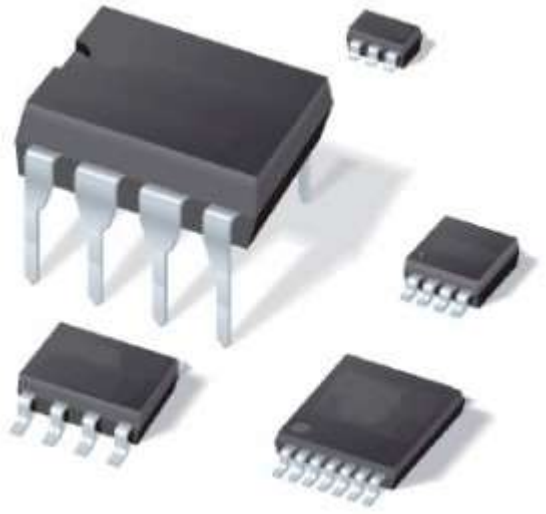
DIFFRENTIAL AMPLIFIERS

&

OP-AMP

INTEGRATED CIRCUITS

An integrated circuit (IC) is a miniature ,low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

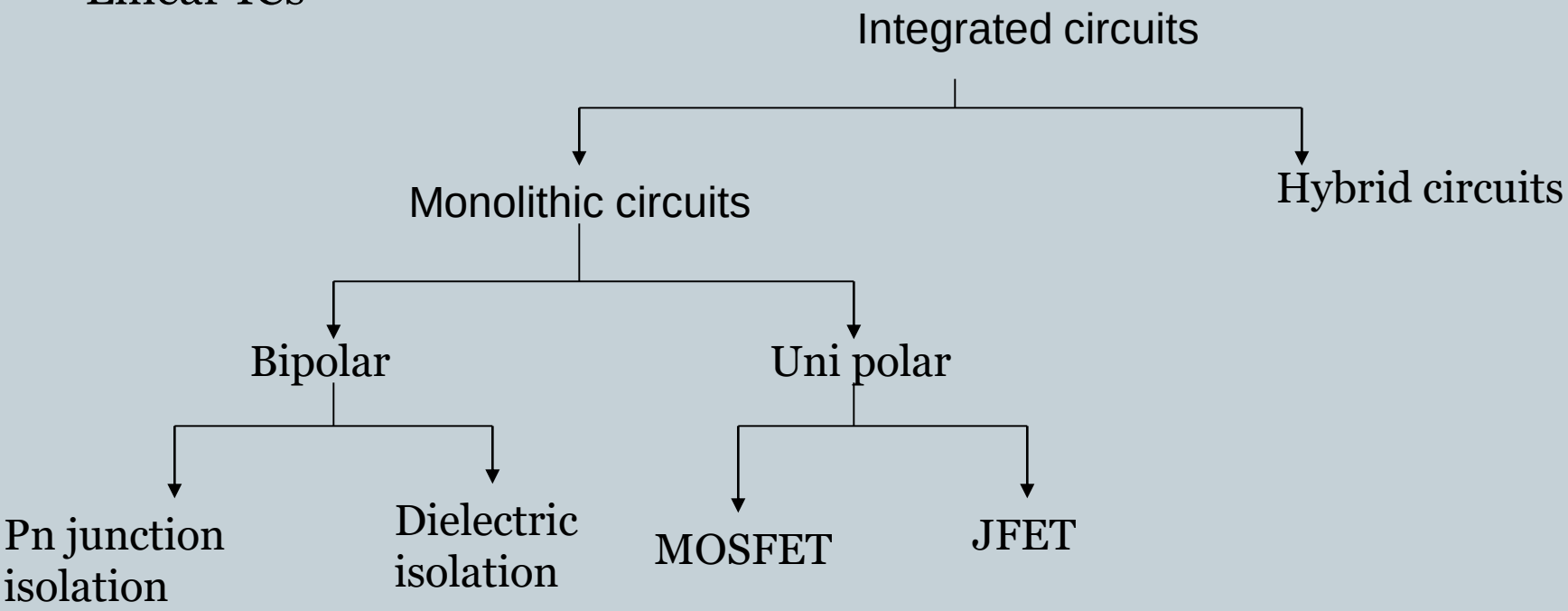


Advantages of integrated circuits

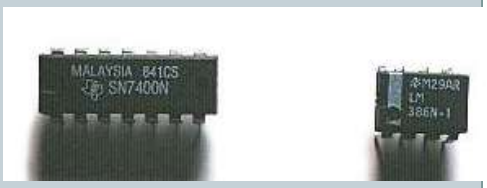
1. Miniaturization and hence increased equipment density.
2. Cost reduction due to batch processing.
3. Increased system reliability due to the elimination of soldered joints.
4. Improved functional performance.
5. Matched devices.
6. Increased operating speeds.
7. Reduction in power consumption

Classification

- Digital ICs
- Linear ICs



Chip size and Complexity



- Invention of Transistor (Ge) - 1947
- Development of Silicon - 1955-1959
- Silicon Planar Technology - 1959
- First ICs, SSI (3- 30gates/chip) - 1960
- MSI (30-300 gates/chip) - 1965-1970
- LSI (300-3000 gates/chip) -1970-1975
- VLSI (More than 3k gates/chip) - 1975
- ULSI (more than one million active devices are integrated on single chip)

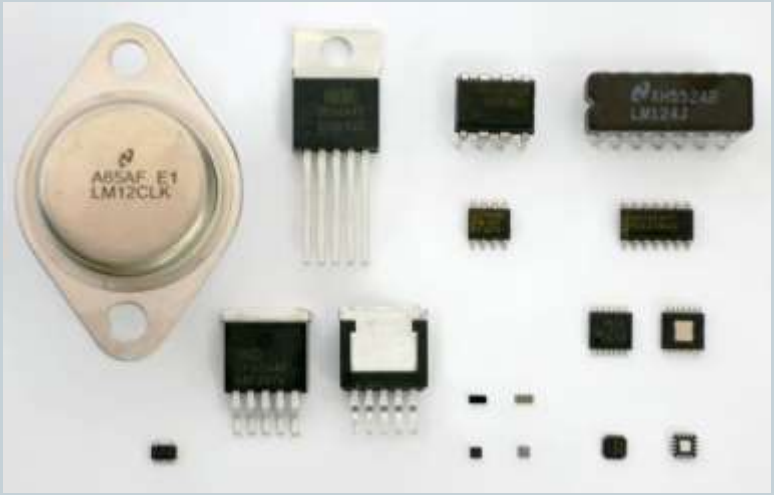
OPERATION AMPLIFIER

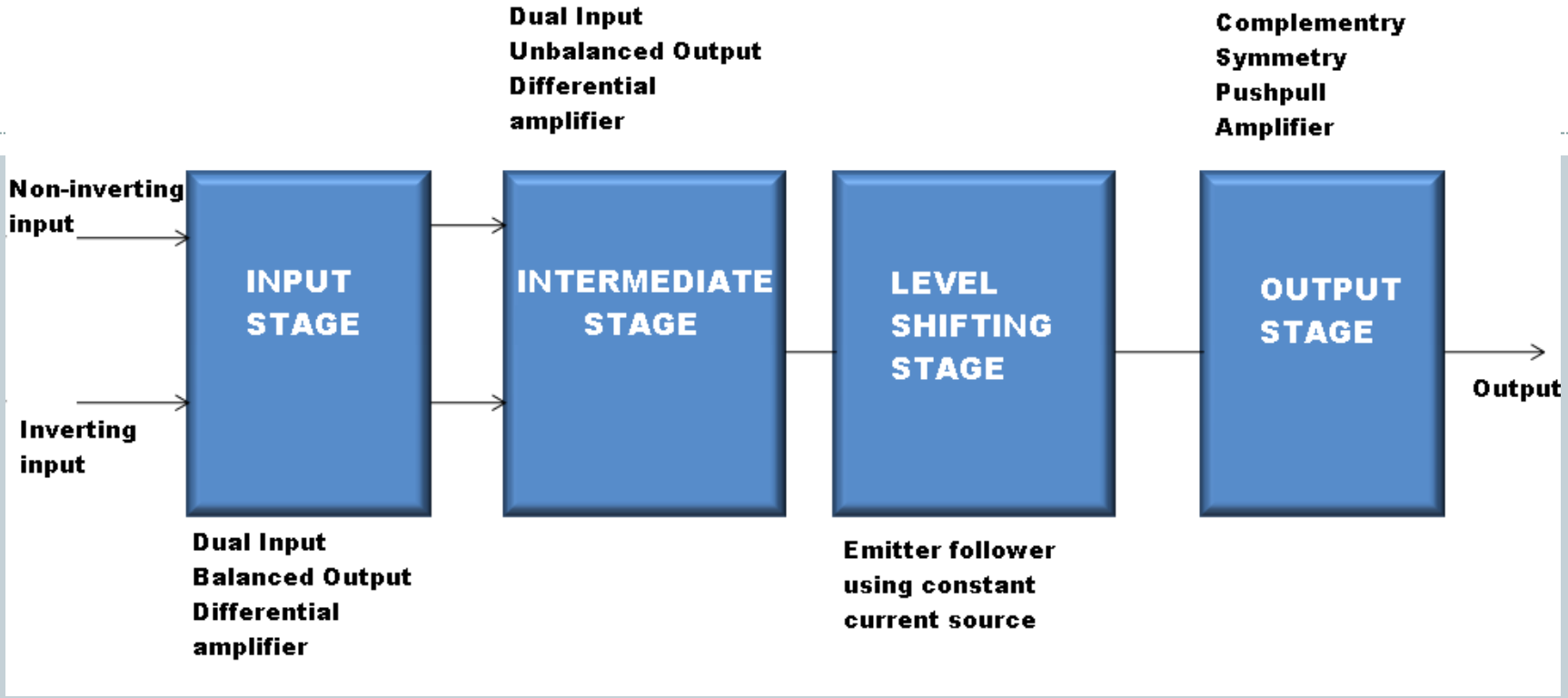
An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage.

It is a versatile device that can be used to amplify ac as well as dc input signals & designed for computing mathematical functions such as addition, subtraction ,multiplication, integration & differentiation

IC packages available

1. Metal can package.
2. Dual-in-line package.
3. Ceramic flat package.

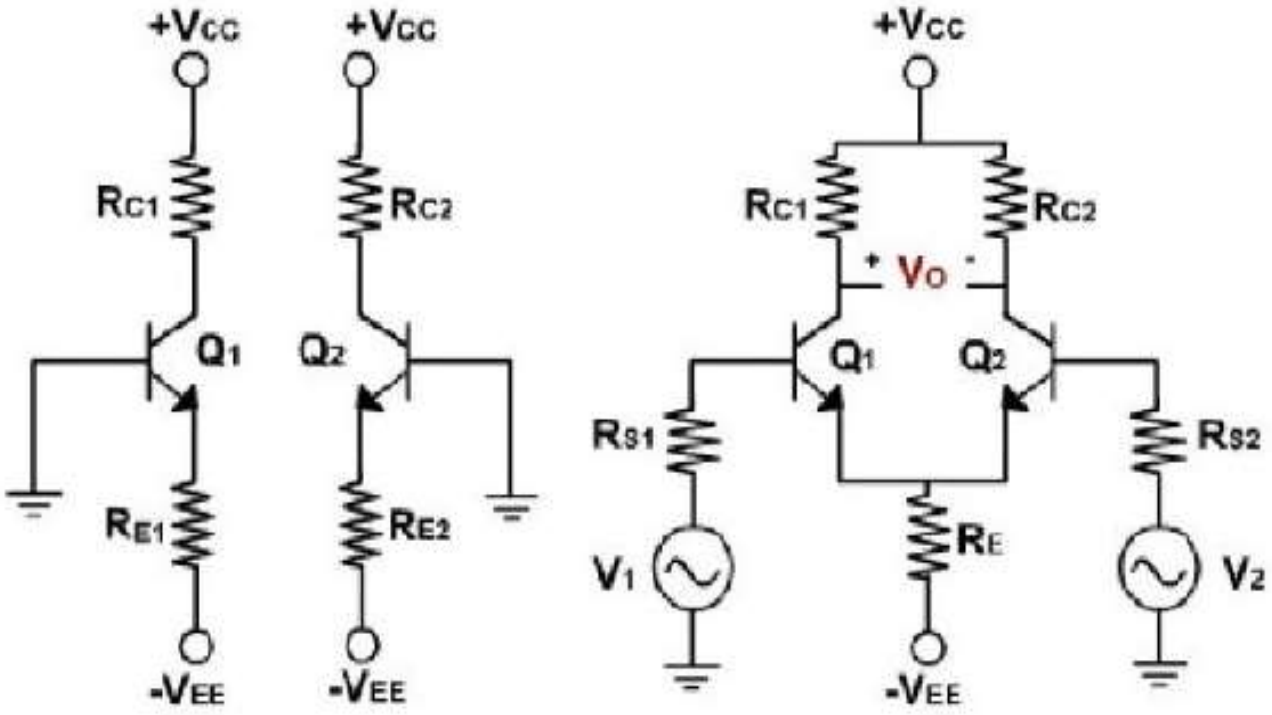



Dual Input
Unbalanced Output
Differential
amplifier
Complementry
Symmetry
Pushpull
Amplifier
Non-inverting
input
Inverting
input
INPUT
STAGE
INTERMEDIATE
STAGE
LEVEL
SHIFTING
STAGE
OUTPUT
STAGE
Output
Dual Input
Balanced Output
Differential
amplifier
Emitter follower
using constant
current source

DIFFERENTIAL AMPLIFIER:

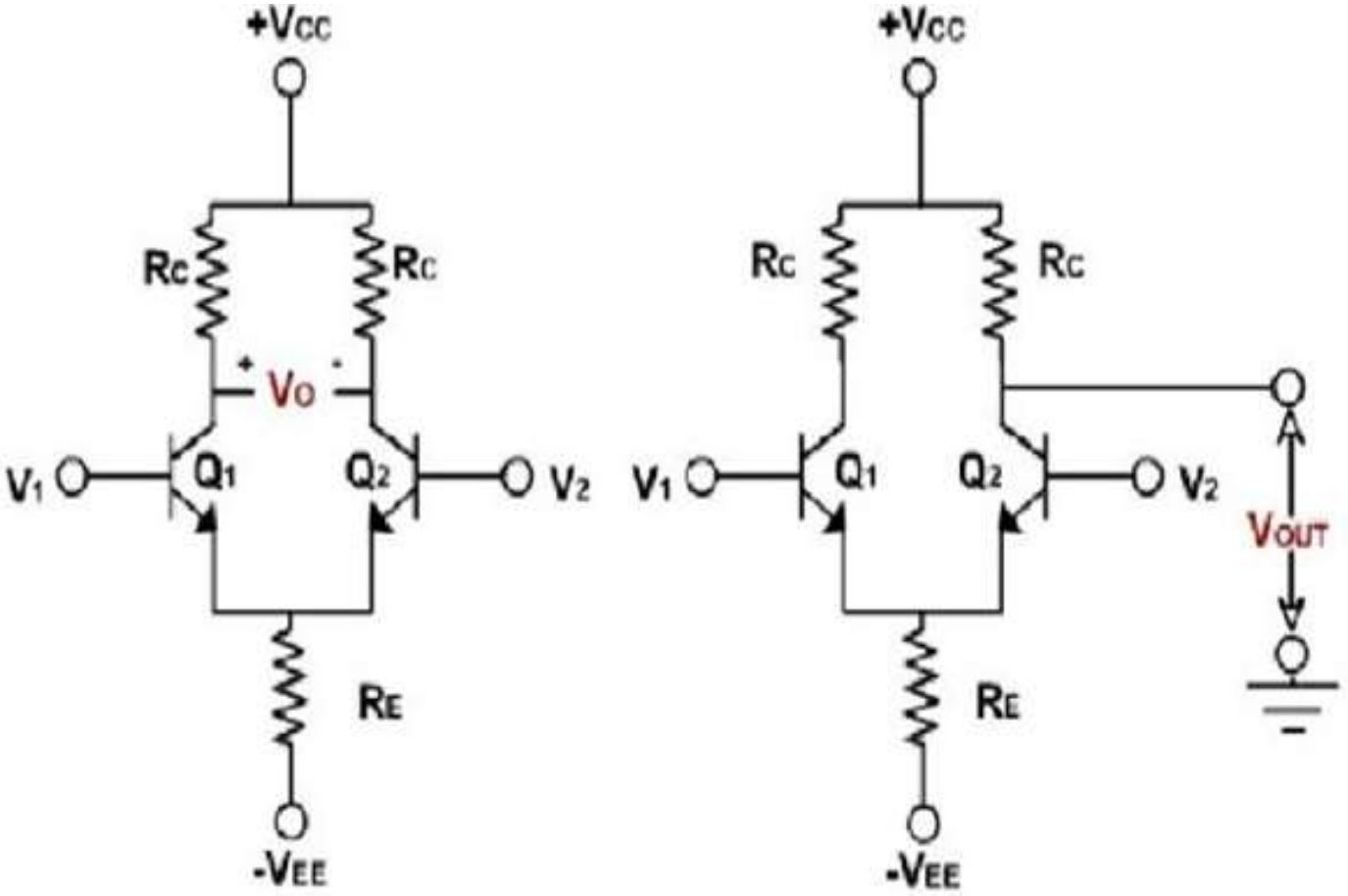
Differential amplifier is a basic building block of an op-amp. The function of a differential

amplifier is to amplify the difference between two input signals.



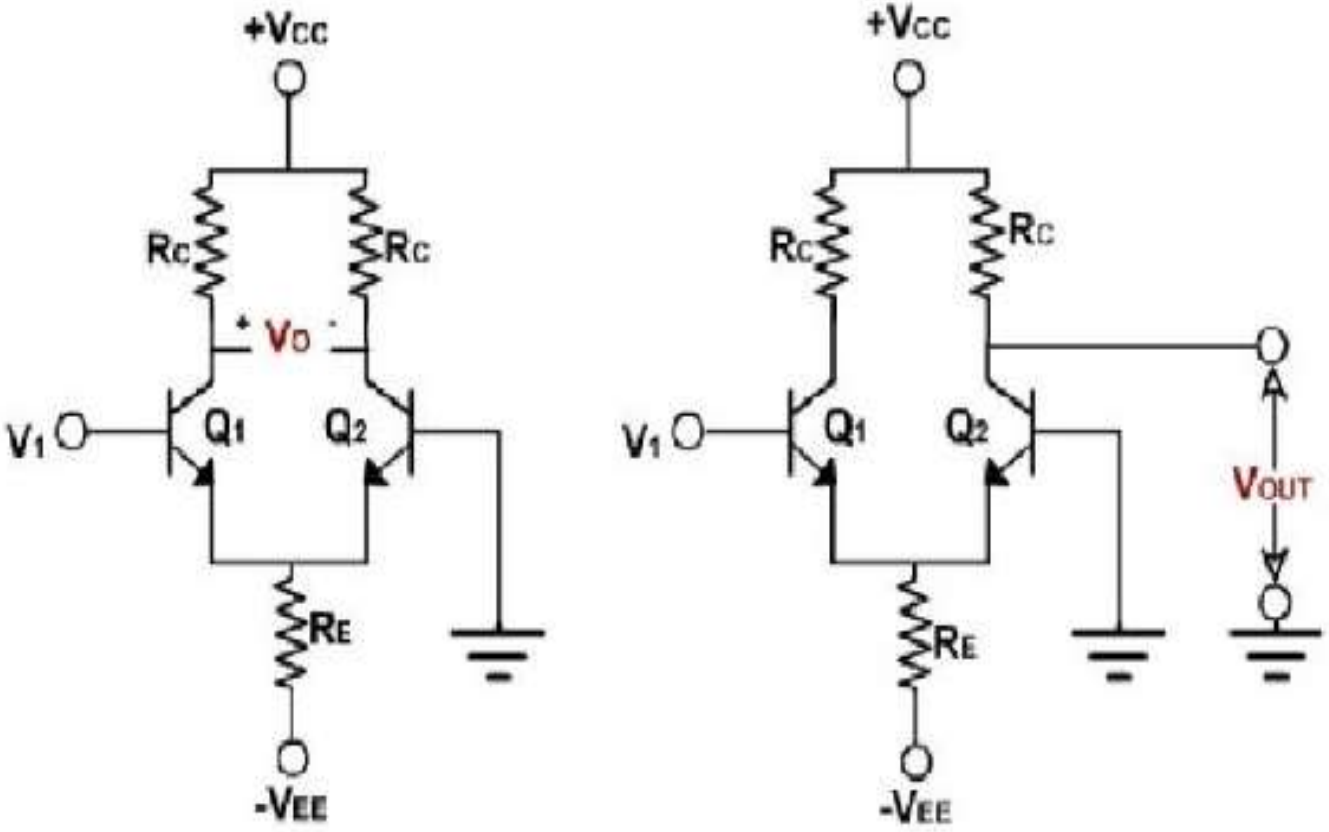
The four differential amplifier configurations are following:

1. Dual input, balanced output differential amplifier.
2. Dual input, unbalanced output differential amplifier.
3. Single input balanced output differential amplifier.
4. Single input unbalanced output differential amplifier



DUAL I/P BALANCED O/P AMP & DUAL I/P UNBALNCED O/P AMP

SINGLE I/P BALANCED O/P AMP & SINGLE I/P UNBALANCED O/P



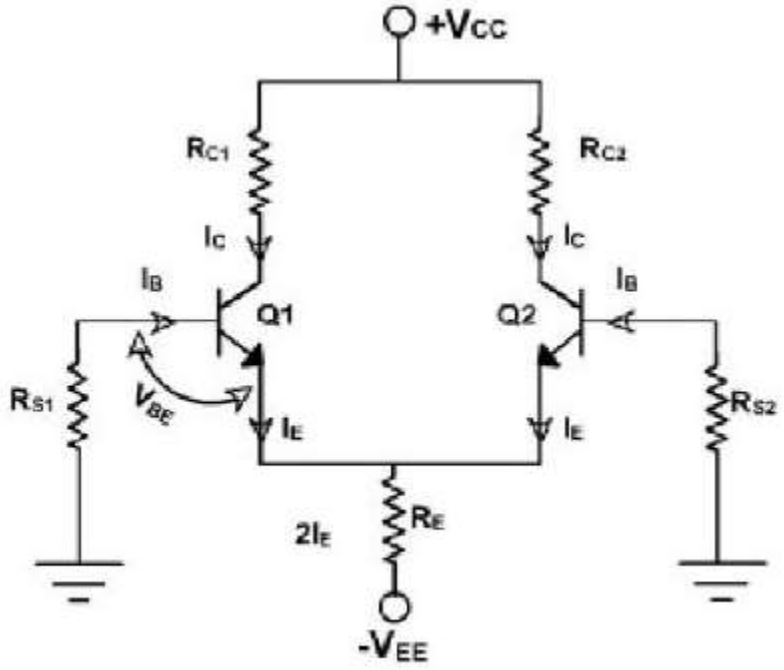
DUAL INPUT , BALANCED OUTPUT DIFFERENTIAL AMPLIFIER :

The circuit is shown in fig 1, v1 and v2 are the two inputs, applied to the bases of Q1 and Q2

transistors. The output voltage is measured between the two collectors C1 and C2 , which are at

same dc potentials.

DC ANALYSIS :



$$R_S I_B + V_{BE} + 2 I_E R_E = V_{EE}$$

But $I_B = \frac{I_E}{\beta_{dc}}$ and $I_C \approx I_E$

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E + R_S / \beta_{dc}}$$

$V_{BE} = 0.6V$ for S_i and $0.2V$ for G_e.

Generally $\frac{R_S}{\beta_{dc}} << 2R_E$ because R_S is the internal resistance of input signal.

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E}$$

VC =VCC – Ic Rc

and VCE = VC - VE

= VCC - IC RC + VBE

VCE = VCC + VBE - ICRC

AC ANALYSIS

DIFFRENTIAL I/P RESISTANCE

$$R_{i1} = \left.\frac{v_1}{i_{b1}}\right|_{v_2 = 0}$$

$$= \left.\frac{v_1}{i_{e1}/\beta}\right|_{v_2 = 0}$$

Substituting i_{e1}.

$$R_{i1} = \frac{\beta r'_e (r'_e + 2R_E)}{r'_e + R_E}$$

Since $R_E >> r'_e$

$\therefore \quad r'_e + 2R_E >> 2R_E$

or $\quad r'_e + R_E >> R_E$

$\therefore \quad R_{i1} = 2\beta r_e'$

Similarly.

$$R_{i2} = \left.\frac{V_2}{i_{b2}}\right|_{v_1 = 0}$$

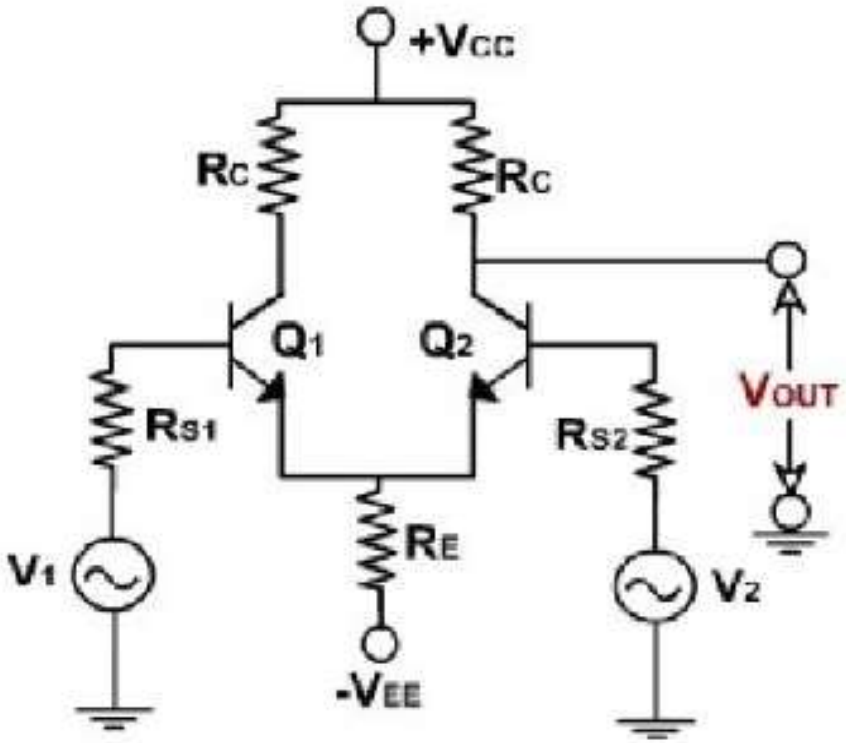
$$= \left.\frac{V_2}{i_{e2}/\beta}\right|_{v_1 = 0}$$

$$R_{i2} = 2\beta r'_e$$

OUT PUT RESISTANCE:

$R_{O1} = R_{O2} = R_C$

SINGLE I/P UNBALANCED O/P AMP



AC ANALYSIS

VOLTAGE GAIN

$$A_d = \frac{V_0}{V_d} = \frac{R_C}{2r'_e}$$

DIFFRENTIAL I/P RESISTANC

$$R_{i1} = \left.\frac{v_1}{i_{b1}}\right|_{v_2 = 0}$$

$$= \left.\frac{v_1}{i_{e1}/\beta}\right|_{v_2 = 0}$$

OUT PUT RESISTANCE:

$R_{O1} = R_{O2} = R_C$

Substituting i_{e1}.

$$R_{i1} = \frac{\beta r'_e (r'_e + 2R_E)}{r'_e + R_E}$$

Since $R_E >> r'_e$

$\therefore \quad r'_e + 2R_E >> 2R_E$

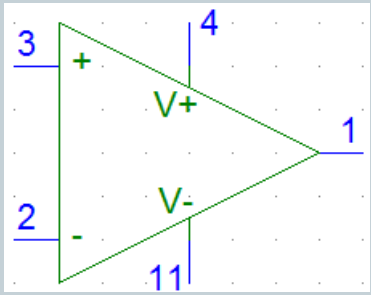
or $\quad r'_e + R_E >> R_E$

$\therefore \quad R_{i1} = 2\beta r_e'$

Terminals on an Op Amp

Positive power supply
(Positive rail)

Non-inverting
Input terminal

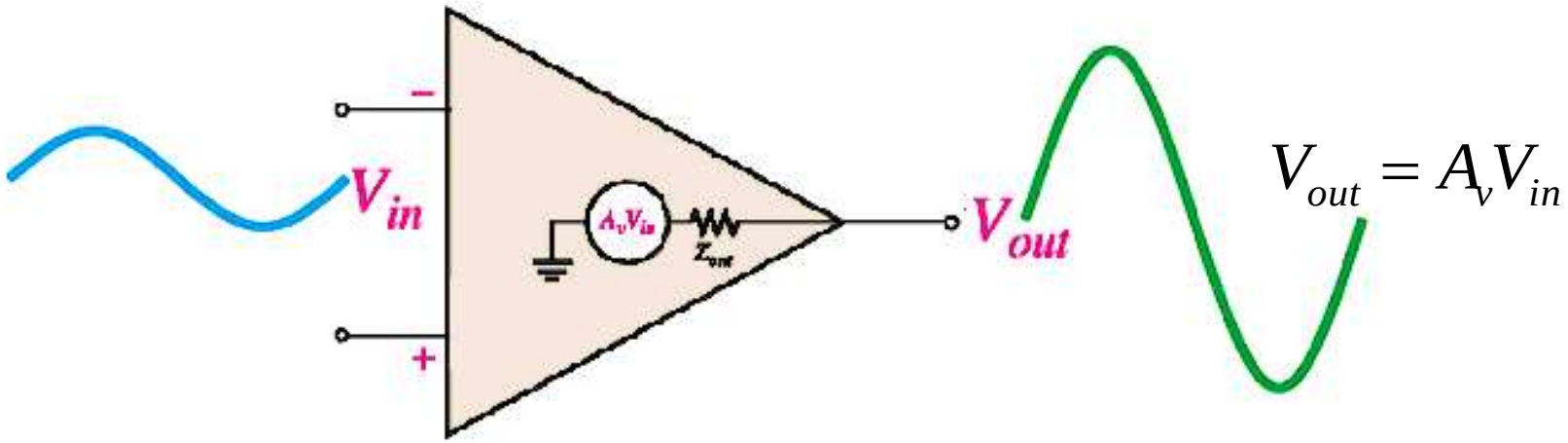


Output terminal

Inverting input
terminal

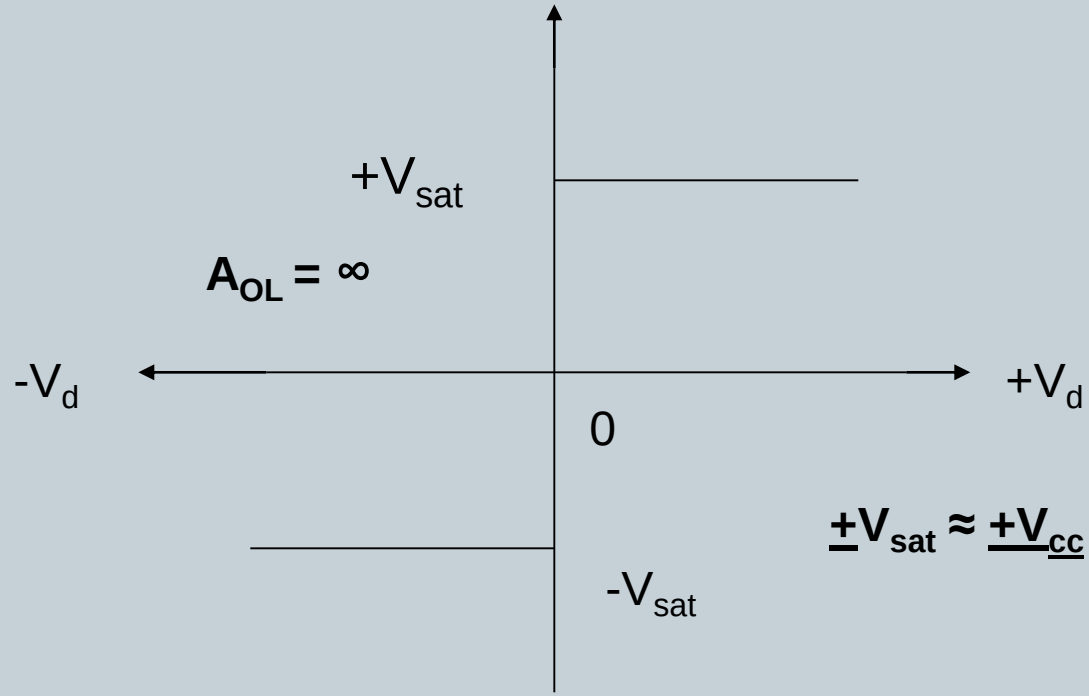
Negative power supply
(Negative rail)

1.2 Ideal Op-Amp



- **Infinite Open-Loop Gain**
  - Open-Loop Gain, A is the gain of the op-amp without feedback.
  - In the ideal op-amp, A is infinite
  - In real op-amp, A is 20k to 200k

Ideal Voltage transfer curve



Why op-amp is generally not used in open loop mode?

As open loop gain of op-amp is very large, very small input voltage drives the op-amp voltage to the saturation level. Thus in open loop configuration, the output is at its positive saturation voltage ($+V_{sat}$) or negative saturation voltage ($-V_{sat}$) depending on which input V_1 or V_2 is more than the other. For a.c. input voltages, output may switch between positive and negative saturation voltages

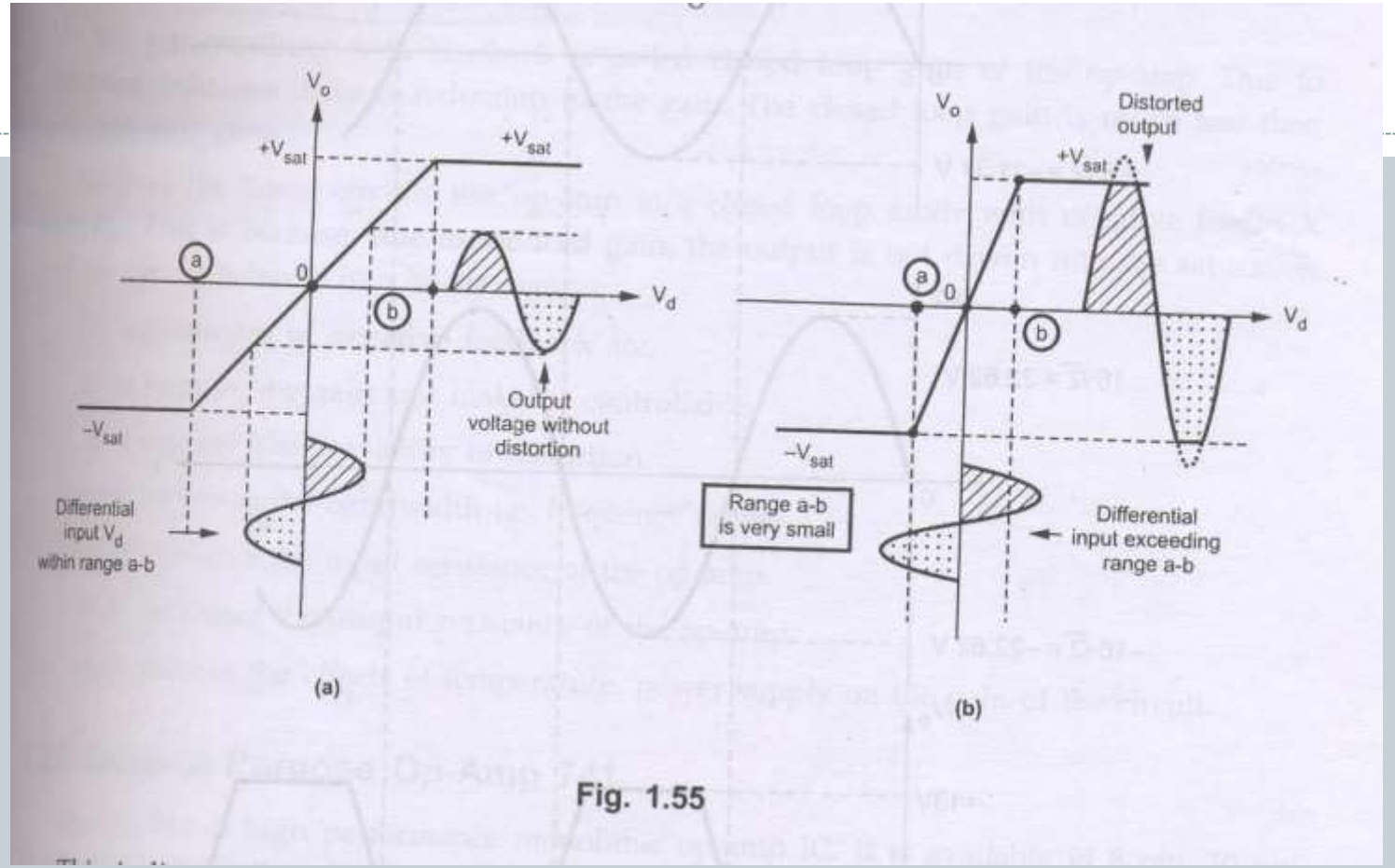
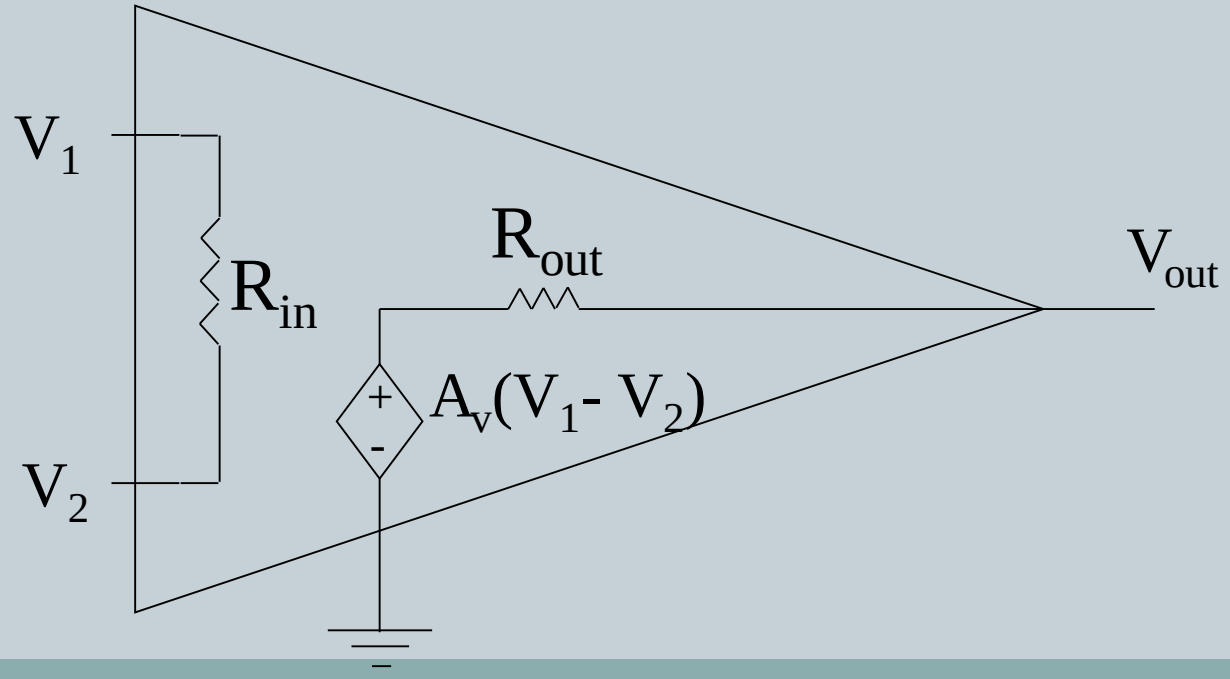


Fig. 1.55

This indicates the inability of op-amp to work as a linear small signal amplifier in the open loop mode. Hence the op-amp in open loop configuration is not used for the linear applications

Operational Amplifier Model

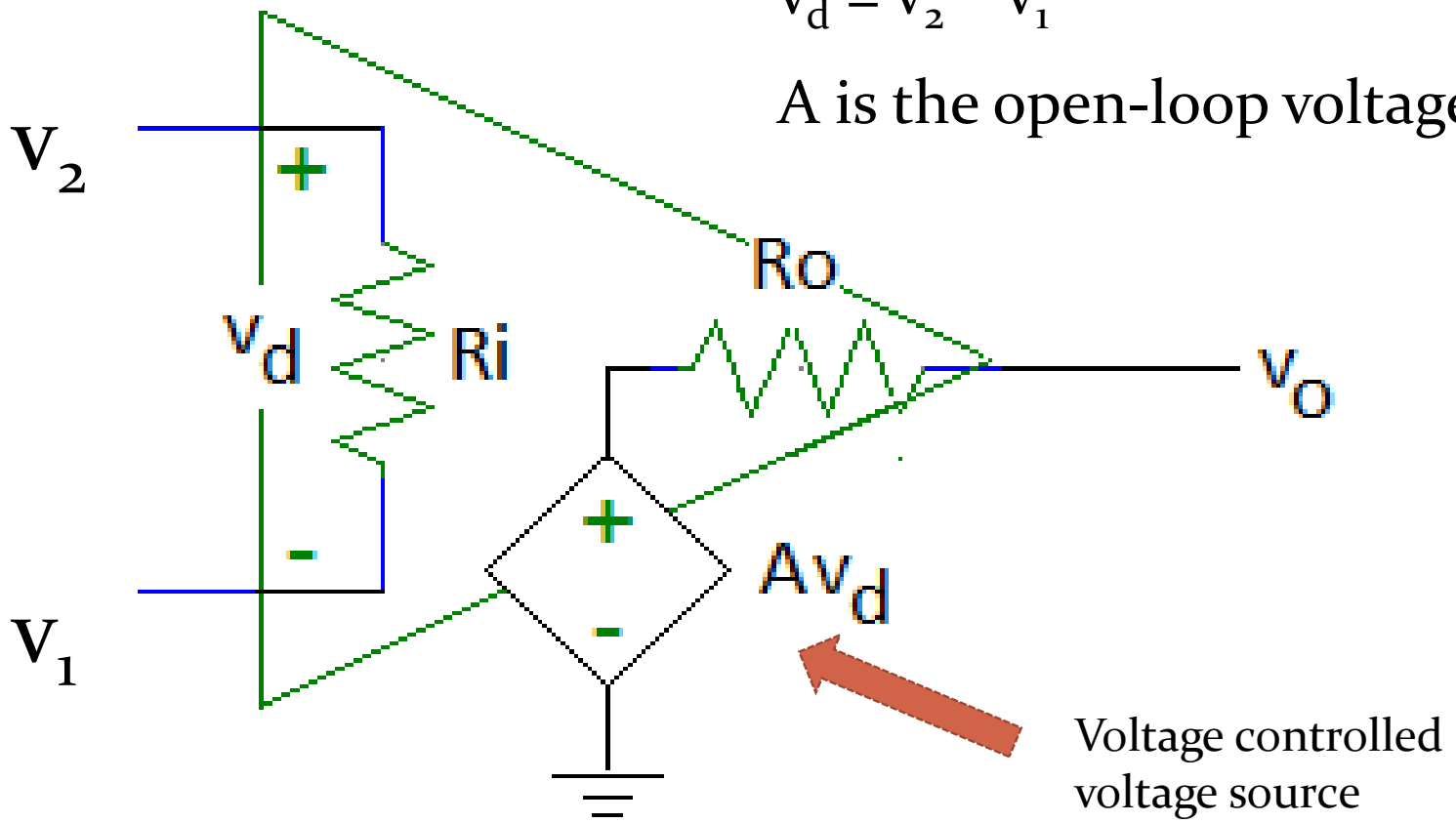
- An operational amplifier circuit is designed so that
  1) $V_{out} = A_v (V_1 - V_2)$ ($\mathbf{A_v}$ is a very large gain)
  2) Input resistance ($\mathbf{R_{in}}$) is very large
  3) Output resistance ($\mathbf{R_{out}}$) is very low



Op Amp Equivalent Circuit

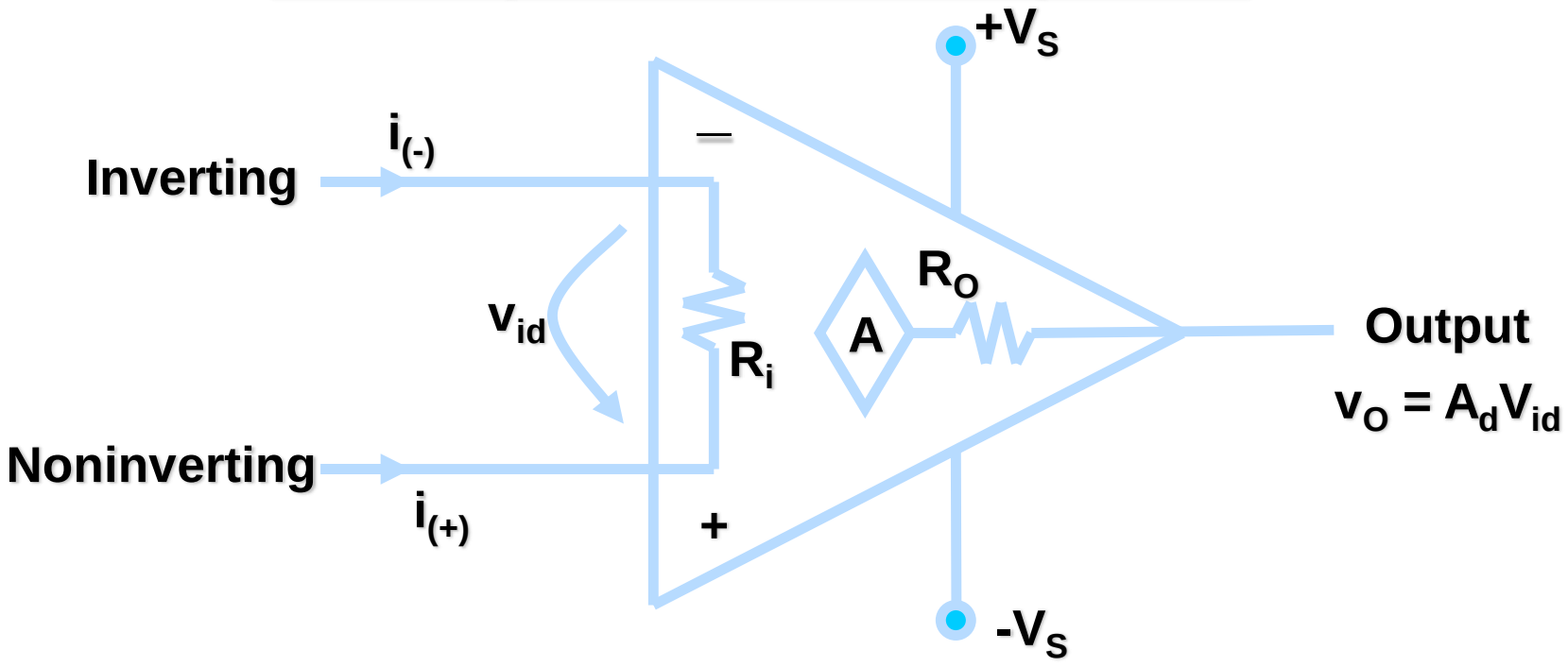
$v_d = v_2 - v_1$

A is the open-loop voltage gain



Voltage controlled voltage source

The Operational Amplifier



- $i_{(+)}$, $i_{(-)}$: Currents into the amplifier on the inverting and non-inverting lines respectively
- v_{id} : The input voltage from inverting to non-inverting inputs
- $+V_S$, $-V_S$: DC source voltages, usually +15V and –15V
- R_i : The input resistance, ideally infinity
- A : The gain of the amplifier. Ideally very high, in the $1x10^{10}$ range.
- R_O: The output resistance, ideally zero
- v_O: The output voltage; $v_O = A_{OL} v_{id}$ where A_{OL} is the open-loop voltage gain

The Ideal Operational Amplifier

- Open loop voltage gain A_{OL} $= \infty$
- Input Impedance R_i $= \infty$
- Output Impedance R_o $= 0$
- Bandwidth BW $= \infty$
- Zero offset ($V_o = 0$ when $V_1 = V_2 = 0$) V_{ios} $= 0$
- CMRR ρ $= \infty$
- Slew rate S $= \infty$
- No effect of temperature
- Power supply rejection ratio $PSRR$ $= 0$

An IDEAL OP AMP

An ideal op amp has the following characteristics:

1. Infinite open-loop voltage gain, $A_V \approx \infty$.
2. Infinite input resistance, $R_i \approx \infty$.
3. Zero output resistance, $R_o \approx 0$.
4. Infinite CMRR, $\rho = \infty$
5. The output voltage Vo=0; when $V_d = V_2 - V_1 = 0$
6. Change of output with respect to input, slew rate = ∞
7. Change in out put voltage with Temp., $\partial V_o / \partial V_i = 0$

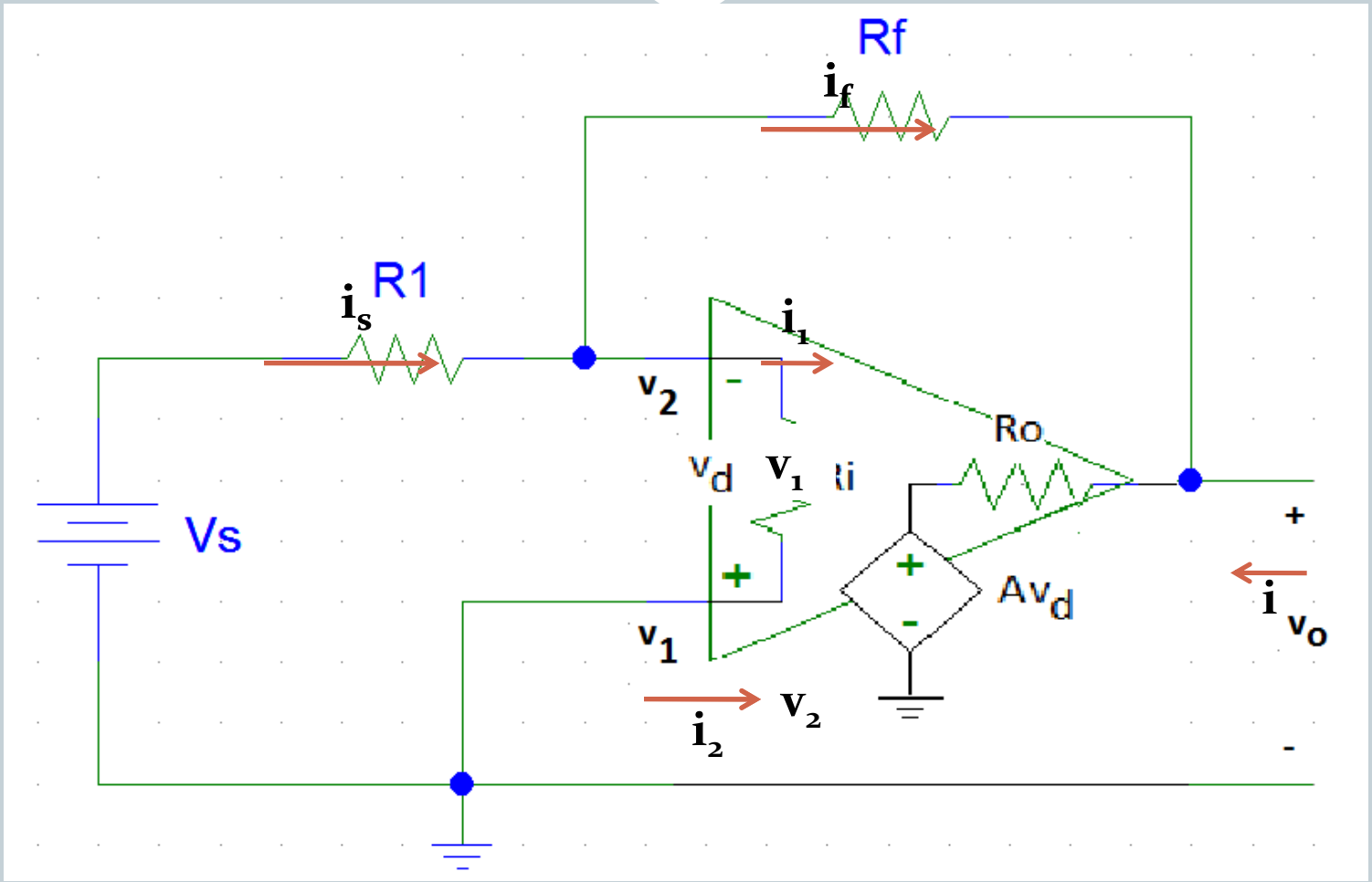
Ideal Op-amp

1. An ideal op-amp draws no current at both the input terminals I.e. $I_1 = I_2 = 0$. Thus its input impedance is infinite. Any source can drive it and there is no loading on the driver stage

2. The gain of an ideal op-amp is infinite, hence the differential input $V_d = V_1 - V_2$ is essentially zero for the finite output voltage V_o

3. The output voltage V_o is independent of the current drawn from the output terminals. Thus its output impedance is zero and hence output can drive an infinite number of other circuits

Example #3: Closed Loop Gain with Real Op Amp



IC Package types

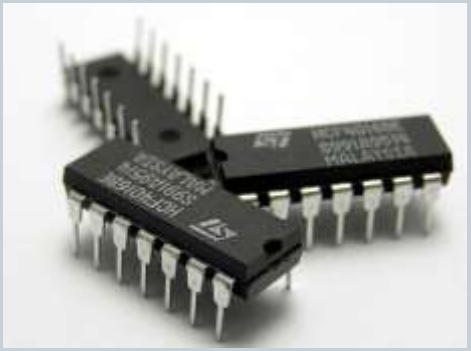
- Metal can Package
- Dual-in-line
- Flat Pack

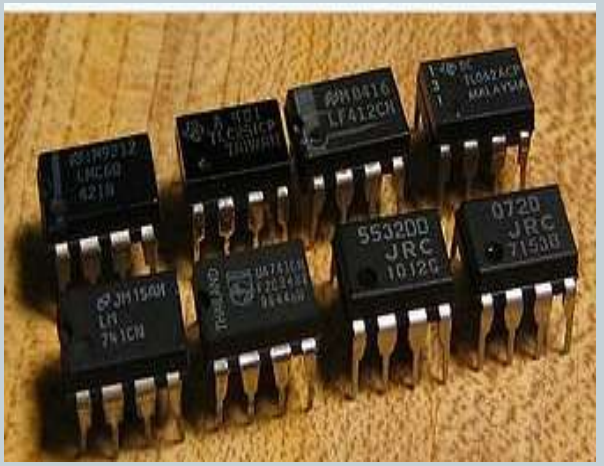
Metal can Packages

- The metal sealing plane is at the bottom over which the chip is bounded
- It is also called **transistor pack**

Doul-in-line Package

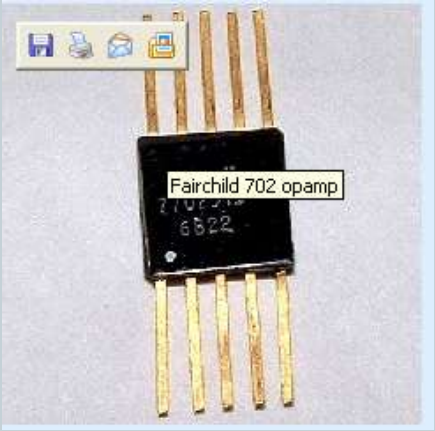
- The chip is mounted inside a plastic or ceramic case
- The 8 pin Dip is called **MiniDIP** and also available with 12, 14, 16, 20pins





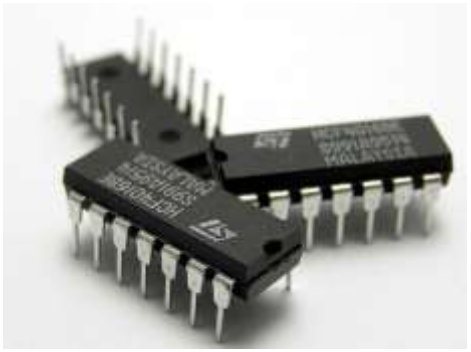
Flat pack

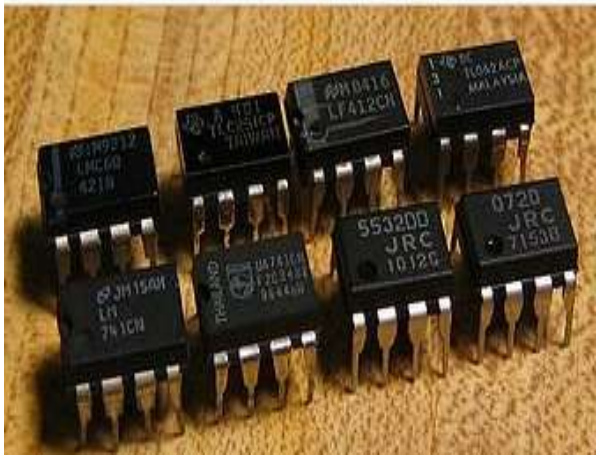
- The chip is enclosed in a rectangular ceramic case



Packages

The metal can (TO) Package





The Dual-in-Line (DIP) Package

The Flat Package

Temperature Ranges

1. Military temperature range : -55^{o} C to +125^{o} C (-55^{o} C to +85^{o} C)
2. Industrial temperature range: -20^{o} C to +85^{o} C (-40^{o} C to +85^{o} C)
3. Commercial temperature range: 0^{o} C to +70^{o} C (0^{o} C to +75^{o} C)

Manufacturer's Designation for Linear ICs

- Fairchild - µA, µAF
- National Semiconductor - LM,LH,LF,TBA
- Motorola - MC,MFC
- RCA - CA,CD
- Texas Instruments - SN
- Signetics - N/S,NE/SE
- Burr- Brown - BB

The 8pin DIP package of IC 741

The 8 pin DIP package of IC 741 is shown in the Fig. 1.59.

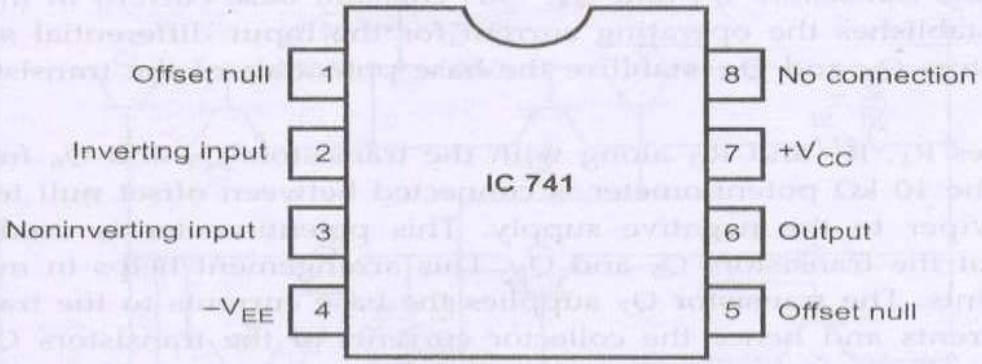


Fig. 1.59 8 Pin diagram

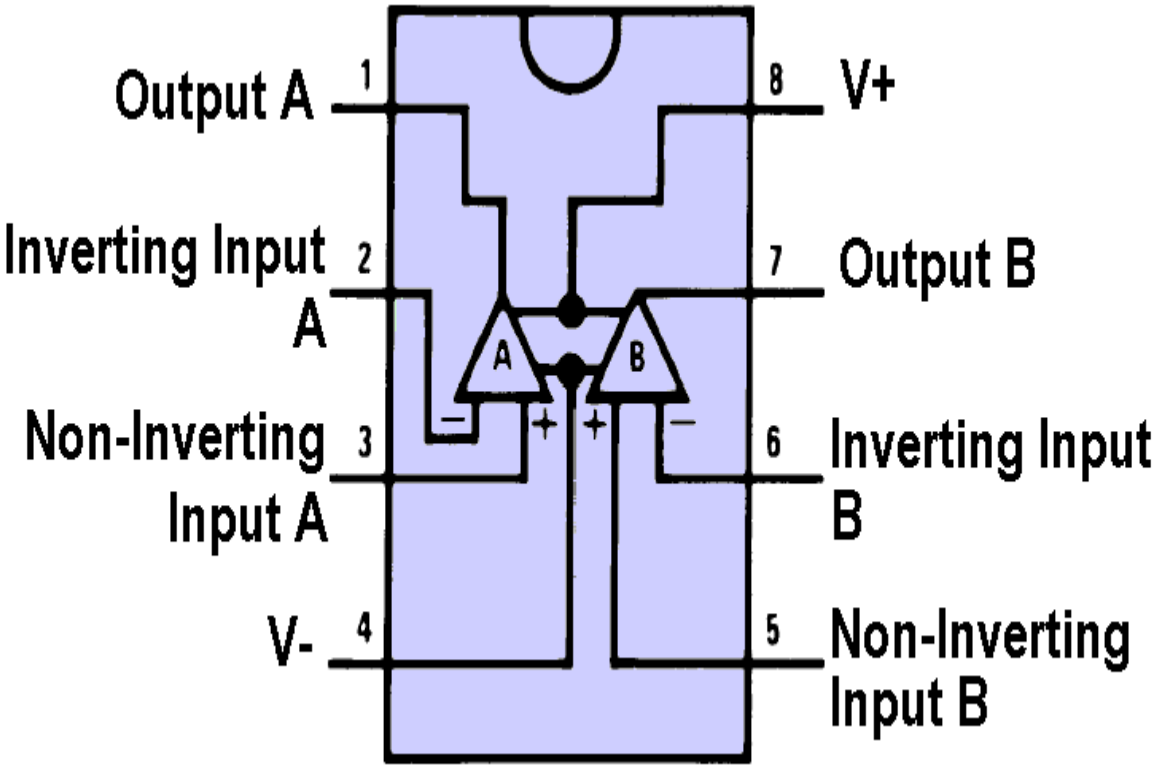
1.26.3 Ideal Vs Practical Characteristics of IC 741 Op-Amp

The Table 1.7 lists the ideal op-amp characteristics and the typical characteristics f
741 IC, a popular general purpose op-amp IC.

Sr. No	Parameter	Symbol	Ideal	Typical for 741 IC
1	Open loop voltage gain	A_{OL}	∞	2×10^5
2	Output impedance	Z_{out}	0	75 Ω
3	Input impedance	Z_{in}	∞	2 MΩ
4	Input offset current	I_{ios}	0	20 nA
5	Input offset voltage	V_{ios}	0	1 mV
6	Bandwidth	B.W	∞	1 MHz
7	CMRR	ρ	∞	90 dB
8	Slew rate	S	∞	0.5 V/μsec
9	Input bias current	I_b	0	80 nA
10	PSRR	PSRR	0	30 μV/V

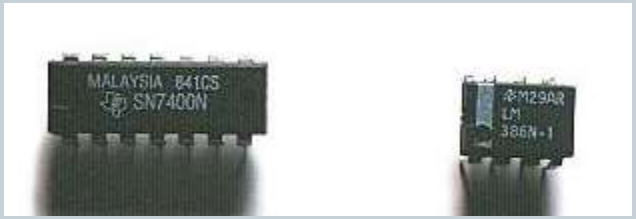
Table 1.7

TL 082 PIN CONFIGURATION



UNIT-II
NEGATIVE FEED BACK SYSTEM
&
FREQUENCY RESPONSE

Def: The “Integrated Circuit “ or IC is a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon.



Introduction

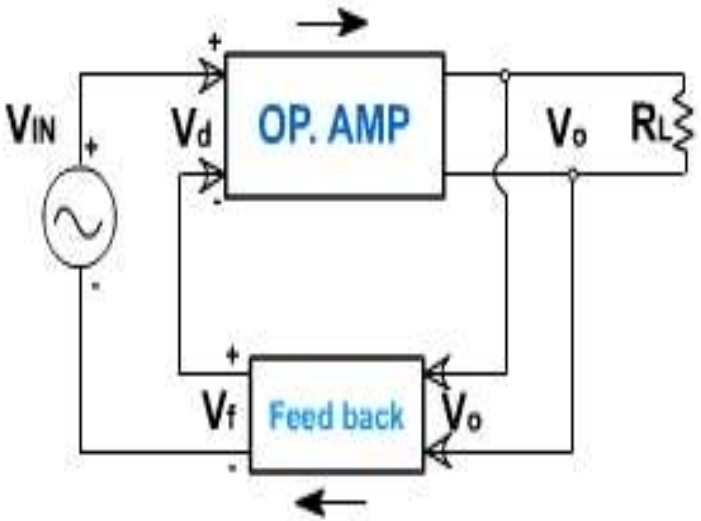
When the part of output is sampled & fed back to the input of amplifier.

Input & part of output which is fed back to the input

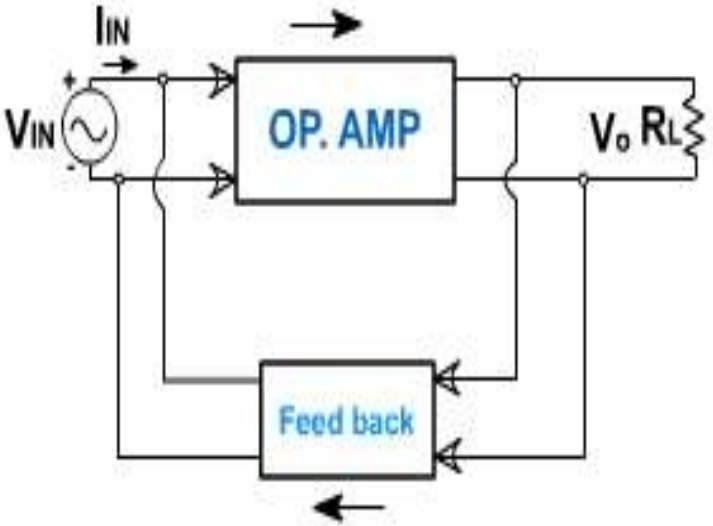
- Positive Feedback (In phase) ⟶ +
- Negative Feed back (Output of Phase) ⟶ -

Improve its performance & to make it more ideal.

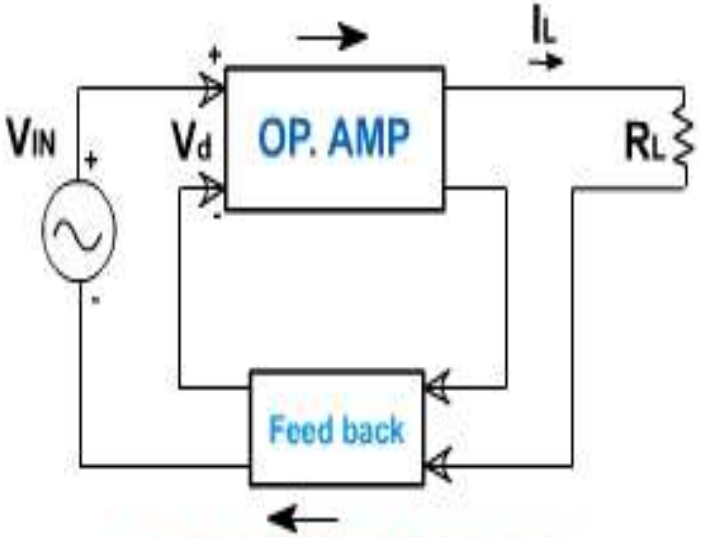
+ve Feedback results in oscillators & hence not used in amplifiers.



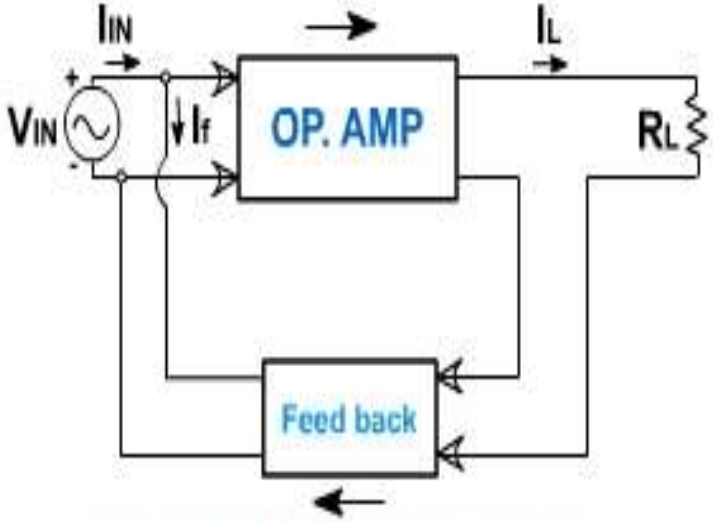
Voltage series feedback



Voltage shunt feedback

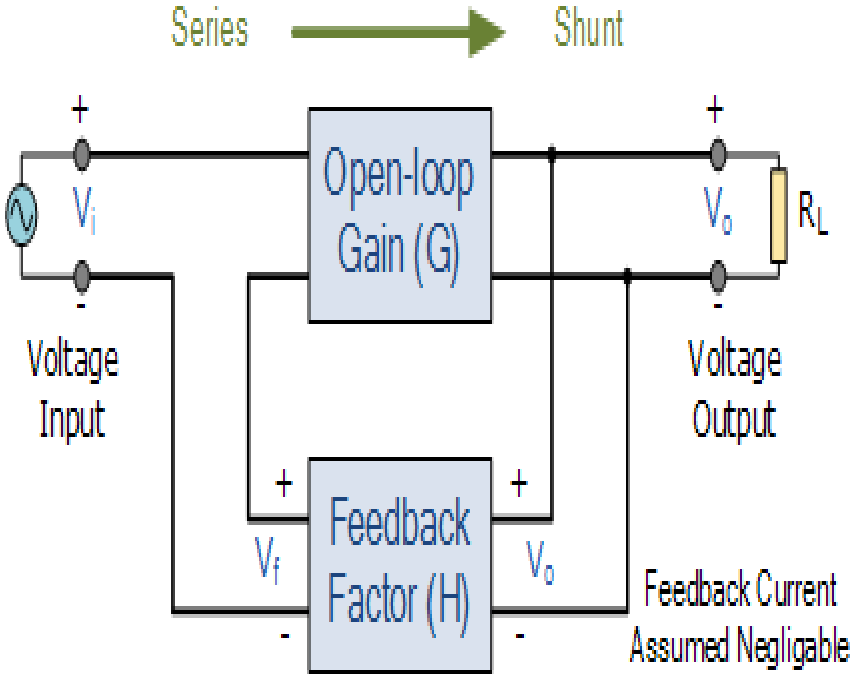


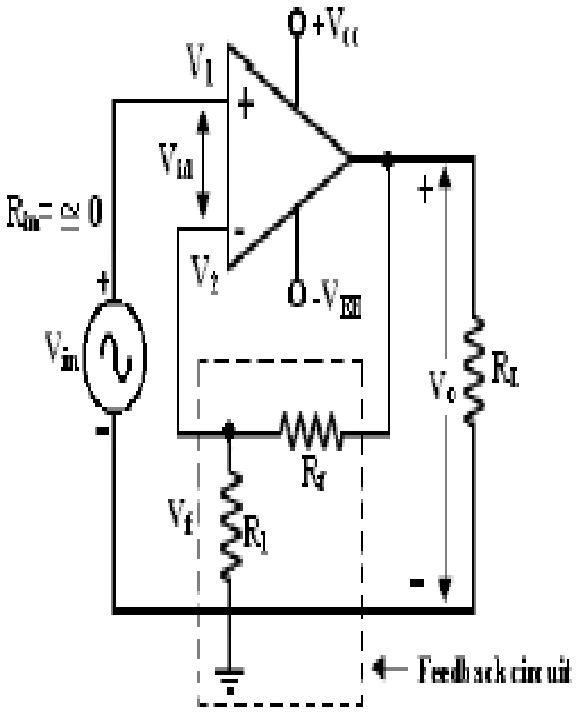
Current series feedback



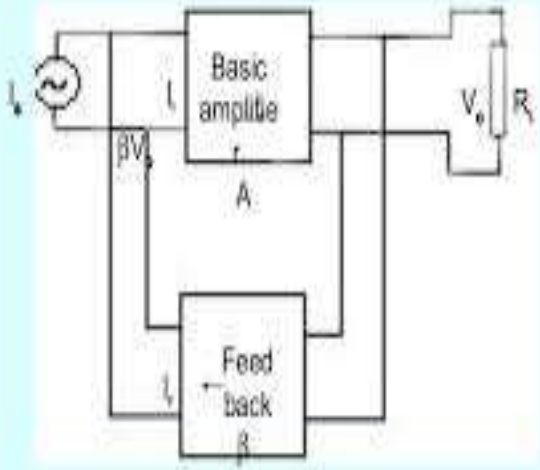
Current shunt feedback

Voltage Series Feedback Amplifier:

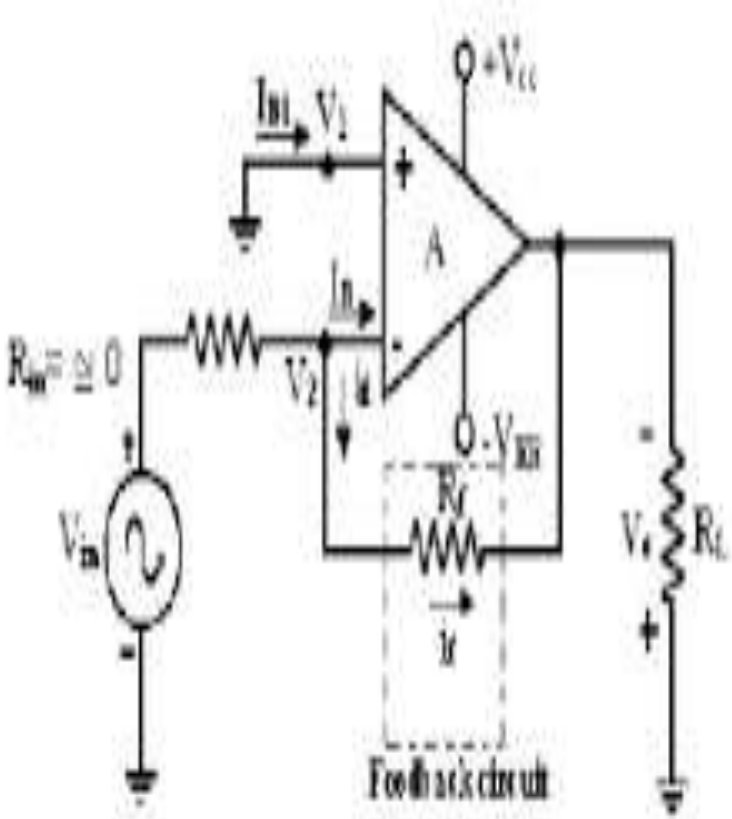




Voltage shunt feedback amplifier



This connection decreases both input resistance and output resistance.

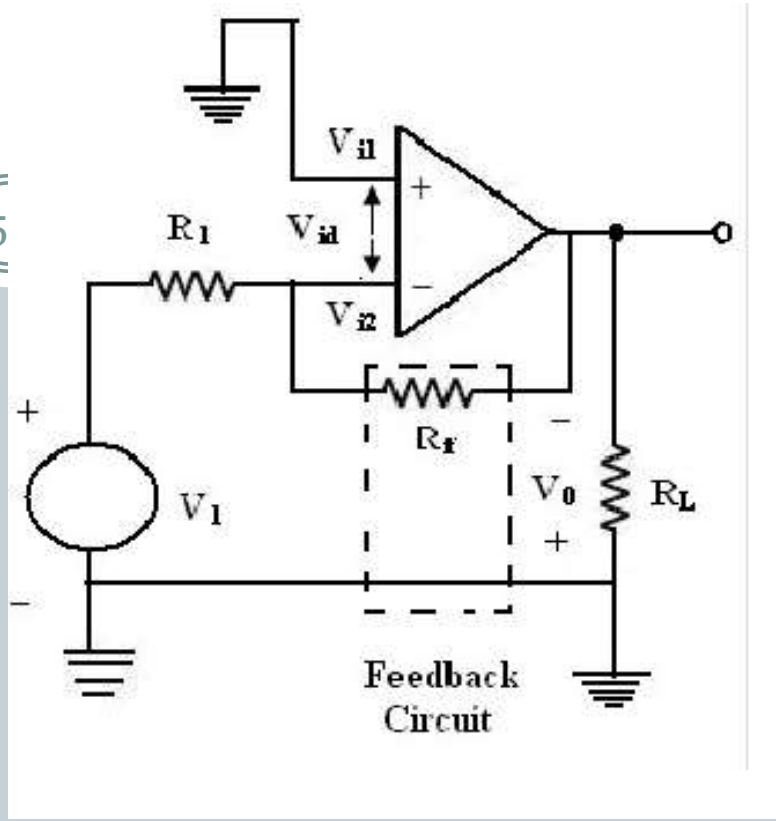


Selection of IC Package

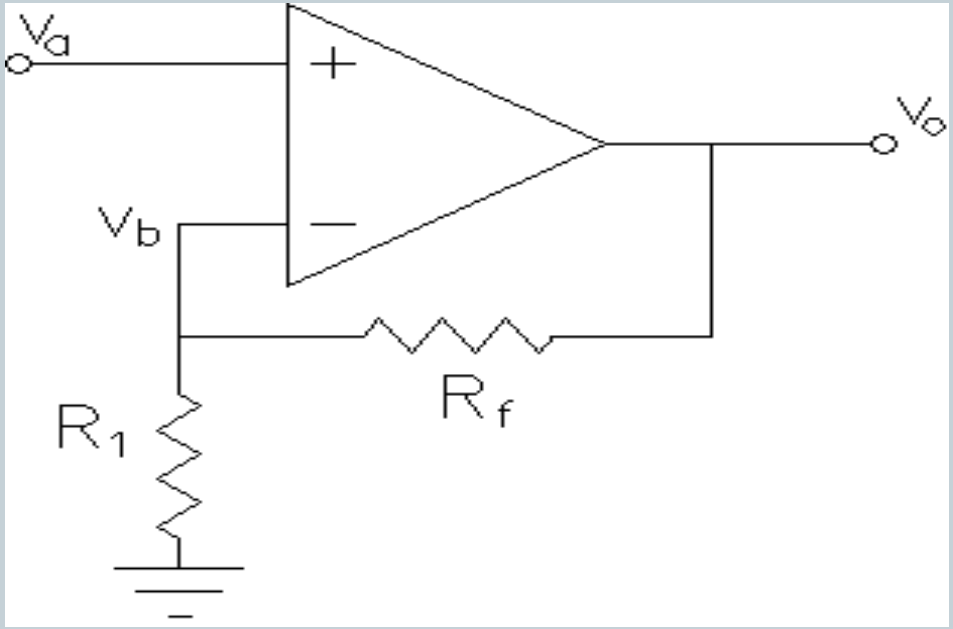
Type	Criteria
Metal can package	1. Heat dissipation is important 2. For high power applications like power amplifiers, voltage regulators etc.
DIP	1. For experimental or bread boarding purposes as easy to mount 2. If bending or soldering of the leads is not required 3. Suitable for printed circuit boards as lead spacing is more
Flat pack	1. More reliability is required 2. Light in weight 3. Suited for airborne applications

Inverting Op-Amp

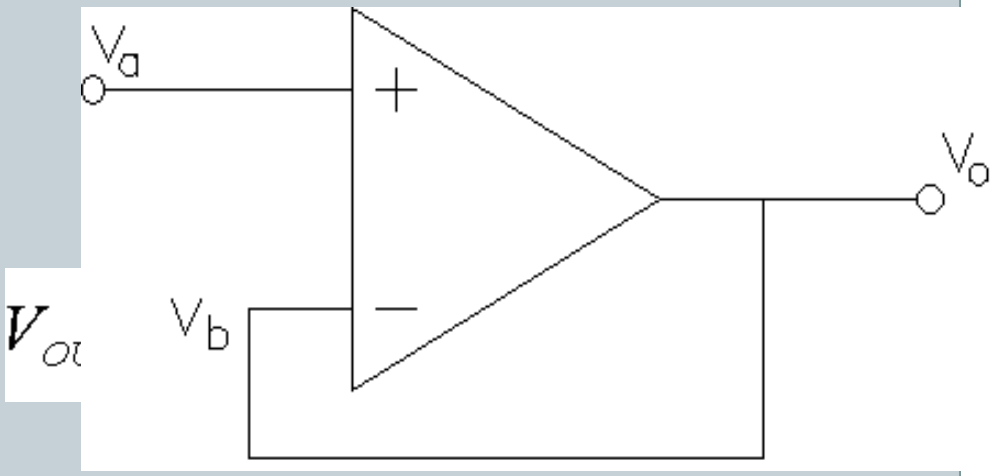
$$V_{OUT} = -V_{IN}\frac{R_f}{R_1}$$



Non-Inverting Amplifier



Voltage follower



Characteristics and performance parameters of Op-amp

- Input offset Voltage
- Input offset current
- Input bias current
- Differential input resistance
- Input capacitance
- Open loop voltage gain
- CMRR
- Output voltage swing

Basic Information of an Op-amp

Power supply connection:

The power supply voltage may range from about $\pm$ 5V to $\pm$ 22V.

The common terminal of the V^+ and V^- sources is connected to a reference point or ground.

Differential Amplifier

$$V_o = A_d (V_1 - V_2)$$

$$A_d = 20 \log_{10} (A_d) \text{ in dB}$$

$$V_c = \frac{(V_1 + V_2)}{2}$$

$$\text{CMRR} = \rho = \left| \frac{A_d}{A_c} \right|$$

1. Input Offset Voltage

INPUT OFFSET VOLTAGE

The differential voltage that must be applied between the two input terminals of an op-amp, to make the output voltage zero.

It is denoted as $\mathbf{V_{ios}}$

For op-amp 741C the input offset voltage is 6mV

2. Input offset current

The algebraic difference between the currents flowing into the two input terminals of the op-amp

It is denoted as $I_{ios} = | I_{b1} - I_{b2}|$

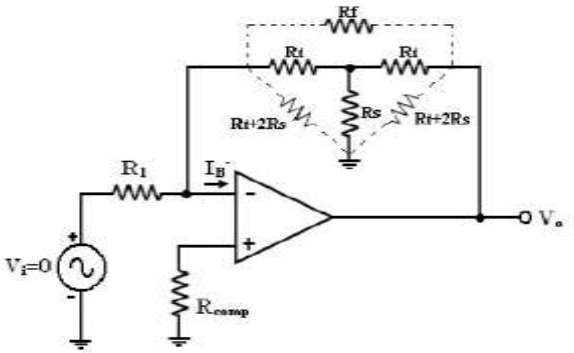
For op-amp 741C the input offset current is 200nA

3. Input bias current

The average value of the two currents flowing into the op-amp input terminals

It is expressed mathematically as

$$\frac{I_{b1} + I_{b2}}{2}$$



For 741C the maximum value of I_b is 500nA

4. Differential Input Resistance

It is the equivalent resistance measured at either the inverting or non-inverting input terminal with the other input terminal grounded

It is denoted as R_i

For 741C it is of the order of 2MΩ

7. CMRR

It is the ratio of differential voltage gain A_d to common mode voltage gain A_c

CMRR = A_d / A_c

A_d is open loop voltage gain A_{OL} and $A_c = V_{OC} / V_c$

For op-amp 741C CMRR is 90 dB

8. Output Voltage swing

The op-amp output voltage gets saturated at $+V_{cc}$ and $-V_{EE}$ and it cannot produce output voltage more than $+V_{cc}$ and $-V_{EE.}$ Practically voltages $+V_{sat}$ and $-V_{sat}$ are slightly less than $+V_{cc}$ and $-V_{EE}$.

For op-amp 741C the saturation voltages are $\pm$ 13V for supply voltages $\pm$ 15V

12. Power supply rejection ratio

PSRR is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it, keeping the other power supply voltage constant. It is also called as power supply sensitivity (PSV)

$PSRR = (\Delta v_{ios} / \Delta V_{cc})|_{\text{constant } V_{EE}}$

$PSRR = (\Delta v_{ios} / \Delta V_{EE})|_{\text{constant } V_{cc}}$

The typical value of PSRR for op-amp 741C is 30μV/V

14. Slew rate

It is defined as the maximum rate of change of output voltage with time. The slew rate is specified in V/µsec

$$\text{Slew rate} = S = dV_o / dt \big|_{max}$$

It is specified by the op-amp in unity gain condition.

The slew rate is caused due to limited charging rate of the compensation capacitor and current limiting and saturation of the internal stages of op-amp, when a high frequency large amplitude signal is applied.

Slew rate

It is given by $dV_c/dt = I/C$

For large charging rate, the capacitor should be small or the current should be large.

$$S = I_{max} / C$$

For 741 IC the charging current is 15 µA and the internal capacitor is 30 pF. S= 0.5V/ µsec

Slew rate equation

$V_s = V_m \sin\omega t$

$V_o = V_m \sin\omega t$

$$\frac{dVo}{dt} = V_m\,\omega\cos\omega t$$

$$\text{S = slew rate} = \left.\frac{dVo}{dt}\right|_{max}$$

$S = V_m\,\omega = 2\,\pi\,f\,V_m$

$S = 2\,\pi\,f\,V_m$ V / sec

This is also called **full power bandwidth** of the op-amp

For distortion free output, the maximum allowable input frequency f_m can be obtained as

$$f_m = \frac{S}{2\Pi V_m}$$

15. Gain – Bandwidth product

It is the bandwidth of op-amp when voltage gain is unity (1). It is denoted as GB.

The GB is also called unity gain bandwidth (UGB) or closed loop bandwidth

It is about 1MHz for op-amp 741C

16. Equivalent Input Noise Voltage and Current

The noise is expressed as a power density

Thus equivalent noise voltage is expressed as V^2 /Hz

while the equivalent noise current is expressed as A^2 /Hz

17. Average temperature coefficient of offset parameters

The average rate of change of input offset voltage per unit change in temperature is called average temperature coefficient of input offset voltage or input offset voltage drift

It is measured in $\mu V/^oC$. For 741 C it is 0.5 $\mu V/^oC$

The average rate of change of input offset current per unit change in temperature is called average temperature coefficient of input offset current or input offset current drift

It is measured in $nA/^oC$ or $pA/^oC$. For 741 C it is 12 $pA/^oC$

18. Output offset voltage (V_{oos})

The output offset voltage is the dc voltage present at the output terminals when both the input terminals are grounded.

It is denoted as V_{oos}

Ideal Inverting amplifier	Ideal non-inverting amplifier
1. Voltage gain=$-R_f/R_1$	1. Voltage gain=$1+R_f/R_1$
2. The output is inverted with respect to input	2. No phase shift between input and output
3. The voltage gain can be adjusted as greater than, equal to or less than one	3. The voltage gain is always greater than one
4. The input impedance is R_1	4. The input impedance is very large

Thermal Voltage Drift

It is defined as the average rate of change of input offset voltage per unit change in temperature. It is also called as input offset voltage drift

Input offset voltage drift = $\frac{\Delta V_{ios}}{\Delta T}$

ΔV_{ios} = change in input offset voltage

ΔT = Change in temperature

AC Characteristics

Frequency Response

Ideally, an op-amp should have an infinite bandwidth but practically op-amp gain decreases at higher frequencies. Such a gain reduction with respect to frequency is called as roll off.

The plot showing the variations in magnitude and phase angle of the gain due to the change in frequency is called ***frequency response*** of the op-amp

When the gain in decibels, phase angle in degrees are plotted against logarithmic scale of frequency, the plot is called ***Bode Plot***

The manner in which the gain of the op-amp changes with variation in frequency is known as the *magnitude plot*.

The manner in which the phase shift changes with variatio in frequency is known as the *phase-angle plot*.

Obtaining the frequency response

To obtain the frequency response , consider the high frequency model of the op-amp with capacitor C at the output, taking into account the ***capacitive effect*** present

$$A_{OL}(f) = \frac{A_{OL}}{1 + j2\Pi f R_o C}$$

$$A_{OL}(f) = \frac{A_{OL}}{1 + j(\frac{f}{f_o})}$$

Where

$A_{OL}(f)$ = open loop voltage gain as a function of frequency

A_{OL} = Gain of the op-amp at 0Hz

F = operating frequency

F_o = Break frequency or cutoff frequency of op-amp

For a given op-amp and selected value of C, the frequency f_o is constant.

The above equation can be written in the polar form as

$$\left|A_{OL}(f)\right| = \frac{A_{OL}}{\sqrt{1+\left(\frac{f}{f_o}\right)^2}}$$

$$\angle A_{OL}(f) = \Phi(f) = -\tan^{-1}\left(\frac{f}{f_0}\right)$$

Frequency Response of an op-amp

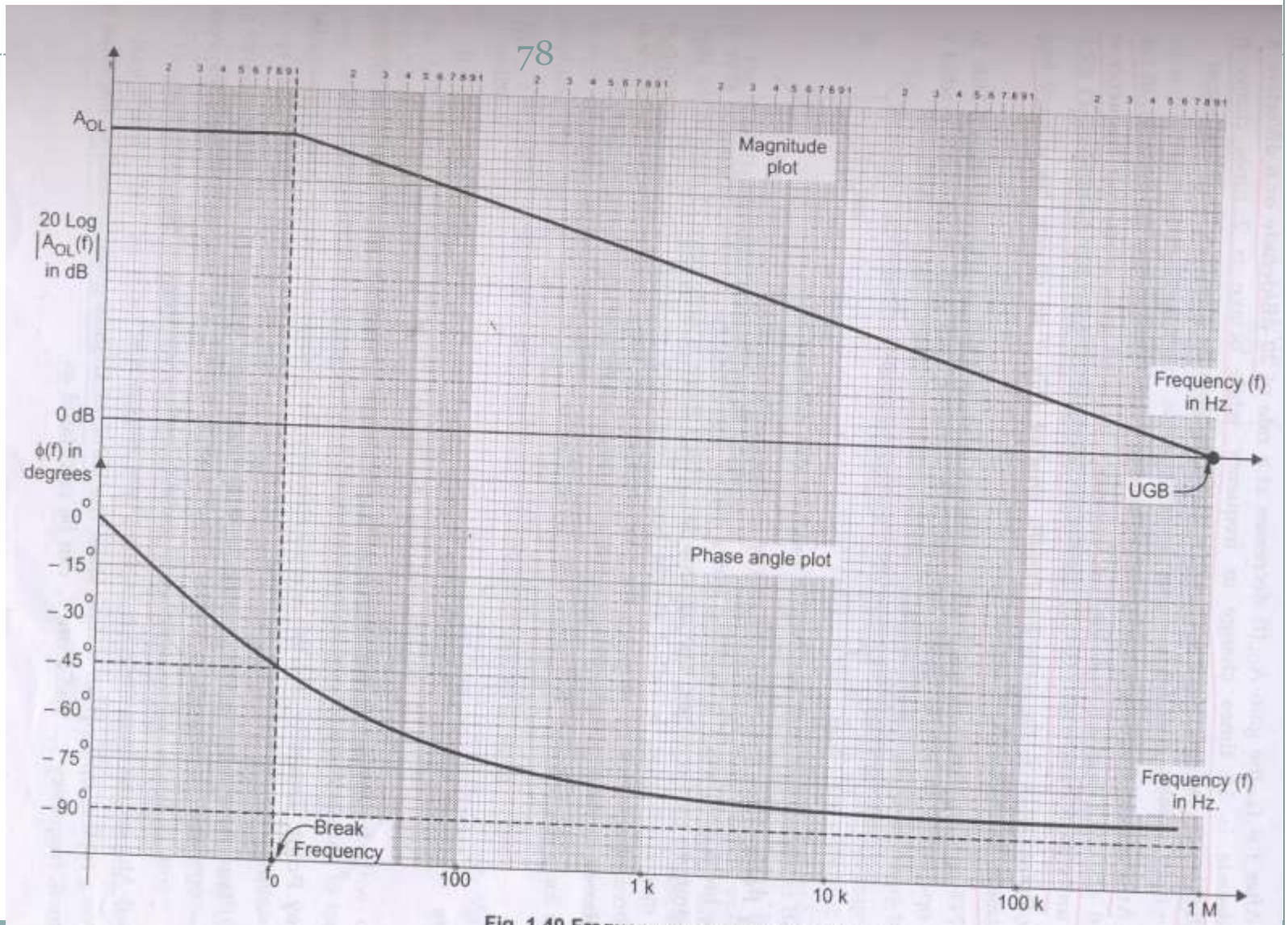


Fig. 1.49 Frequency response of an op-amp

The following observations can be made from the frequency response of an op-amp

i) The open loop gain A_{OL} is almost constant from 0 Hz to the break frequency f_o.

ii) At $f=f_o$, the gain is 3dB down from its value at 0Hz. Hence the frequency f_o is also called as -3dB frequency. It is also know as corner frequency

iii) After $f=f_o$, the gain A_{OL} (f) decreases at a rate of 20 dB/decade or 6dB/octave. As the gain decreases, slope of the magnitude plot is -20dB/decade or -6dB/octave, after $f=f_o$.

iv) At a certain frequency, the gain reduces to 0dB. This means $20\log|A_{OL}|$ is 0dB i.e. $|A_{OL}| =1$. Such a frequency is called gain cross-over frequency or unity gain bandwidth (UGB). It is also called closed loop bandwidth.

UGB is the gain bandwidth product only if an op-amp has a single break over frequency, before A_{OL} (f) dB is zero.

For an op-amp with single break frequency f_o , after f_o the gain bandwidth product is constant equal to UGB

$$UGB = A_{OL} \; f_o$$

UGB is also called gain bandwidth product and denoted as f_t

Thus f_t is the product of gain of op-amp and bandwidth.

The break frequency is nothing but a corner frequency f_o . At this frequency, slope of the magnitude plot changes. The op-amp for which there is only once change in the slope of the magnitude plot, is called single break frequency op-amp.

For a single break frequency we can also write

$$\mathbf{UGB = A_f \ f_f}$$

A_f = closed loop voltage gain

F_f = bandwidth with feedback

v) The phase angle of an op-amp with single break frequency varies between 0^0 to 90^0 . The maximum possible phase shift is -90^0 , i.e. output voltage lags input voltage by 90^0 when phase shift is maximum

vi) At a corner frequency $f=f_o$, the phase shift is $-45^{0.}$

$$\mathbf{F_o = UGB / A_{OL}}$$

Frequency f in Hz	$\lvert A_{OL}(f) \rvert$ in dB = $20 \log \frac{A_{OL}}{\sqrt{1+\left(\frac{f}{f_o}\right)^2}}$ in dB	$\phi(f) = -\tan^{-1}\left(\frac{f}{f_o}\right)$ in degrees
0	106.02 dB	0°
5	103.01 dB	– 45°
10	99.03 dB	– 63.43°
100	79.98 dB	– 87.13°
1000	60.00 dB	– 89.71°
100×10^3	20.00 dB	– 89.99°
1×10^6	0 dB	– 89.999°

Table 1.6

The modes of using an op-amp

- ***Open Loop*** : (The output assumes one of the two possible output states, that is $+V_{sat}$ or $-V_{sat}$ and the amplifier acts as a switch only).
- ***Closed Loop*:** (The utility of an op-amp can be greatly increased by providing negative feed back. The output in this case is not driven into saturation and the circuit behaves in a linear manner).

Open loop configuration of op-amp

- The voltage transfer curve indicates the inability of op-amp to work as a linear small signal amplifier in the open loop mode
- Such an open loop behaviour of the op-amp finds some rare applications like voltage comparator, zero crossing detector etc.

Open loop op-amp configurations

- The configuration in which output depends on input, but output has no effect on the input is called open loop configuration.
- No feed back from output to input is used in such configuration.
- The opamp works as high gain amplifier
- The op-amp can be used in three modes in open loop configuration they are

1. Differential amplifier
2. Inverting amplifier
3. Non inverting amplifier

Differential Amplifier

The amplifier which amplifies the difference between the two input voltages is called differential amplifier.

$$V_o = A_{OL} V_d = A_{OL}(V_1 - V_2) = A_{OL}(V_{in1} - V_{in2})$$

Key point: For very small V_d , output gets driven into saturation due to high A_{OL} , hence this application is applicable for very small range of differential input voltage.

Inverting Amplifier

The amplifier in which the output is inverted i.e. having 180° phase shift with respect to the input is called an inverting amplifier

$$V_o = -A_{OL} V_{in2}$$

Keypoint: The negative sign indicates that there is phase shift of 180° between input and output i.e. output is inverted with respect to input.

Non-inverting Amplifier

The amplifier in which the output is amplified without any phase shift in between input and output is called non inverting amplifier

$$V_o = A_{OL} V_{in1}$$

Keypoint: The positive output shows that input and output are in phase and input is amplified A_{OL} times to get the output.

Why op-amp is generally not used in open loop mode?

As open loop gain of op-amp is very large, very small input voltage drives the op-amp voltage to the saturation level. Thus in open loop configuration, the output is at its positive saturation voltage ($+V_{sat}$) or negative saturation voltage ($-V_{sat}$) depending on which input V_1 or V_2 is more than the other. For a.c. input voltages, output may switch between positive and negative saturation voltages

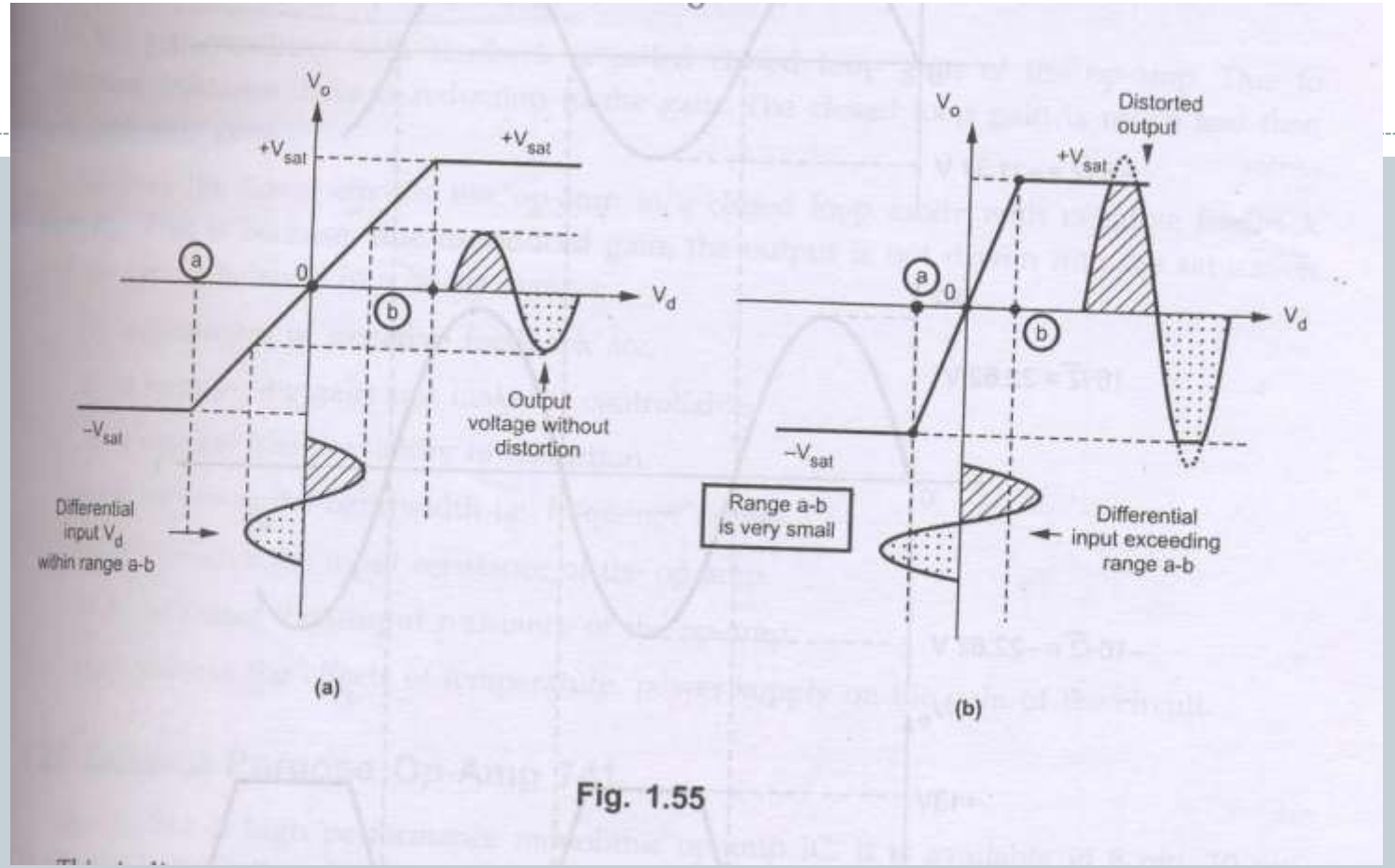


Fig. 1.55

This indicates the inability of op-amp to work as a linear small signal amplifier in the open loop mode. Hence the op-amp in open loop configuration is not used for the linear applications

General purpose op-amp 741

The IC 741 is high performance monolithic op-amp IC.

It is available in 8pin, 10pin or 14pin configuration.

It can operate over a temperature of -55° C to 125° C.

Features:

i) No frequency compensation required

ii) Short circuit protection provided

iii) Offset Voltage null capability

iv) Large common mode and differential voltage range

v) No latch up

Internal schematic of 741 op-amp

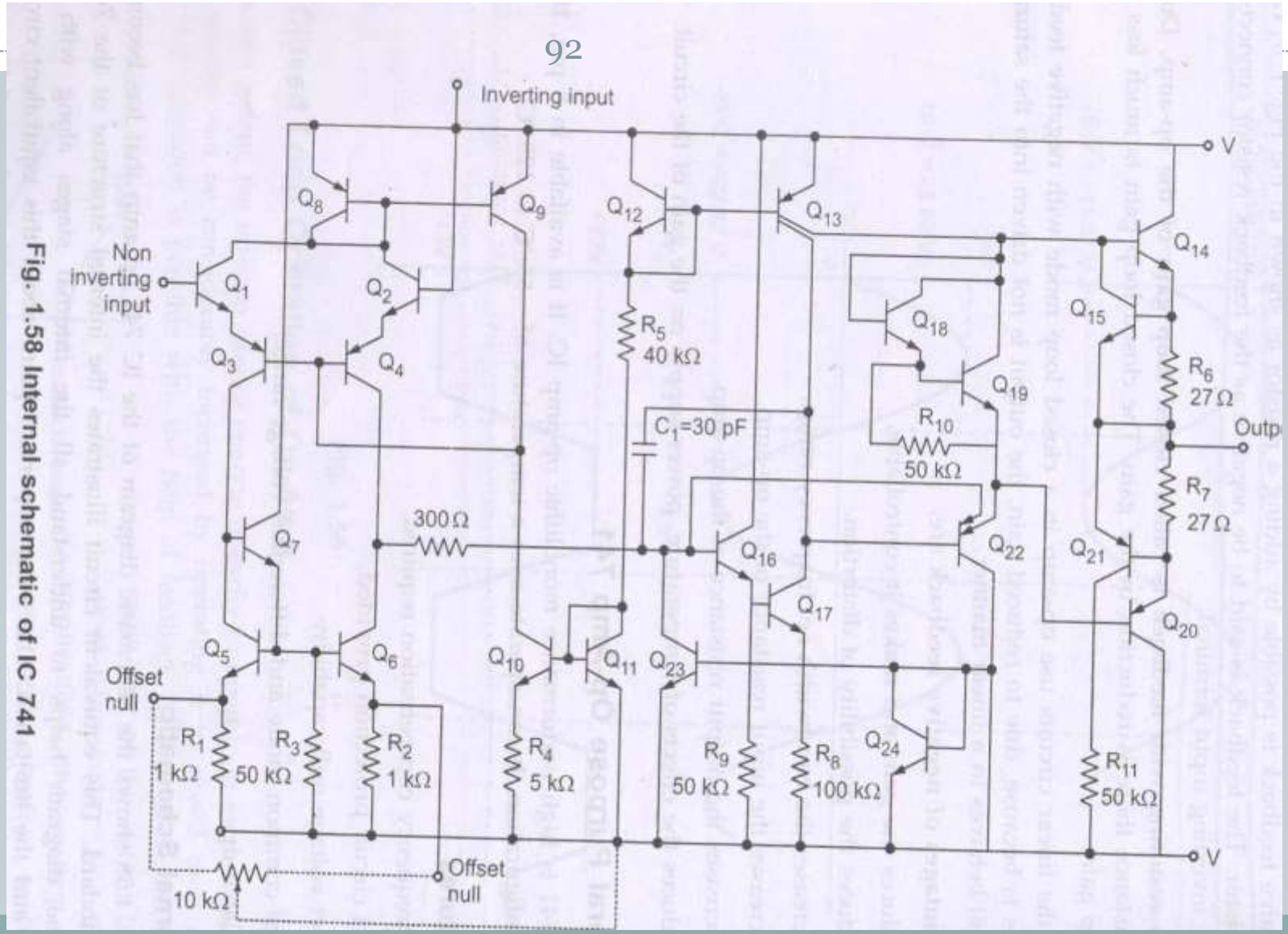


Fig. 1.58 Internal schematic of IC 741

Realistic simplifying assumptions

- Zero input current: The current drawn by either of the input terminals (inverting and non-inverting) is zero

- Virtual ground :This means the differential input voltage V_d between the non-inverting and inverting terminals is essentially zero. (The voltage at the non inverting input terminal of an op-amp can be realistically assumed to be equal to the voltage at the inverting input terminal

Closed loop operation of op-amp

The utility of the op-amp can be increased considerably by operating in closed loop mode. The closed loop operation is possible with the help of feedback. The feedback allows to feed some part of the output back to the input terminals. In the linear applications, the op-amp is always used with negative feedback. The negative feedback helps in controlling gain, which otherwise drives the op-amp out of its linear range, even for a small noise voltage at the input terminals

Ideal Inverting Amplifier

1. The output is inverted with respect to input, which is indicated by minus sign.
2. The voltage gain is independent of open loop gain of the op-amp, which is assumed to be large.
3. The voltage gain depends on the ratio of the two resistances. Hence selecting R_f and R_1 , the required value of gain can be easily obtained.
4. If $R_f > R_1$, the gain is greater than 1

   If $R_f < R_1$, the gain is less than 1

   If $R_f = R_1$, the gain is unity

Thus the output voltage can be greater than, less than or equal to the input voltage in magnitude

5. If the ratio of R_f and R_1 is K which is other than one, the circuit is called scale changer while for $R_f/R_1 = 1$ it is called phase inverter.
6. The closed loop gain is denoted as A_{VF} or A_{CL} i.e. gain with feedback

Ideal Non-inverting Amplifier

1. The voltage gain is always greater than one
2. The voltage gain is positive indicating that for a.c. input, the output and input are in phase while for d.c. input, the output polarity is same as that of input
3. The voltage gain is independent of open loop gain of op-amp, but depends only on the two resistance values
4. The desired voltage gain can be obtained by selecting proper values of R_f and R_1

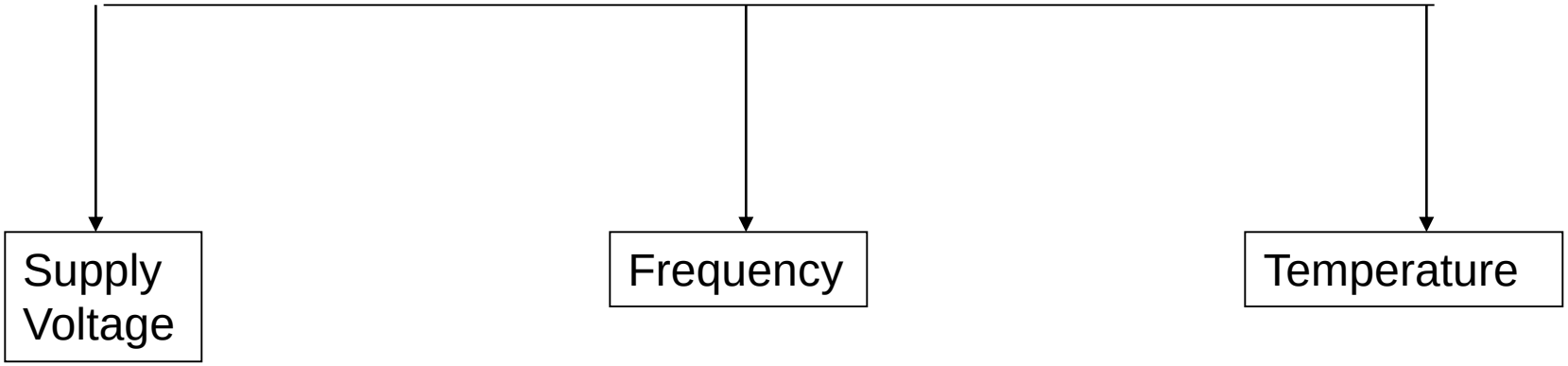
Comparison of the ideal inverting and non-inverting op-amp

Ideal Inverting amplifier	Ideal non-inverting amplifier
1. Voltage gain=$-R_f/R_1$	1. Voltage gain=$1+R_f/R_1$
2. The output is inverted with respect to input	2. No phase shift between input and output
3. The voltage gain can be adjusted as greater than, equal to or less than one	3. The voltage gain is always greater than one
4. The input impedance is R_1	4. The input impedance is very large

Parameter consideration for various applications

For A.C. applications	For D.C. applications
Input resistance	Input resistance
Output resistance	Output resistance
Open loop voltage gain	Open loop voltage gain
Slew rate	Input offset voltage
Output voltage swing	Input offset current
Gain- bandwidth product	Input offset voltage and current drifts
Input noise voltage and current	
Input offset voltage and current drifts	

Factors affecting parameters of Op-amp



1. Voltage gain
2. Output Voltage swing
3. Input voltage range
4. Power consumption
5. Input offset current

1. Voltage gain
2. Input resistance
3. Output resistance
4. CMRR
5. Input noise voltage
6. Input noise current

1. Input offset current
2. Input offset voltage
3. Input bias current
4. Power consumption
5. Gain-Bandwidth product
6. Slew rate
7. Input resistance

Practical Inverting Amplifier

Closed Loop Voltage gain =

$$A_{CL} = -\frac{A_{OL} R_f}{R_1 + R_f + R_1 A_{OL}}$$

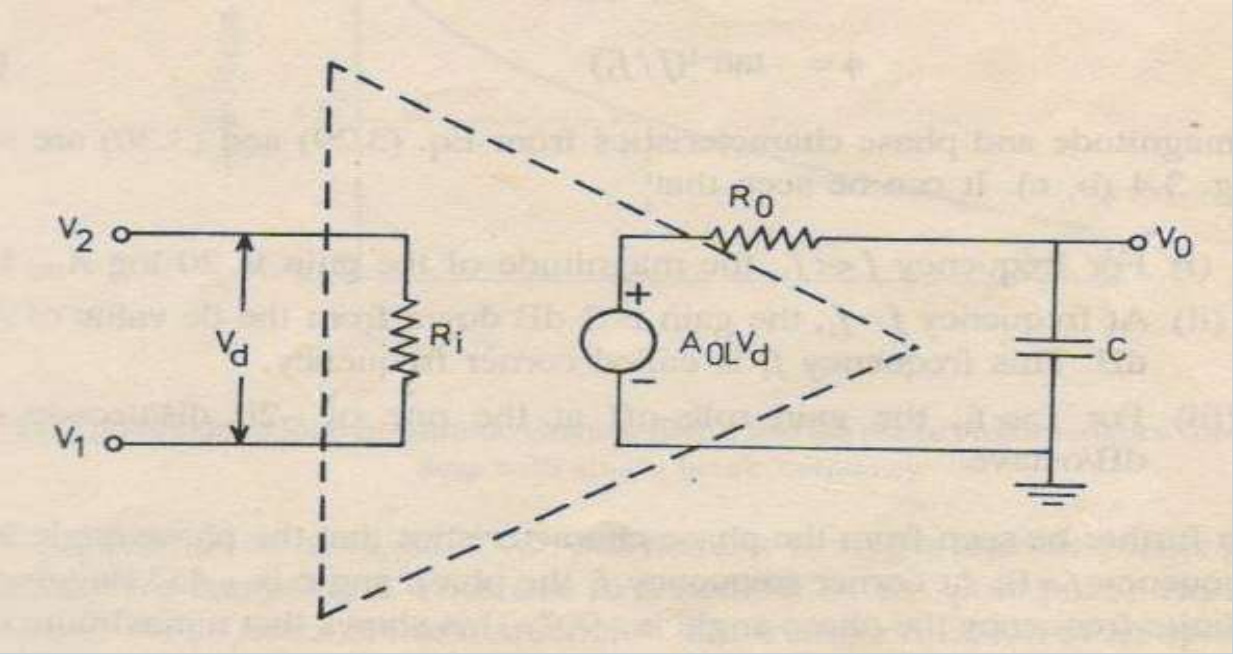
Practical Non-Inverting Amplifier

Closed Loop Voltage gain =

$$A_{CL} = \frac{A_{OL}(R_1 + R_f)}{R_1 + R_f + R_1 A_{OL}}$$

AC characteristics

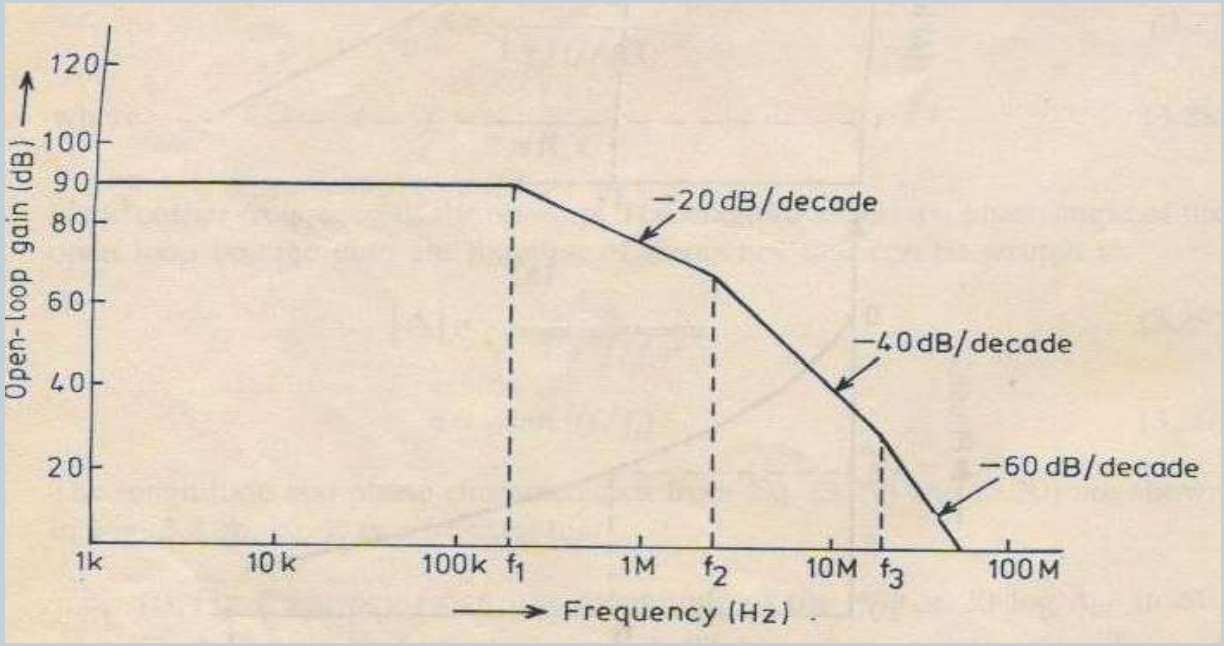
Frequency Response



HIGH FREQUENCY MODEL OF OPAMP

AC characteristics

Frequency Response



OPEN LOOP GAIN VS FREQUENCY

Need for frequency compensation in practical op-amps

- Frequency compensation is needed when large bandwidth and lower closed loop gain is desired.
- Compensating networks are used to control the phase shift and hence to improve the stability

Frequency compensation methods

- Dominant- pole compensation
- Pole- zero compensation

Slew Rate

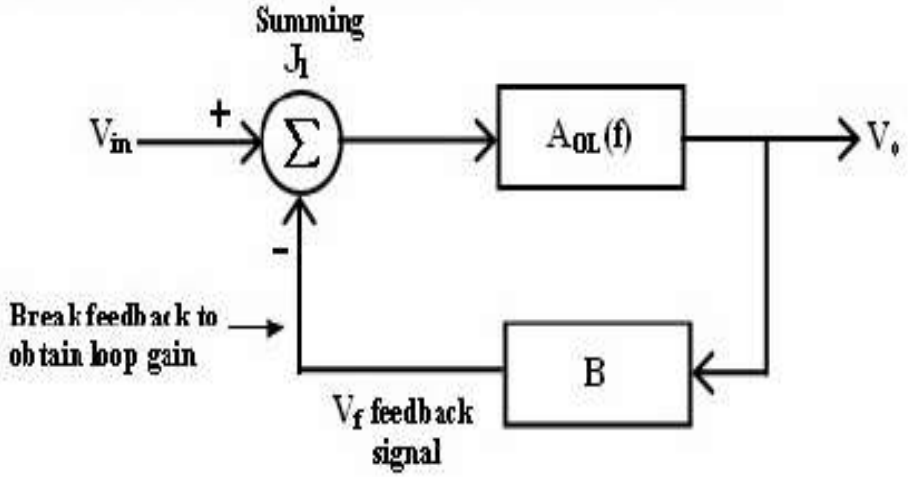
- The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage.

- An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage

Circuit Stability:

A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. (or) A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable sys keeps on increasing until the system break down. The unstable system are impractical and need be made stable. The criterian gn for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability , ex: Bode plots.

Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram.



The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred "Transfer frequency' From fig we represented it by $A_{OL}(f)$ which is given by

$A_{OL}(f) = V_0/Vin$ if $V_f = 0$. -----(1)

where $A_{OL}(f)$ = open loop volt gain. The closed loop gain A_f is given by

$A_F = V_0/Vin$

$A_F = A_{OL} / (1+(A_{OL})(B)$ ----(2)

B = gain of feedback circuit.

B is a constant if the feedback circuit uses only resistive components. Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

1. Method:1:

Determine the phase angle when the magnitude of $(A_{OL})(B)$ is 0dB (or) 1. If phase angle is $> .-180^0$, the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

2. Method 2:

Determine the phase angle when the magnitude of (A_{OL}) (B) is 0dB (or) 1. If phase angle is > .-180^0 , If the magnitude is –ve decibels then the system is stable. However, the some systems the phase angle of a system may reach -180^0 , under such conditions method 1 must be used to determine the system stability.

UNIT-III
OP AMP APPLICATIONS -1

IMPORTANT POINTS

- The amplifier output voltage does not depend on the “load” (what is attached to the output).
- The “form” of the output voltage (the signs of the scaling factors on the input voltages, for example) depends on the amplifier circuit layout.

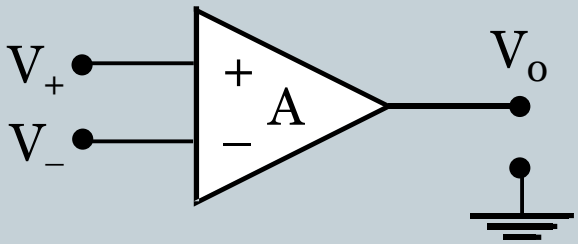
  To change the values (magnitudes) of scaling factors, adjust resistor values.
- Input voltages which are attached to the + (non-inverting) amplifier terminal get positive scaling factors.

  Inputs attached to the – (inverting) terminal get negative scaling factors.
- You can use these last two principles to design amplifiers which perform a particular function on the input voltages.

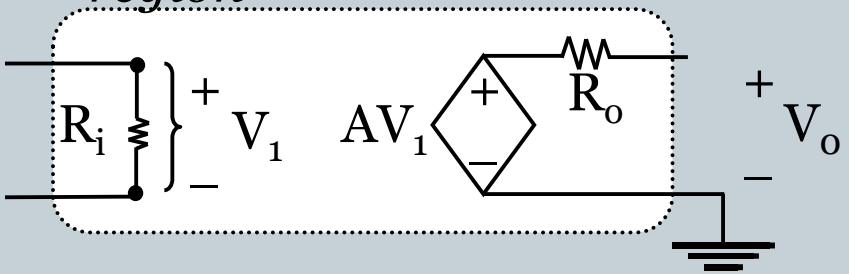
DIFFERENTIAL AMPLIFIER

Differential Amplifier

$V_0 = A(V_+ - V_-)$

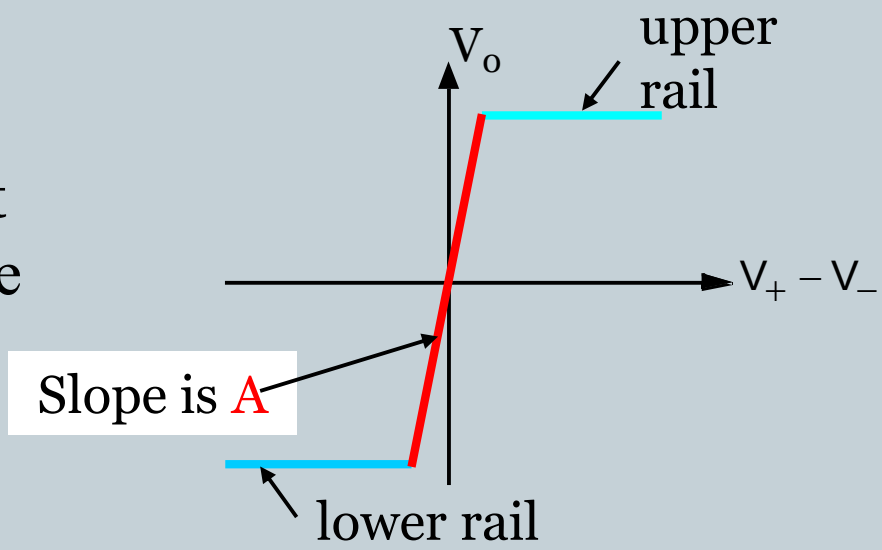


Circuit Model *in linear region*



"Differential" $\Rightarrow V_o$ depends only on difference $(V_+ - V_-)$

The output cannot be larger than the supply voltages, which are not shown. It will limit or "clip" if we attempt to go too far. We call the limits of the output the "**rails**".



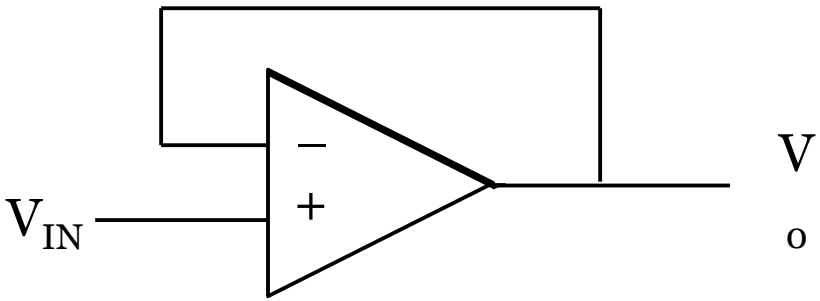
Can add negative feedback to perform an "operation" on input voltages (addition, integration, etc.): operational amplifier

AMPLIFIER ANALYSIS USING CIRCUIT MODEL

To analyze an amplifier circuit, you can replace the amplifier with the circuit model, then make sure the output is within "rails".

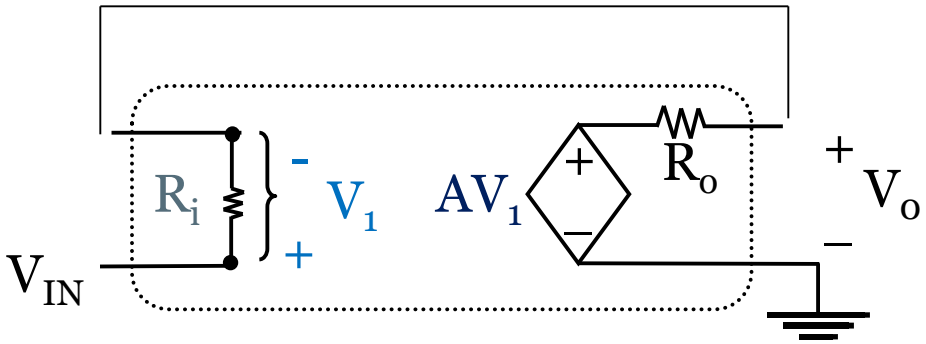
$$\frac{V_o - AV_1}{R_o} = \frac{V_1}{R_i}$$

Example: Voltage Follower



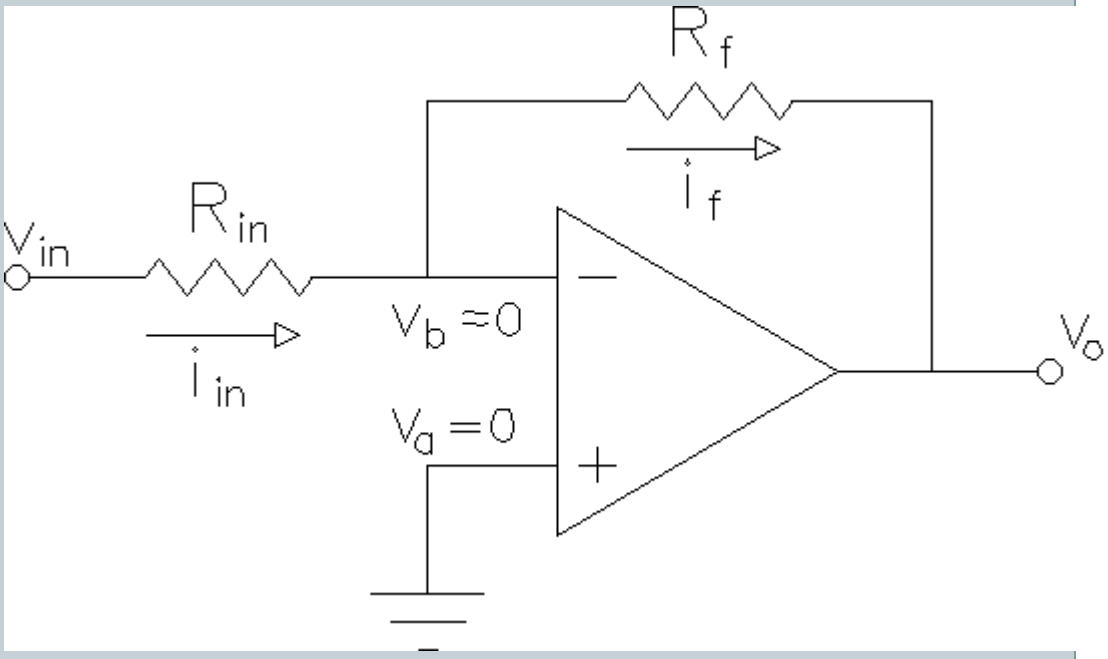
$$V_1 = V_{IN} - V_o$$

Circuit Model in linear region



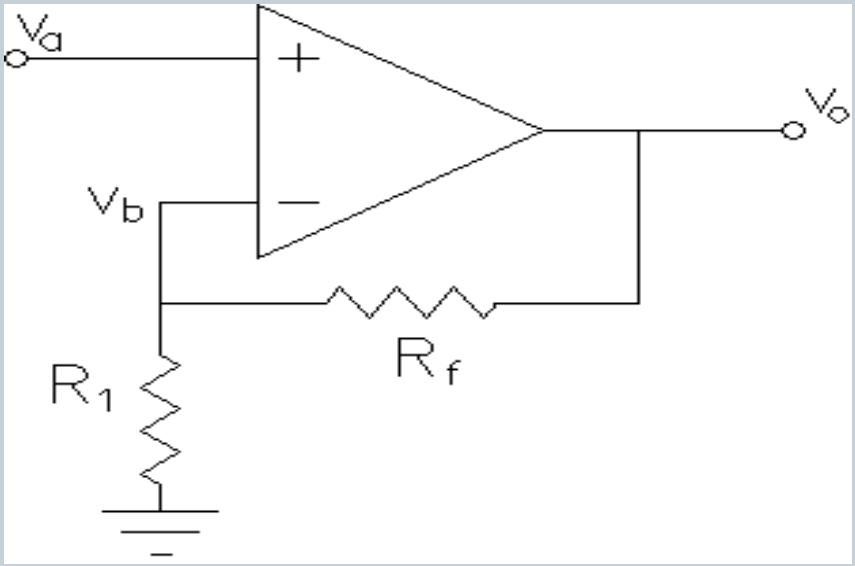
$$V_o = \frac{AR_i + R_o}{(A+1)R_i + R_o} V_{IN}$$

Inverting Op-Amp



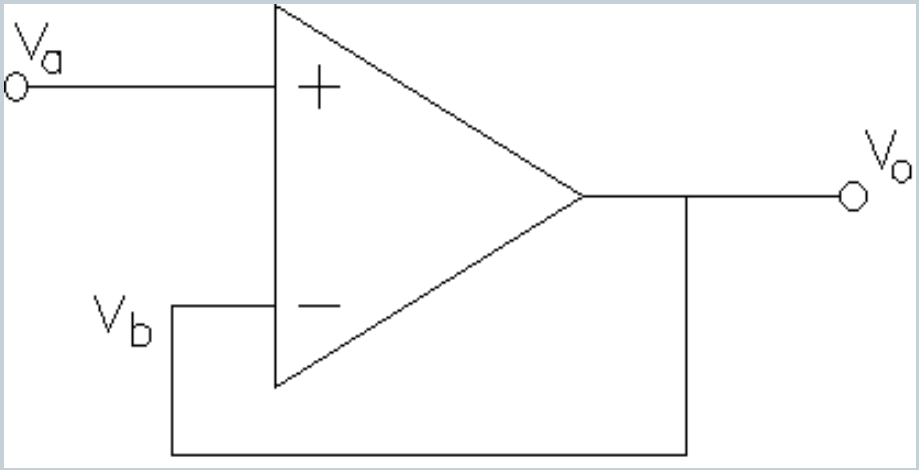
$$V_{OUT} = -V_{IN}\frac{R_f}{R_1}$$

Non-Inverting Amplifier



$$V_{OUT} = V_{IN}\left(1 + \frac{R_1}{R_2}\right)$$

Voltage follower

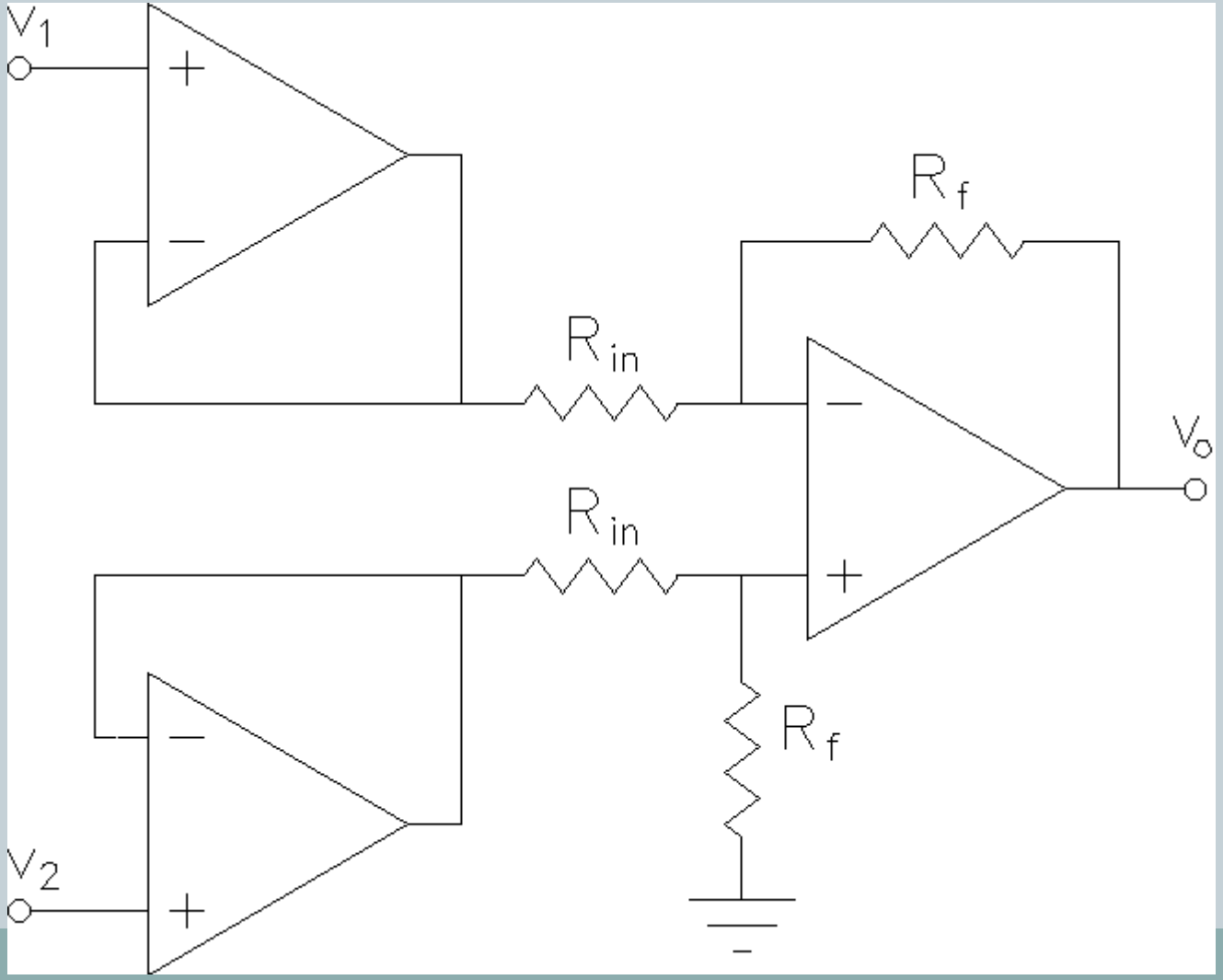


$$V_{OUT} = V_{IN}$$

Instrumentation Amplifier

In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier

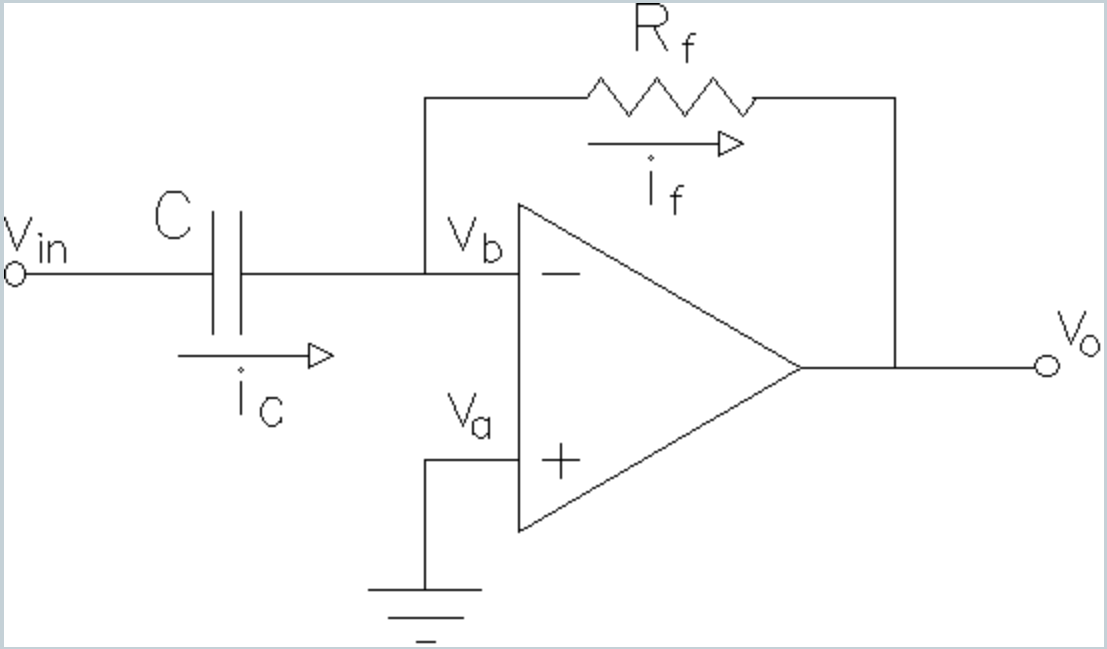
Instrumentation Amplifier



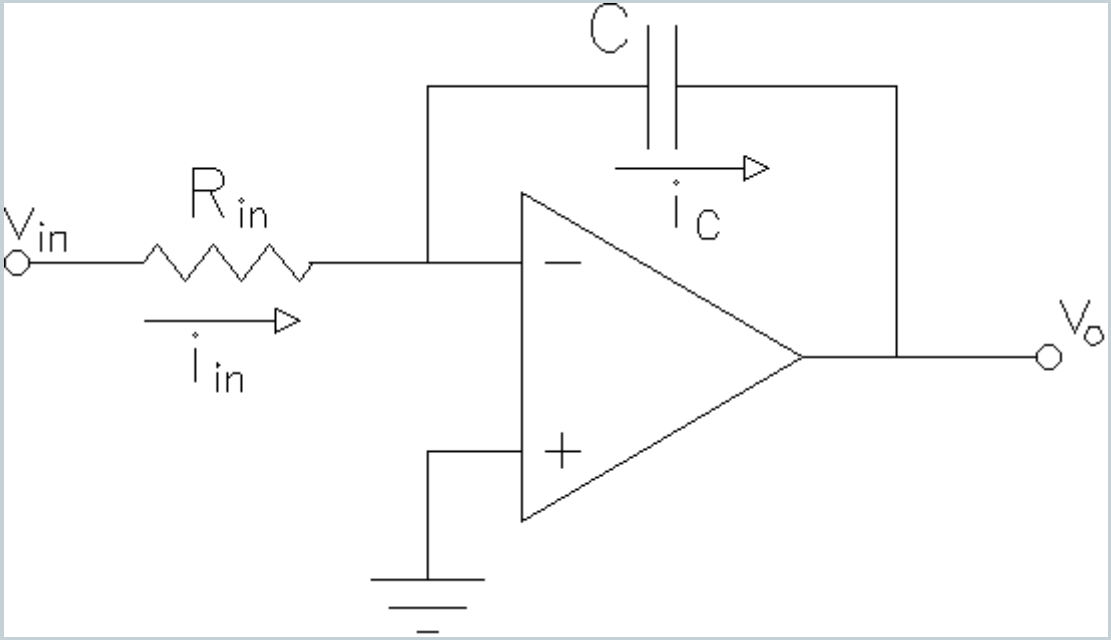
Features of instrumentation amplifier

1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature co-efficient
4. low dc offset
5. low output impedance

Differentiator

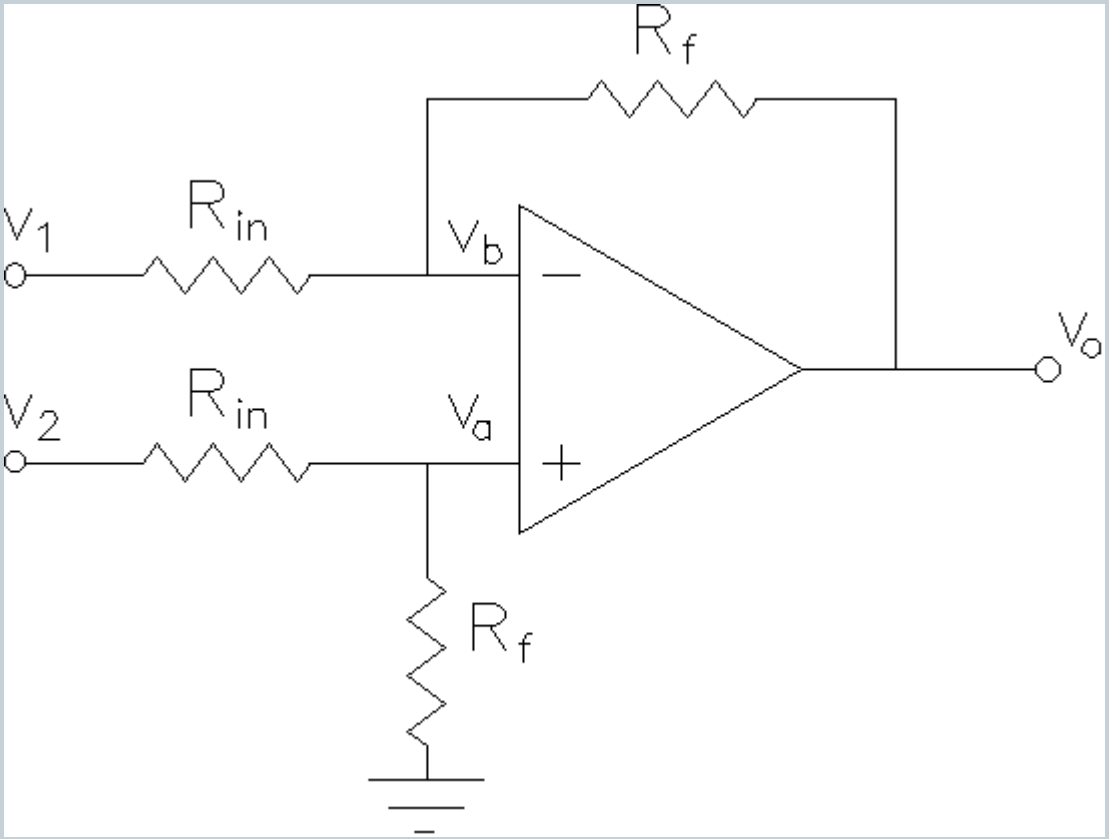


Integrator



$$V_o(t) = -\frac{1}{RC}\int_0^t V_{IN}(T)\,dT + V_C(0)$$

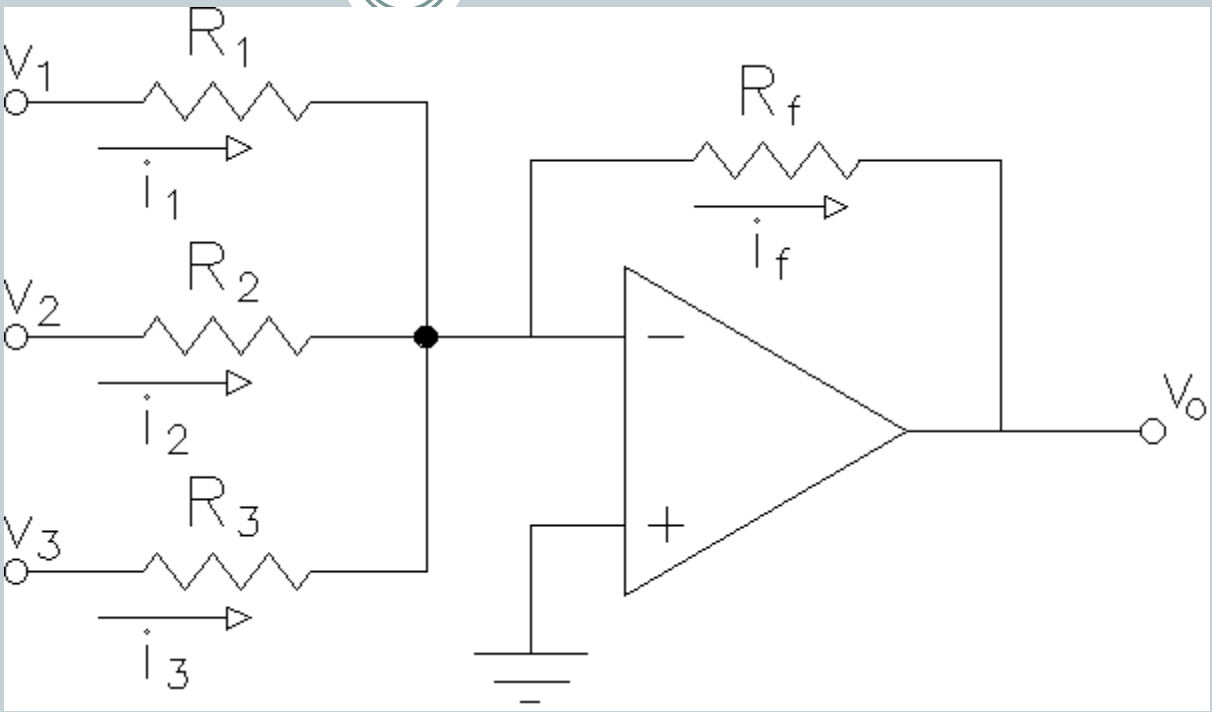
Differential amplifier



Differential amplifier

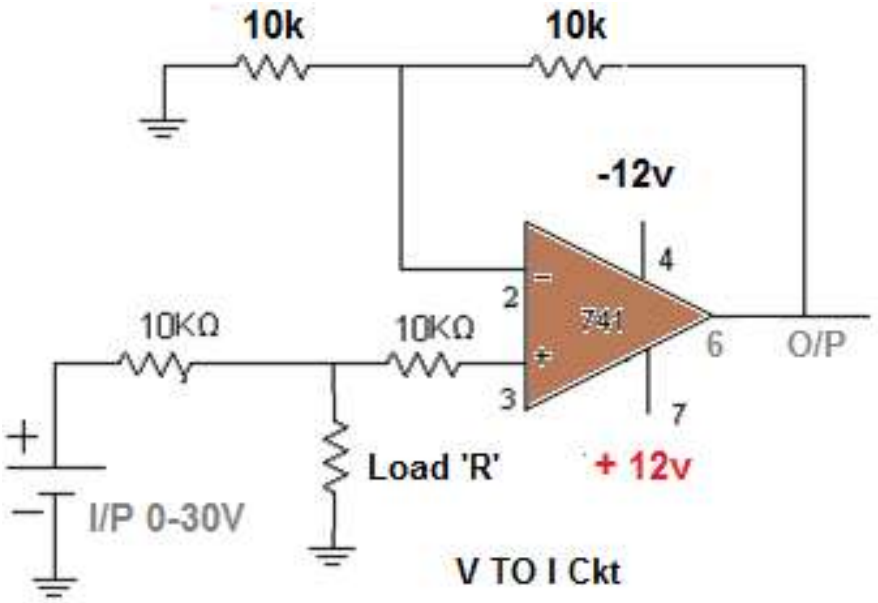
This circuit amplifies only the difference between the two inputs. In this circuit there are two resistors labeled R_{IN} Which means that their values are equal. The differential amplifier amplifies the difference of two inputs while the differentiator amplifies the slope of an input

Summer



$$V_0 = -\frac{R_F}{R_1}V_1 - \frac{R_F}{R_2}V_2 - \frac{R_F}{R_3}V_3$$

VOLTAGE-TO-CURRENT CONVERTER



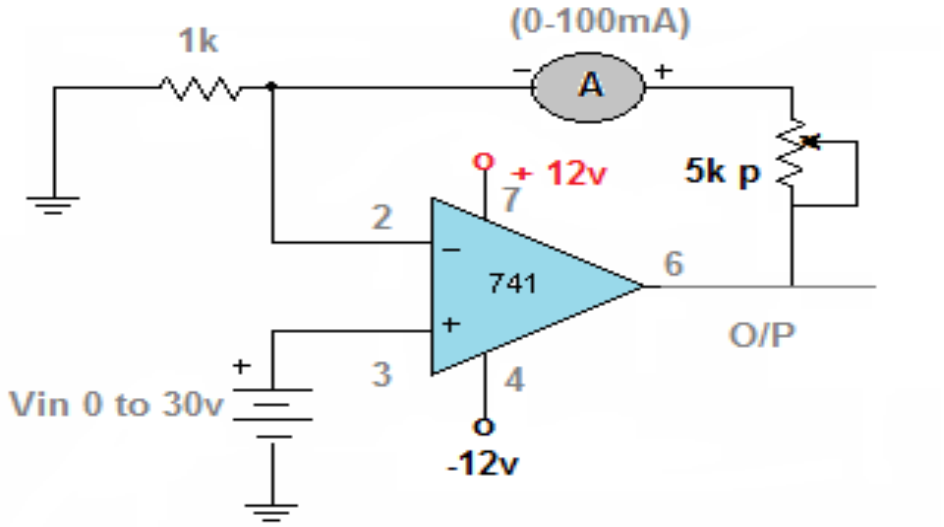
Formula: Floating load:- V – I converter.

$V_{in} = V_{id} + V_f$ where V_{id} is input difference voltage and V_f is the feedback voltage

But $V_{id} = 0$

$V_{in} = V_f = R_1 R_L$

$I_L = V_{in}/R_L$



Formula: Ground load V – I converter.

$I_1+I_2=I_L$

$(V_{in}-V_1)/R+(V_o-V_1)/R=I_L$

$V_{in}+V_o-2V_i=I_LR$

Since op-amp is non inverting

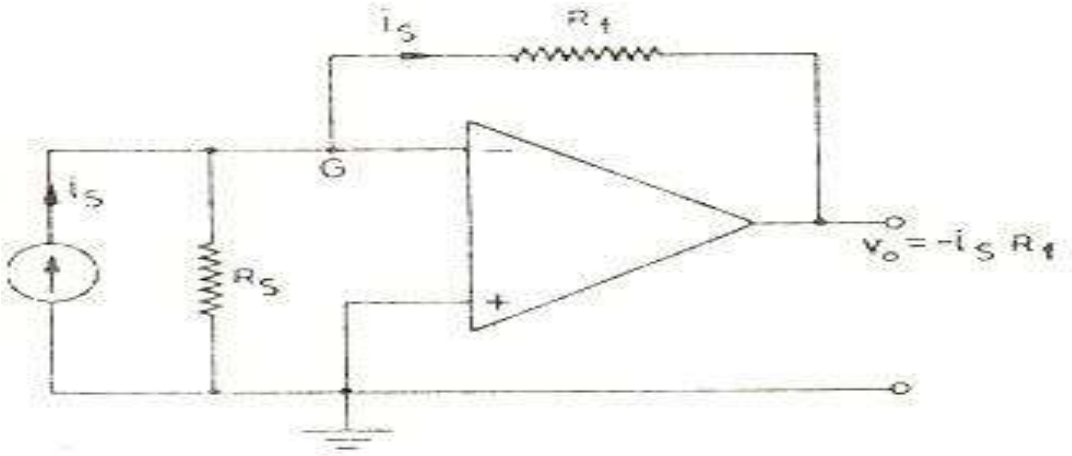
Gain=1+(R/R)=2

Vo=2Vi

V_{in}=Vo-Vo+I_LR

$I_L=V_{in}/R$

CURRENT-TO-VOLTAGE CONVERTER



$$V_o = -i_s R_f$$

Filter

Filter is a frequency selective circuit that passes signal of specified Band of frequencies and attenuates the signals of frequencies outside the band

Type of Filter

1. Passive filters
2. Active filters

Passive filters

Passive filters works well for high frequencies. But at audio frequencies, the inductors become problematic, as they become large, heavy and expensive.For low frequency applications, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance ie, low Q, resulting in high power dissipation

Active filters

Active filters used op- amp as the active element and resistors and capacitors as passive elements. By enclosing a capacitor in the feed back loop , inductor less active filters can be obtained

Some commonly used active filters

1. Low pass filter
2. High pass filter
3. Band pass filter
4. Band reject filter

Active Filters

- Active filters use op-amp(s) and RC components.
- Advantages over passive filters:
  - op-amp(s) provide gain and overcome circuit losses
  - increase input impedance to minimize circuit loading
  - higher output power
  - sharp cutoff characteristics can be produced simply and efficiently without bulky inductors
- Single-chip universal filters (e.g. switched-capacitor ones) are available that can be configured for any type of filter or response.

Review of Filter Types & Responses

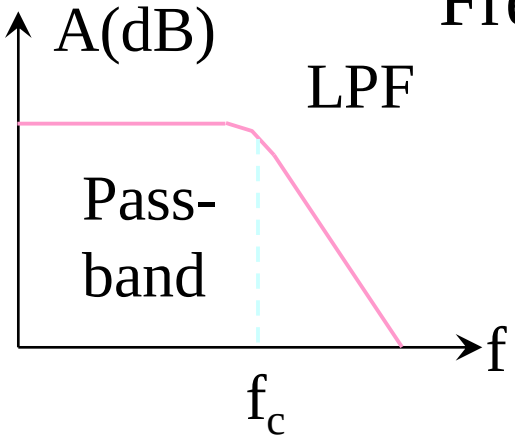
- 4 major types of filters: low-pass, high-pass, band pass, and band-reject or band-stop
- 0 dB attenuation in the pass band (usually)
- 3 dB attenuation at the *critical* or *cutoff frequency*, f_c (for Butterworth filter)
- Roll-off at 20 dB/dec (or 6 dB/oct) per *pole* outside the passband (# of poles = # of reactive elements). Attenuation at any frequency, f, is:

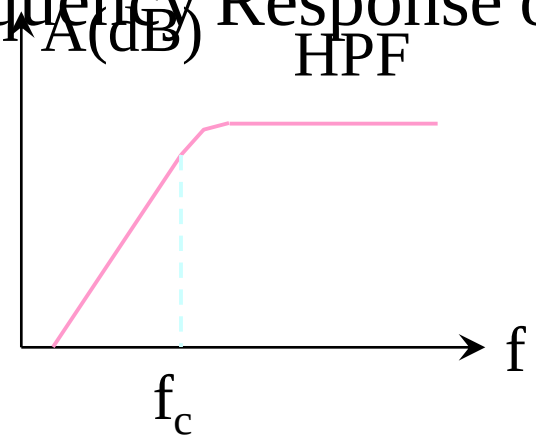
$$atten.(dB)\,at\ f = \log\left(\frac{f}{f_c}\right) x\, atten.(dB)\,at\ f_{dec}$$

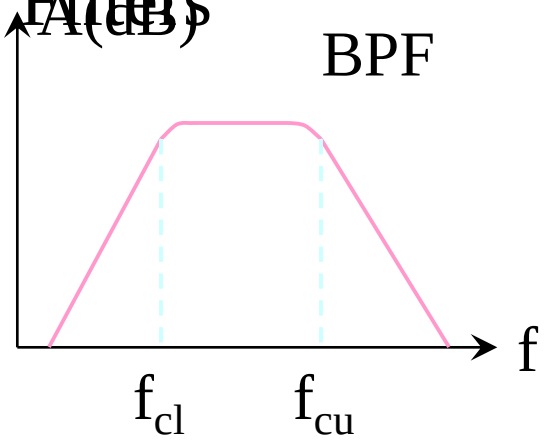
Review of Filters (cont'd)

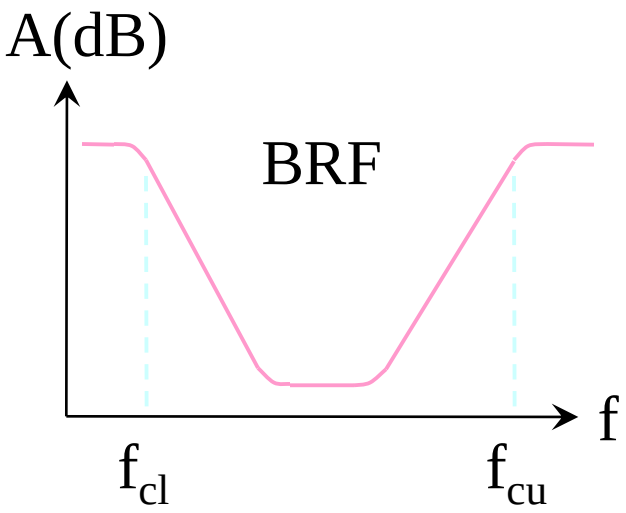
- Bandwidth of a filter: BW = f_{cu} - f_{cl}
- Phase shift: 45°/pole at f_c; 90°/pole at >> f_c
- 4 types of filter responses are commonly used:
  - Butterworth - maximally flat in passband; highly non-linear phase response with frequency
  - Bessel - gentle roll-off; linear phase shift with freq.
  - Chebyshev - steep initial roll-off with ripples in passband
  - Cauer (or elliptic) - steepest roll-off of the four types but has ripples in the passband and in the stop band

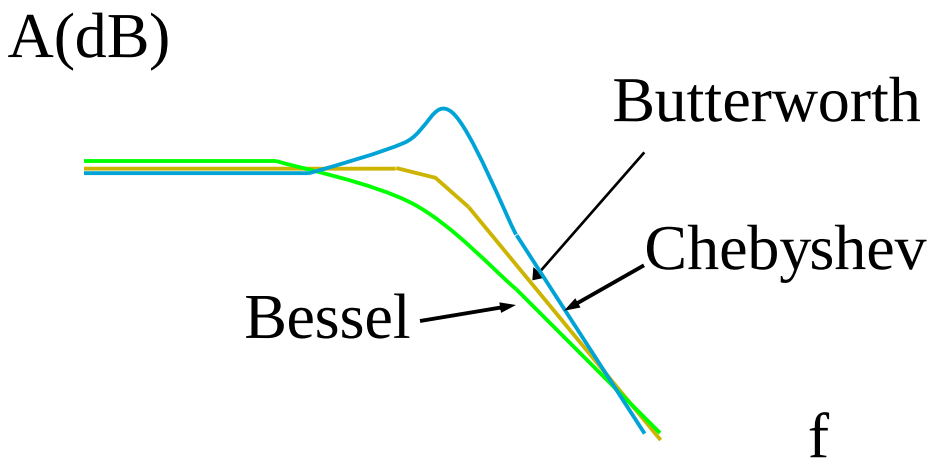
Frequency Response of Filters



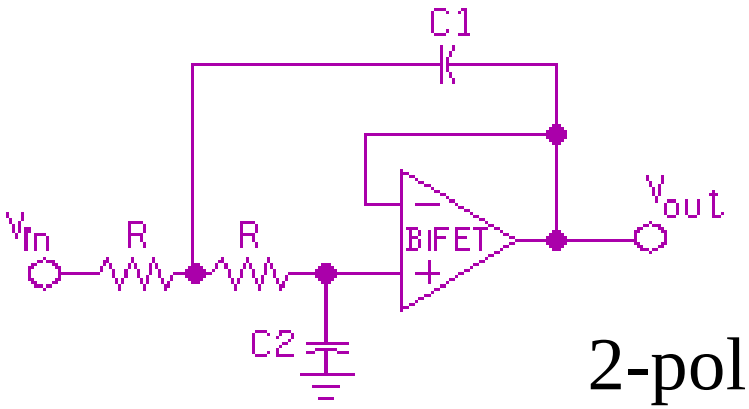




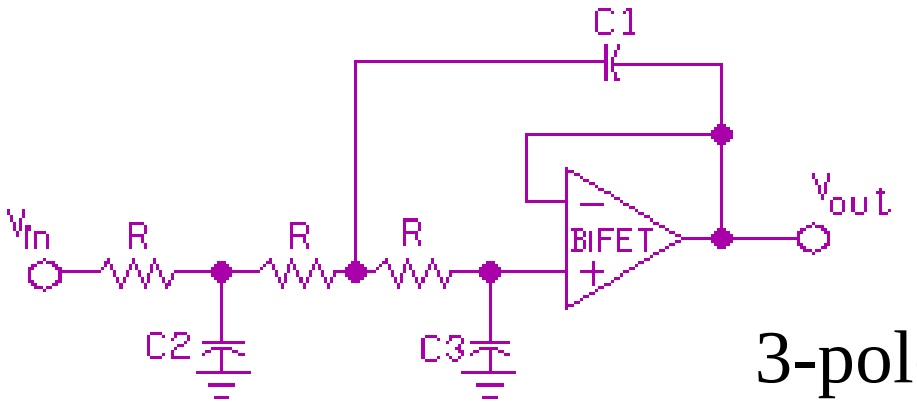




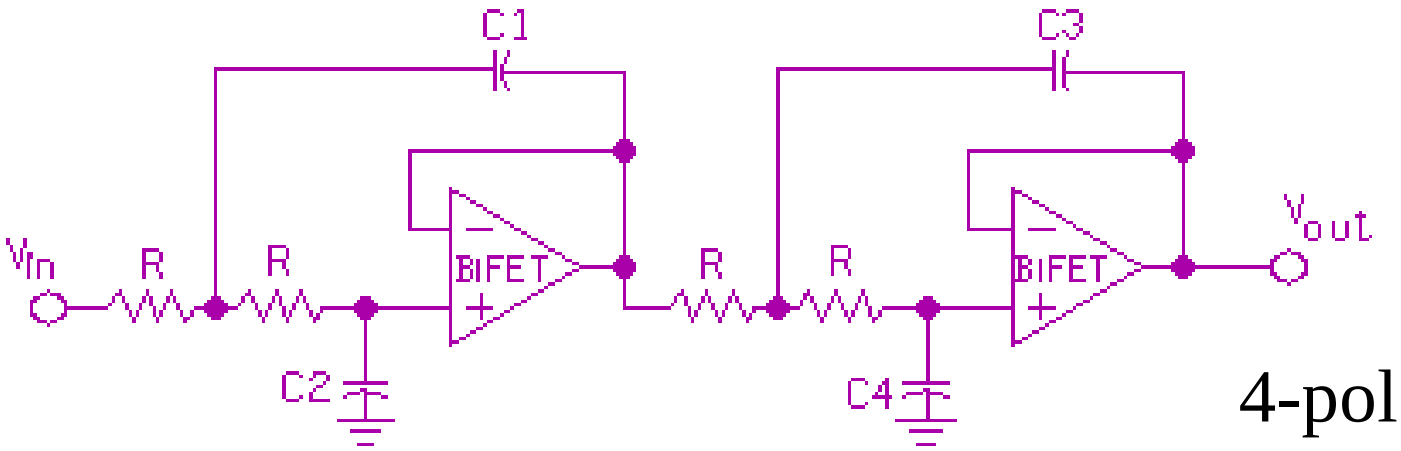
Unity-Gain Low-Pass Filter Circuits



2-pole



3-pole



4-pole

Design Procedure for Unity-Gain LPF

- Determine/select number of poles required.
- Calculate the frequency scaling constant, $K_f = 2pf$
- Divide normalized C values (from table) by K_f to obtain frequency-scaled C values.
- Select a desired value for one of the frequency-scaled C values and calculate the impedance scaling factor:

$$K_x = \frac{frequency - scaled\ C\ value}{desired\ C\ value}$$

  - Divide all frequency-scaled C values by K_x
  - Set $R = K_x W$

An Example

Design a unity-gain LP Butterworth filter with a critical frequency of 5 kHz and an attenuation of at least 38 dB at 15 kHz.

The attenuation at 15 kHz is 38 dB

⑧ the attenuation at 1 decade (50 kHz) = 79.64 dB.

We require a filter with a roll-off of at least 4 poles.

K_f = 31,416 rad/s. Let's pick C_1 = 0.01 mF (or 10 nF). Then

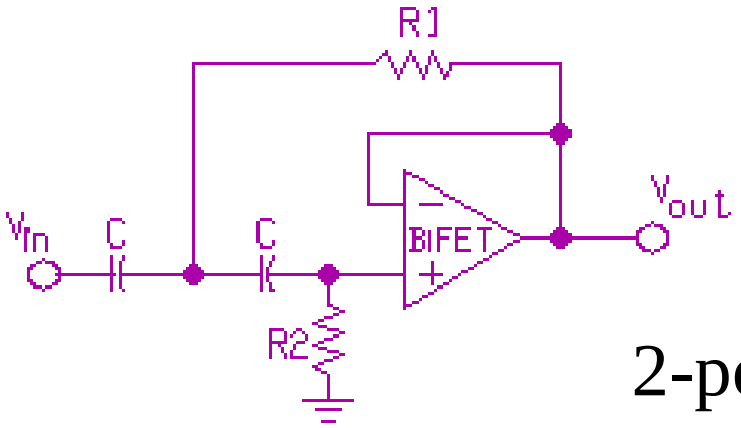
C_2 = 8.54 nF, C_3 = 24.15 nF, and C_4 = 3.53 nF.

Pick standard values of 8.2 nF, 22 nF, and 3.3 nF.

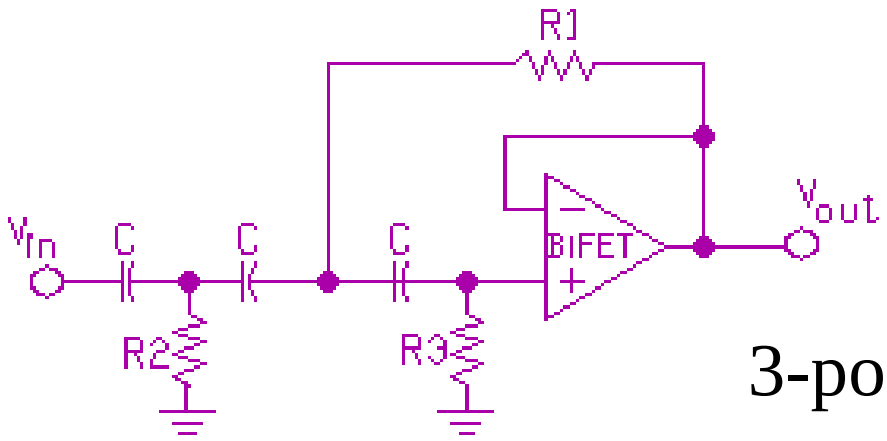
K_x = 3,444

Make all R = 3.6 kW (standard value)

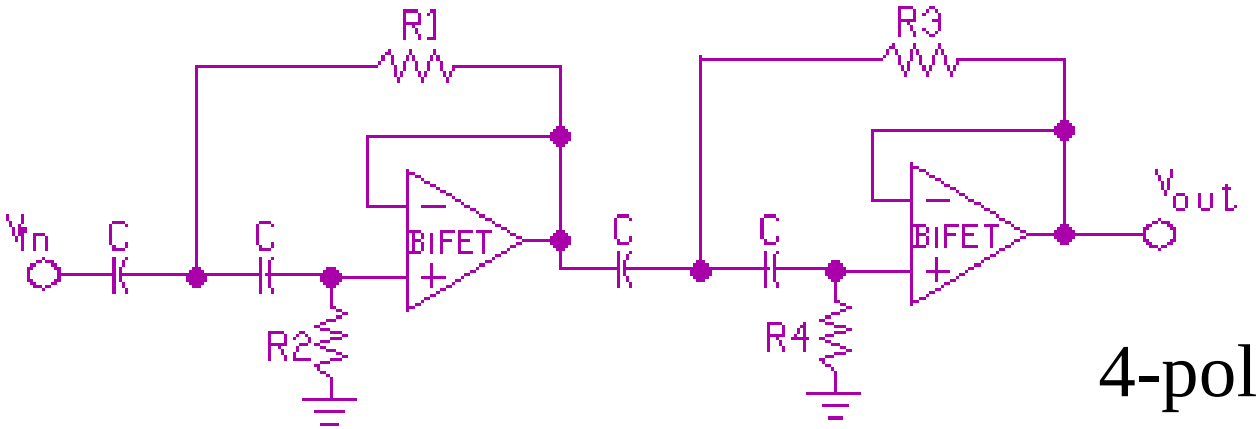
Unity-Gain High-Pass Filter Circuits



2-pole



3-pole



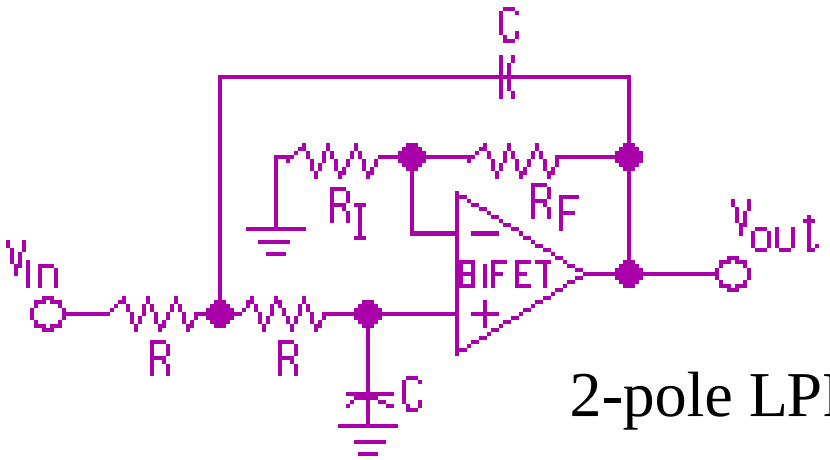
4-pole

Design Procedure for Unity-Gain HPF

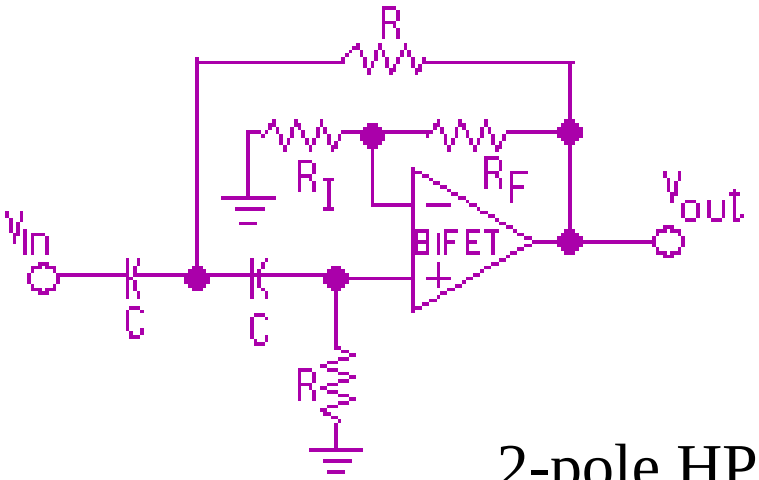
- The same procedure as for LP filters is used except for step #3, the normalized C value of 1 F is divided by K_f. Then pick a desired value for C, such as 0.001 mF to 0.1 mF, to calculate K_x. (Note that all capacitors have the same value).
- For step #6, multiply all normalized R values (from table) by K_x.

E.g. Design a unity-gain Butterworth HPF with a critical frequency of 1 kHz, and a roll-off of 55 dB/dec. (Ans.: C = 0.01 mF, R_1 = 4.49 kW, R_2 = 11.43 kW, R_3 = 78.64 kW.; pick standard values of 4.3 kW, 11 kW, and 75 kW).

Equal-Component Filter Design



2-pole LPF



2-pole HPF

Same value R & same value C are used in filter.

Select C (e.g. 0.01 mF), then:

A_v for # of poles is given in a table and is the same for LP and HP filter design.

$$A_v = \frac{R_F}{R_I} + 1$$

Example

Design an equal-component LPF with a critical frequency of 3 kHz and a roll-off of 20 dB/oct.

Minimum # of poles = 4

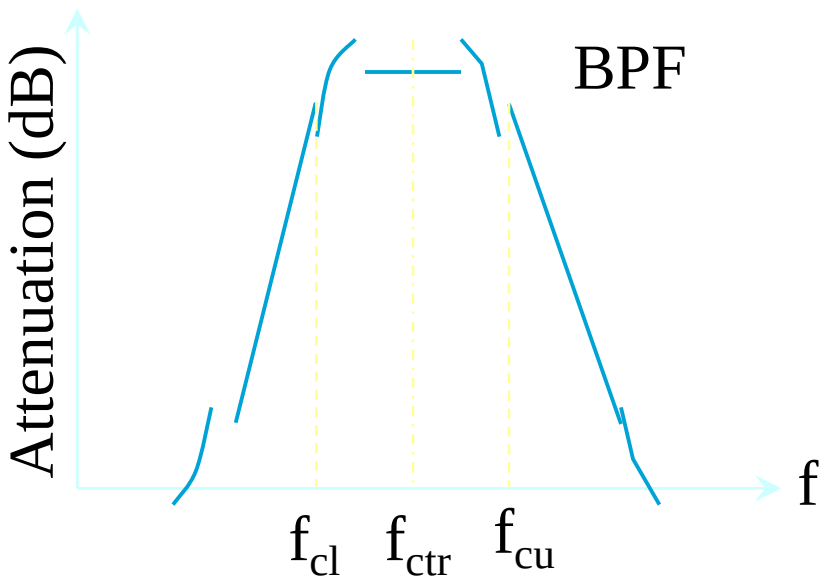
Choose C = 0.01 mF; ⑧ R = 5.3 kW

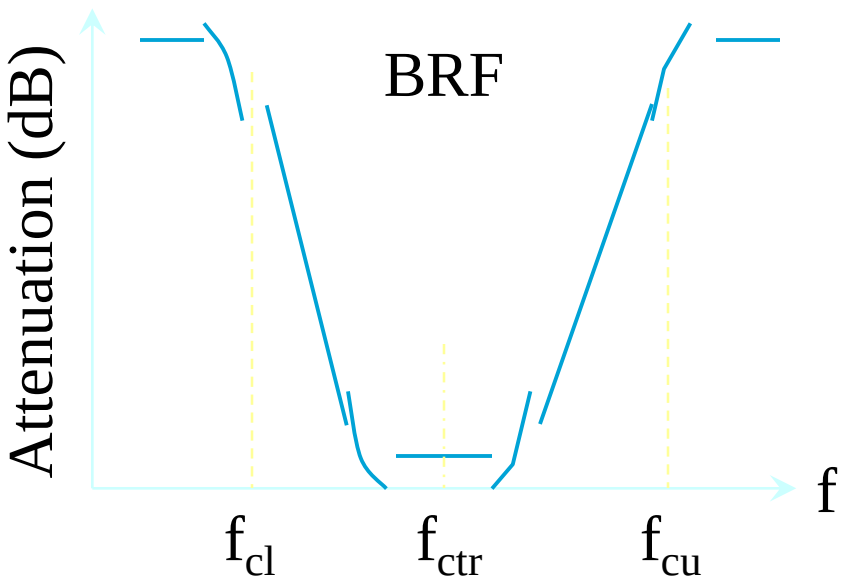
From table, $A_{v1} = 1.1523$, and $A_{v2} = 2.2346$.

Choose $R_{I1} = R_{I2} = 10$ kW; then $R_{F1} = 1.5$ kW, and $R_{F2} = 12.3$ kW .

Select standard values: 5.1 kW, 1.5 kW, and 12 kW.

Bandpass and Band-Rejection Filter





The quality factor, Q, of a filter is given by:

$$Q = \frac{f_{ctr}}{BW}$$

where BW = $f_{cu} - f_{cl}$ and

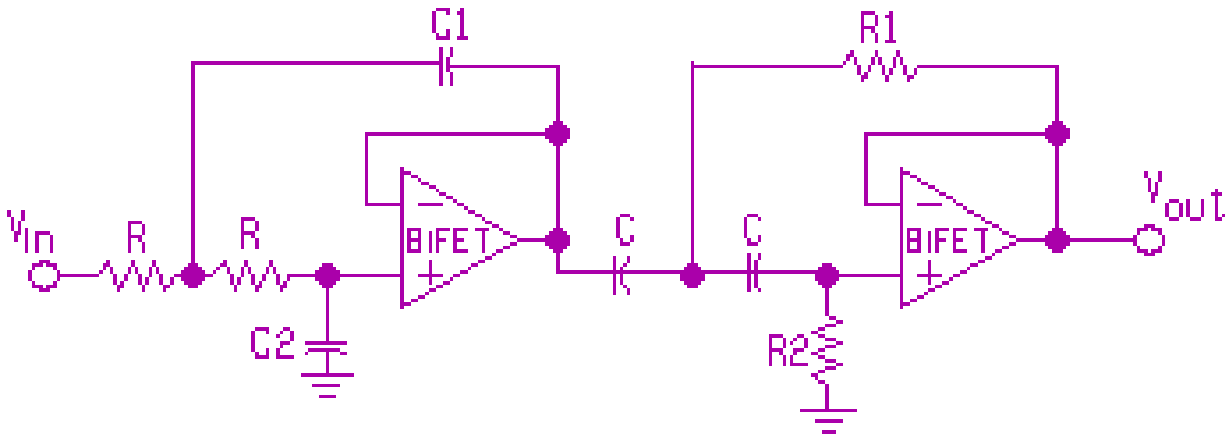
$$f_{ctr} = \sqrt{f_{cu} f_{cl}}$$

More On Band pass Filter

If BW and f_{centre} are given, then:

$$f_{cl} = \sqrt{\frac{BW^2}{4} + f_{ctr}^2} - \frac{BW}{2}\,;\; f_{cu} = \sqrt{\frac{BW^2}{4} + f_{ctr}^2} + \frac{BW}{2}$$

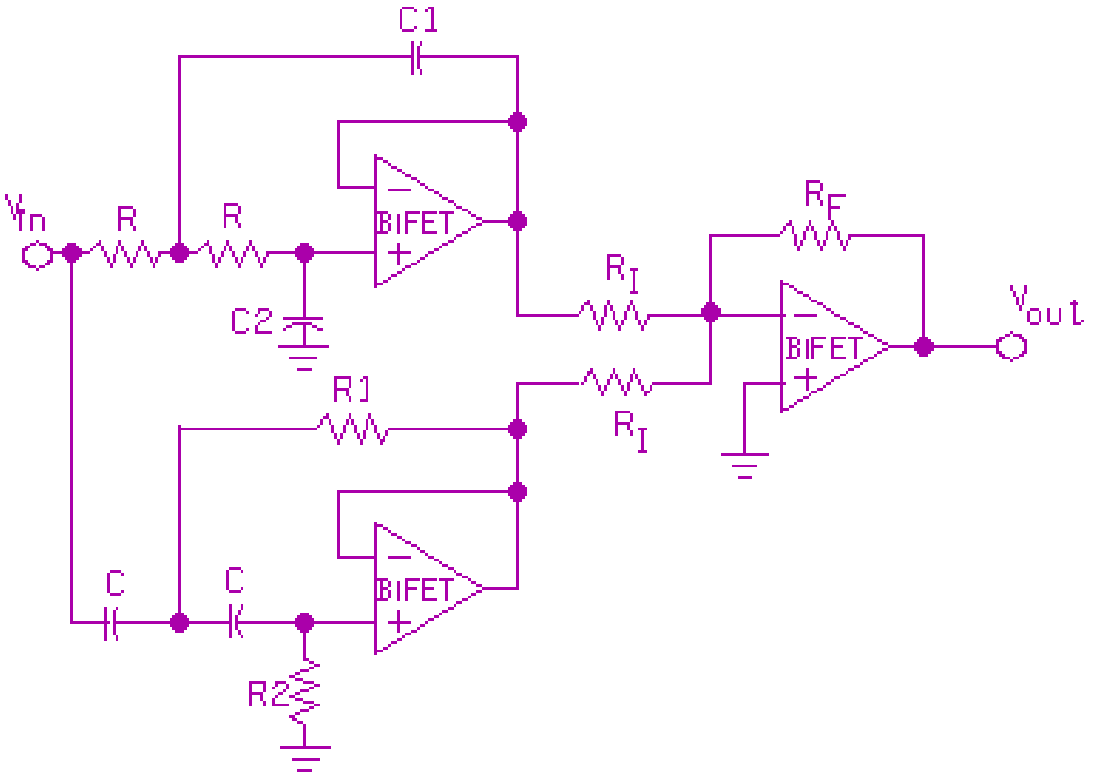
A *broadband* BPF can be obtained by combining a LPF and a HPF:



The Q of this filter is usually > 1.

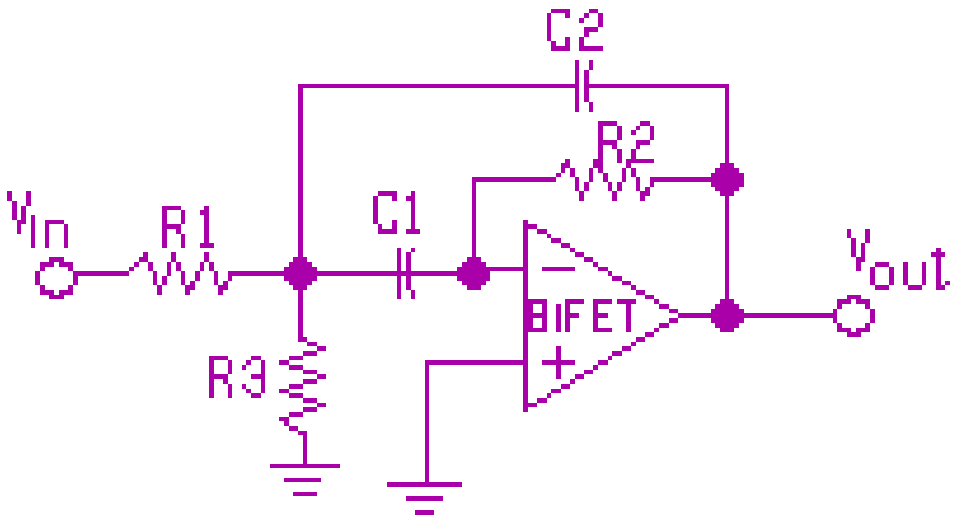
Broadband Band-Reject Filter

A LPF and a HPF can also be combined to give a broadband BRF:



2-pole band-reject filter

Narrow-band Band pass Filter



$$BW = \frac{f_{ctr}}{Q} = \frac{1}{2\pi R_1 C}$$

C1 = C2 = C

$R_2 = 2\,R_1$

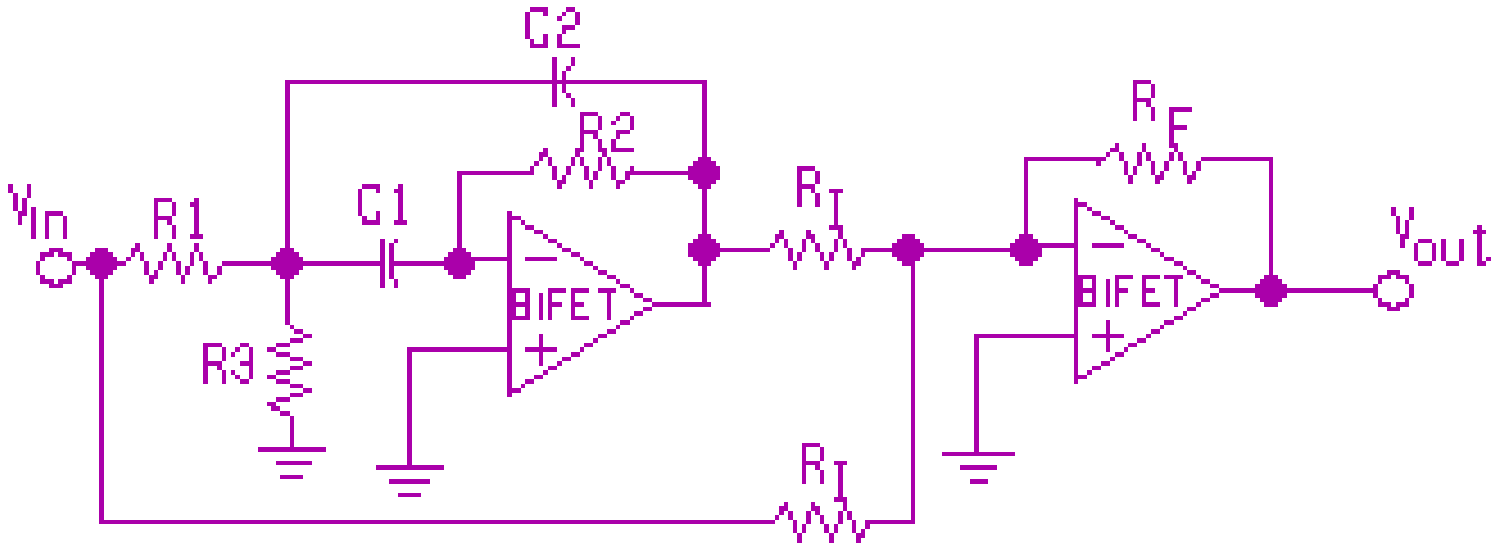
$$R_3 = \frac{R_1}{2Q^2 - 1}$$

$$f_{ctr} = \frac{1}{2\sqrt{2}\pi R_1 C}\sqrt{1 + \frac{R_1}{R_3}}$$

R_3 can be adjusted or trimmed to change f_{ctr} without affecting the BW. Note that Q < 1.

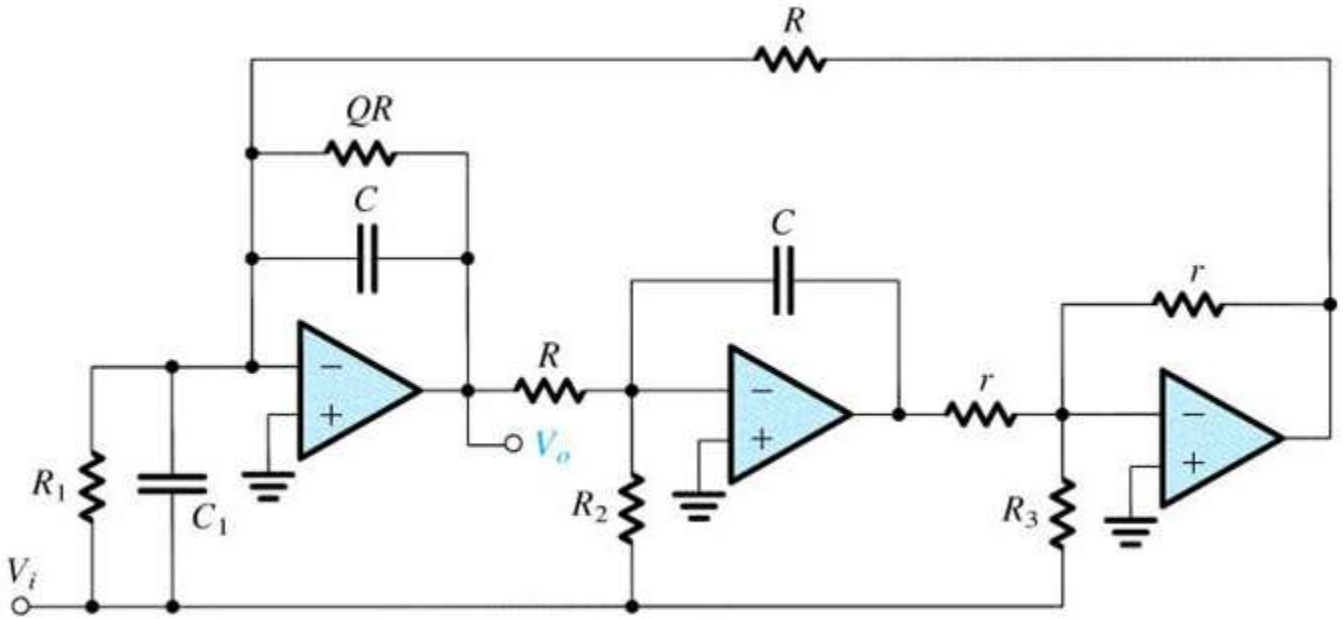
Narrow-band Band-Reject Filter

Easily obtained by combining the inverting output of a narrow-band BRF and the original signal:



The equations for R1, R2, R3, C1, and C2 are the same as before.
$R_I = R_F$ for unity gain and is often chosen to be >> R1.

TWO THOMOS BIQUAD FILTER



UNIT-IV
OP AMP APPLICATIONS-II

AUDIO OSCILLATORS

- An audio oscillator is useful for testing equipment that operates in the audio-frequency range. Such instruments always produce a sine-wave signal, variable in both amplitude and frequency, and usually provide a square-wave output as well. The maximum amplitude of the output waveform is typically on the order of 25 V_{rms}. whereas the range of frequencies covers at least the audio-frequency range from 20 Hz to 20 kHz. The most common output impedances for audio oscillators are 75 Ω and 600 Ω.

- The two most common audio-oscillator circuits are the Wien bridge oscillator and the phase-shift oscillator, both of which employ RC feedback networks. The Wien bridge offers some very attractive features, including a straightforward design, a relatively pure sine-wave output, and a very stable frequency.

Wien Bridge

- The Wien bridge oscillator is essentially a feedback amplifier in which the Wien bridge serves as the phase-shift network. The Wien bridge is an ac bridge, the balance of which is achieved at one particular frequency.

Cont'd

- The basic Wien bridge oscillator is shown in Fig. 1-2. as can be seen. the Wien bridge oscillator consists of a Wien bridge and an operational amplifier represented by the triangular symbol. Operational amplifiers are integrated circuit amplifiers and have high-voltage gain, high input impedance, and low output impedance. The condition for balance for an ac bridge is

$$Z_1 Z_4 = Z_2 Z_3 \quad \textbf{(1-2)}$$

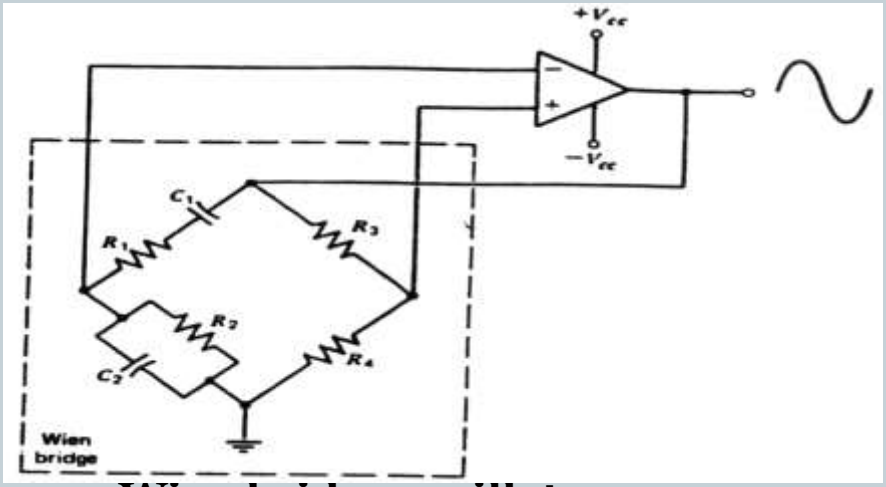


Fig. 1-2 Wien bridge oscillator.

Cont'd

Where

$$Z_1 = R_1 - j/\omega C_1$$

$$Z_2 = \frac{R_2(-j/\omega C_2)}{R_2 - j/\omega C_2} = \frac{-jR_2}{-j + R_2\omega C_2}$$

$$Z_3 = R_3$$

$$Z_4 = R_4$$

Substituting the appropriate expressions into Eq. 1-2 yields

$$\left(R_1 - \frac{j}{\omega C_1}\right)R_4 = \left(\frac{-jR_2}{-j + R_2\omega C_2}\right)R_3 \quad (1\text{-}3)$$

Cont'd

- if the bridge is balanced both the magnitude and phase angle of the impedances must be equal. These conditions are best satisfied by equating real terms and imaginary terms. Separating and equating the real terms in Eq. 1-3 yields.

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \qquad (1\text{-}4)$$

Separating and equating imaginary terms in Eq. 1-3 yields

$$\omega C_1 R_2 = \frac{1}{\omega C_2 R_1} \qquad (1\text{-}5)$$

Cont'd

- Where $\omega = 2\pi f$ Substituting for to in Eq. 1-5, we can obtain an expression for frequency which is

$$f = \frac{1}{2\pi (C_1 R_1 C_2 R_2)^{1/2}} \qquad (1\text{-}6)$$

- If $C_1 = C_2 = C$ and $R_1 = R_2 = R$ then Eq. 1-4 simplifies yield

(1-7)

$$\frac{R_3}{R_4} = 2$$

Cont'd

- and from Eq. 1-6 we obtain

$$f = \frac{1}{2\pi RC} \qquad (1\text{-}8)$$

Where

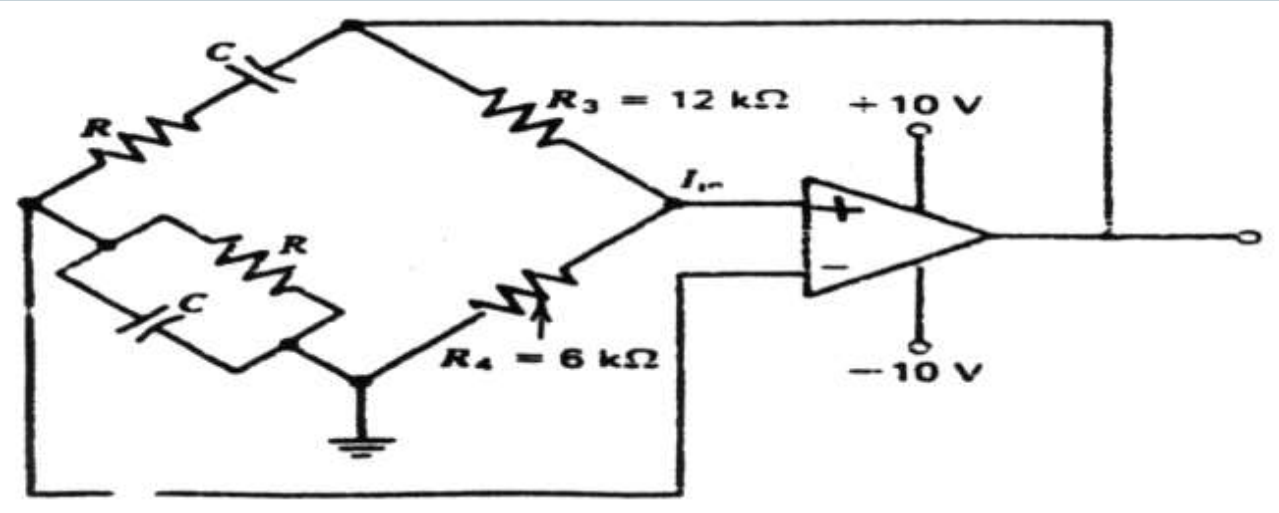
f = frequency of oscillation of the circuit in Hertz

C = capacitance in farads

R = resistance in ohms

EXAMPLE 1-1

- Determine the frequency of oscillation of the Wien bridge oscillator shown in Fig. 1-3 if $R = 6\Omega$ and C = 0.003 F.



Solution

- Using Eq. 1-8. we compute the frequency as

$$f = \frac{1}{2\pi RC}$$

$$= \frac{1}{(2\pi)(6k\Omega)(0.003\mu F)}$$

$$= 8.885 kHz$$

Wein Bridge

- It can be shown, by using ordinary ac circuit analysis techniques, that Eq. 1-2 is satisfied by the value of the components in the circuit in Fig. 1-3. The design of a Wien bridge oscillator can be approached by selecting an operating frequency and level of current that will be acceptable through each arm of the bridge. The bridge currents are typically larger by at least a factor of 100 than the maximum input current to the amplifier, and the peak value of the sinusoidal output voltage is typically on the order of 90% of V_{cc}.

EXAMPLE 1-2

- Design a Wien bridge oscillator around the following specifications:
- F = 15 kHz
- V_{cc} = 10V
- $/_{in}$ = 1
- $/R_4 = 100/_{in}$

Solution

- If the peak value of the sinusoidal waveform is 90% of V_{cc}, we can solve for the value of $R_3 + R_4$ as

Using Eq. 1-7, we can say that

$$R_3 + R_4 = \frac{0.9V_{cc}}{100\,\mu A} = 2R_4$$

$$= \frac{9V}{100\,\mu A} = 90\,k\Omega$$

Cont'd

Therefore

$$3R_4 = 90$$

$$R_4 = 30$$

and

$$R_3 = 2R_4 = 60$$

Wien Bridge

- We arrived at Eq. 1-7 by letting $R_1 = R_2 = R$. It is generally convenient to let $R_1 = R_2 = R_4$: therefore,

$$R_1 = R_2 = 30$$

Using Eq. 1-8. we can now solve for the capacitance *C* as

$$C = \frac{1}{2\pi f R}$$

$$= \frac{1}{(2\pi)(15kHz)(30k\Omega)} = 354\,pF$$

Cont’d

- The Wien bridge oscillator is widely used in audio oscillators because of its relatively small amount of distortion, excellent frequency stability, comparatively wide frequency range, and ease of changing frequency. A typical commercial Wien bridge oscillator can have a frequency range extending from 5 Hz to 500 kHz in decade steps.

Phase Shift Oscillator

- The second audio-oscillator circuit of interest is the phase-shift oscillator.
- The phase-shift network for the phase-shift oscillator, is an RC network made up of equal-value capacitors and resistors connected in cascade. Each of the three *RC* stages shown provides a 60^{o} phase shift. with the total phase shift equal to the required 180^{o}.

Cont'd

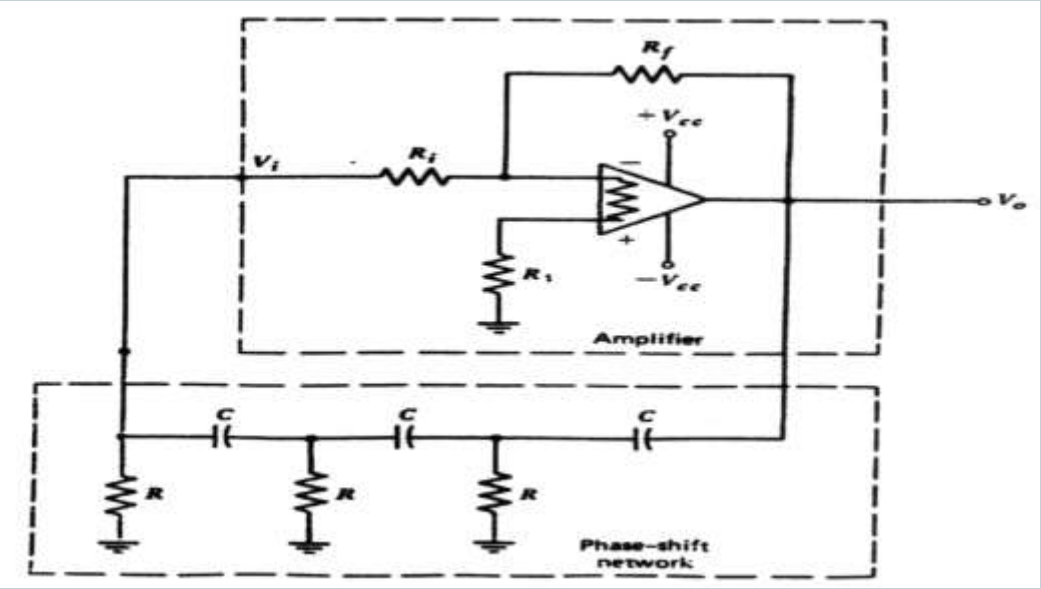


Fig.1-4 Basic phase-shift oscillator circuit.

Cont'd

- The phase-shift oscillator is analyzed by ignoring any minimal loading of the phase-shift network by the amplifier. By applying classical network analysis techniques, we can develop an expression for the feedback factor in terms of the phase-shift network components.
- The result is,

$$\beta = \frac{V_i}{V_o} = \frac{1}{1 - \frac{5}{(\omega RC)^2} + j\left[\frac{1}{(\omega RC)_3} - \frac{6}{\omega RC}\right]} \qquad (1\text{-}9)$$

Cont'd

- If the phase shift of the feedback network satisfies the 180^{o} phase-shift requirements, the imaginary components of Eq. 1-9 must be equal to zero or

$$\frac{1}{(\omega RC)^3} - \frac{6}{\omega RC} = 0$$

Cont'd

- The frequency of oscillation for the circuit can be determined by substituting 2 for in Eq. 1-10 and solving for the frequency. The result is

$$f = \frac{1}{2\sqrt{6\pi RC}} \qquad (10\text{-}11)$$

Cont'd

- We can express Eq. 1-11 as

$$2\pi f = \frac{1}{\sqrt{6RC}} \tag{1-12}$$

or

$$\omega = \frac{1}{\sqrt{6RC}} \tag{1-13}$$

substituting for in Eq. 10-9, we obtain

$$\beta = \frac{V_i}{V_2} = \frac{1}{1 - 5/(1/6) + j(6\sqrt{6} - 6\sqrt{6}} \tag{1-14}$$

Cont'd

- or

$$\beta = \frac{V_i}{V_o} = \frac{1}{1 - 5\,x\,6} = \frac{1}{29} \qquad (1\text{-}15)$$

Rewriting Eq. 1-15, we see that

$$V_o = -29V_i$$

which means that the gain of the amplifier must be at least 29 if the circuit is to sustain oscillation.

EXAMPLE 1-3

- Determine the frequency of oscillation of a phase-shift oscillator with a three-section feedback network consisting of 13-Ω resistors and 100- μ F capacitors.

Solution

- Using Eq. 1-11. we can compute the frequency Of oscillation as

$$f = \frac{1}{2\pi\sqrt{6}RC}$$

$$= \frac{1}{(2\pi\sqrt{6})(13\Omega)(100\mu F)} = 50Hz$$

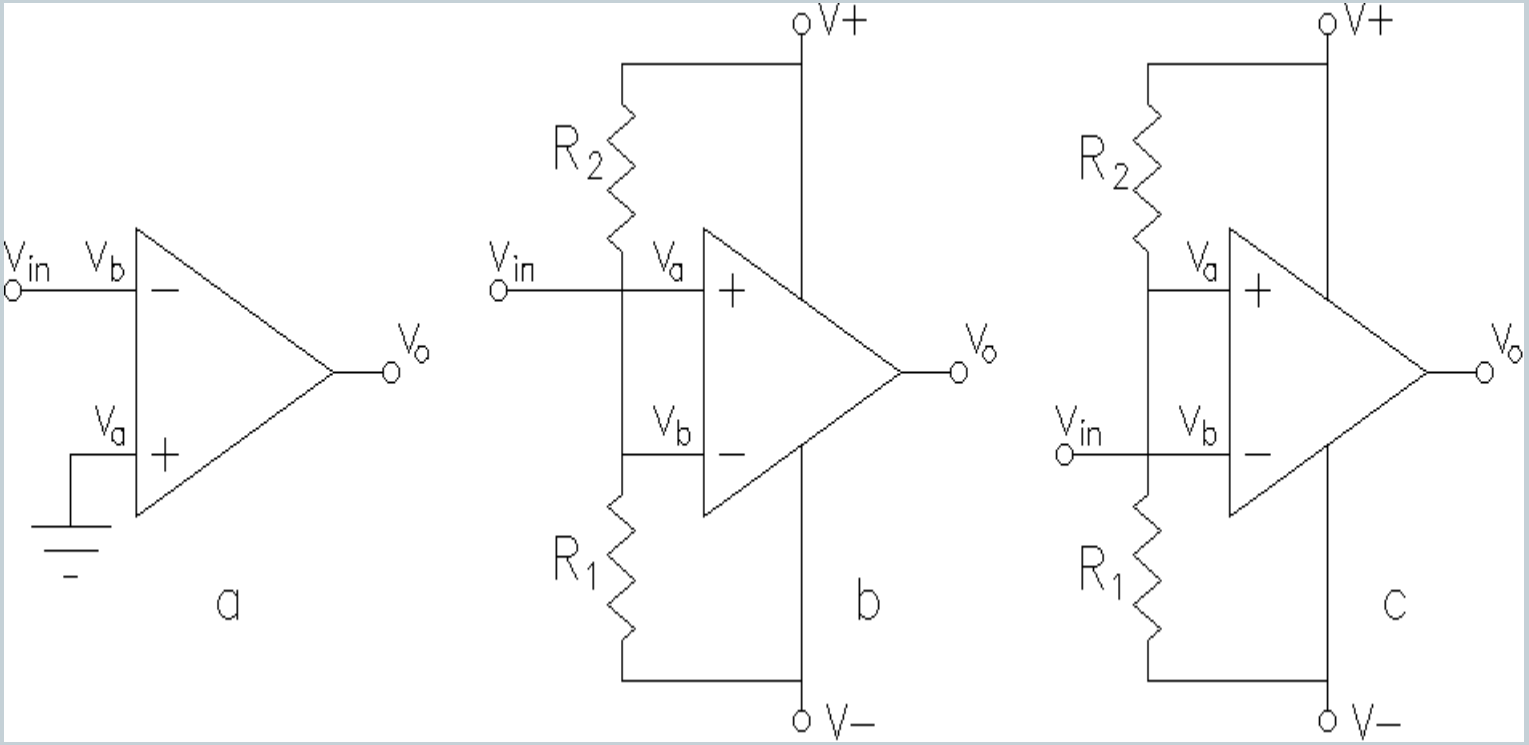
Cont'd

- The phase-shift oscillator is useful for noncritical applications. particularly at medium and low frequencies, even down to 1Hz, because of its simplicity.
- However, its frequency stability is net as good as that of the Wien bridge oscillator, distortion is greater, and changing frequency is inconvenient because the value of each capacitor must be adjusted.
- The choice of an oscillator circuit to operate in the audio-frequency range is determined by the particular application.

Comparator

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is an open loop op - amp with output + Vsat

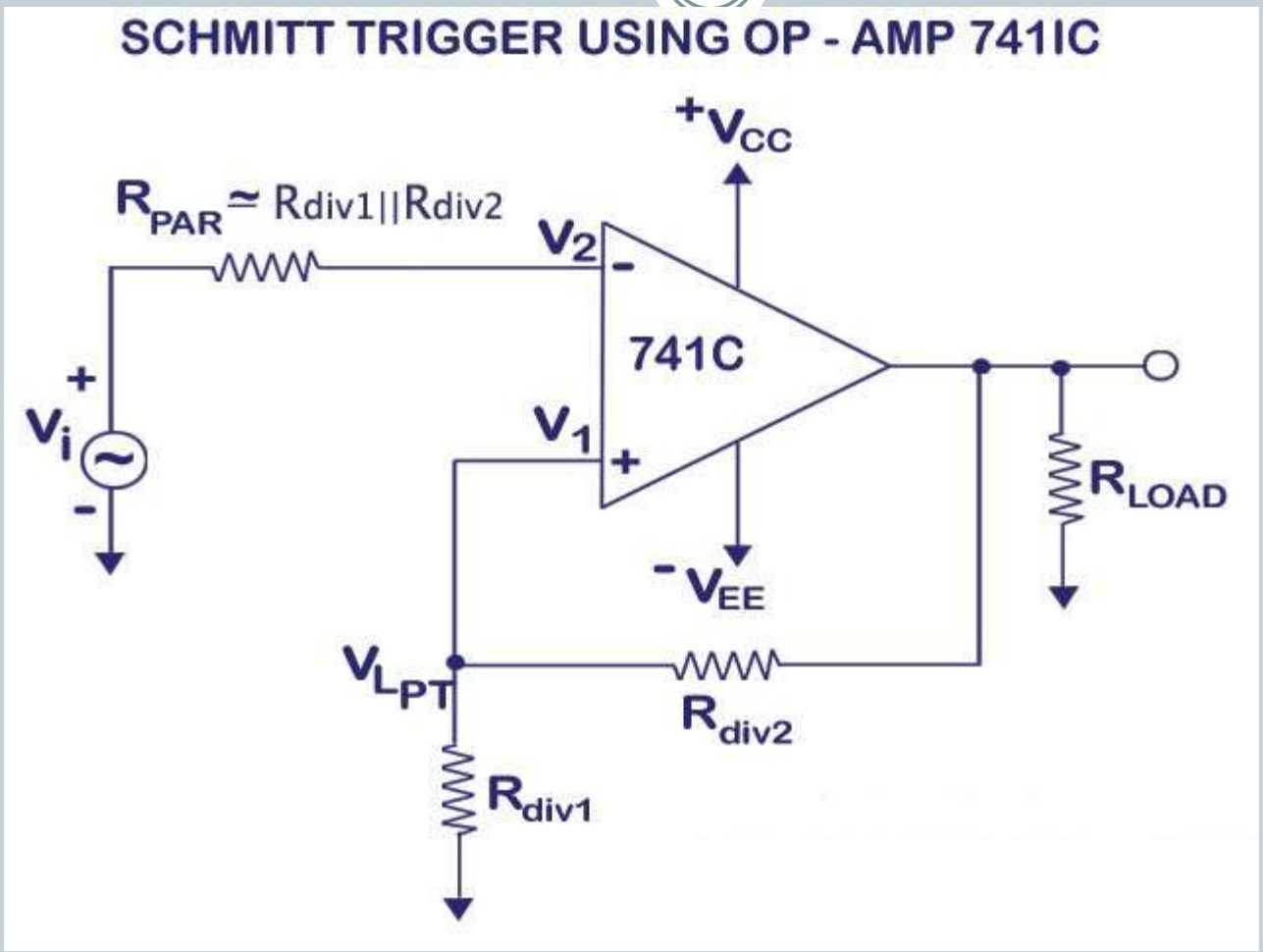
Comparator



Applications of comparator

1. Zero crossing detector
2. Window detector
3. Time marker generator
4. Phase detector

Schmitt trigger

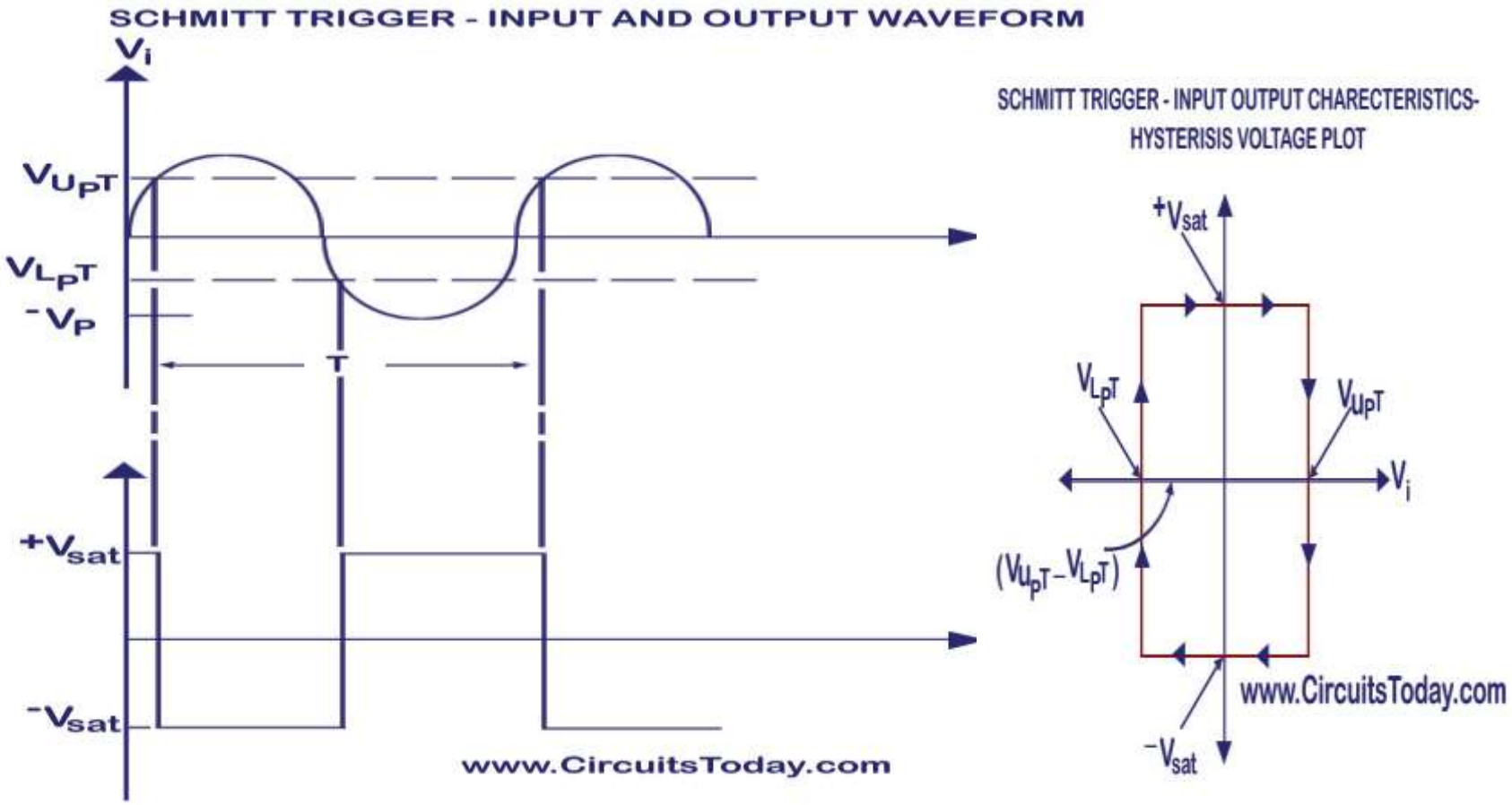


Schmitt trigger

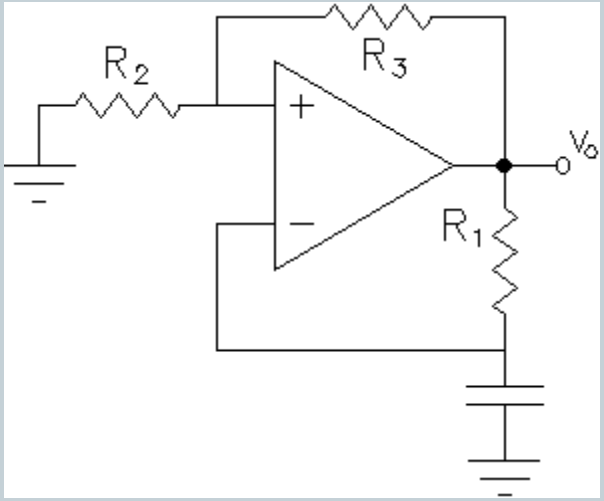
Schmitt trigger is a regenerative comparator. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform

Upper Threshold Voltage, Vupt = +Vsat (Rdiv1/[Rdiv1+Rdiv2])

Lower Threshold Voltage, Vlpt = -Vsat (Rdiv1/[Rdiv1+Rdiv2])


SCHMITT TRIGGER - INPUT AND OUTPUT WAVEFORM
Vi
VUpT
VLpT
-VP
T
+Vsat
-Vsat
www.CircuitsToday.com
SCHMITT TRIGGER - INPUT OUTPUT CHARECTERISTICS-
HYSTERISIS VOLTAGE PLOT
+Vsat
VLpT
VUpT
Vi
(VUpT-VLpT)
www.CircuitsToday.com
-Vsat

square wave generator



Multivibrator

Multivibrators are a group of regenerative circuits that are used extensively in timing applications. It is a wave shaping circuit which gives symmetric or asymmetric square output. It has two states either stable or quasi- stable depending on the type of multivibrator

Monostable multivibrator

Monostable multivibrator is one which generates a single pulse of specified duration in response to each external trigger signal. It has only one stable state. Application of a trigger causes a change to the quasi- stable state.An external trigger signal generated due to charging and discharging of the capacitor produces the transition to the original stable state

Astable multivibrator

Astable multivibrator is a free running oscillator having two quasi- stable states. Thus, there is oscillations between these two states and no external signal are required to produce the change in state

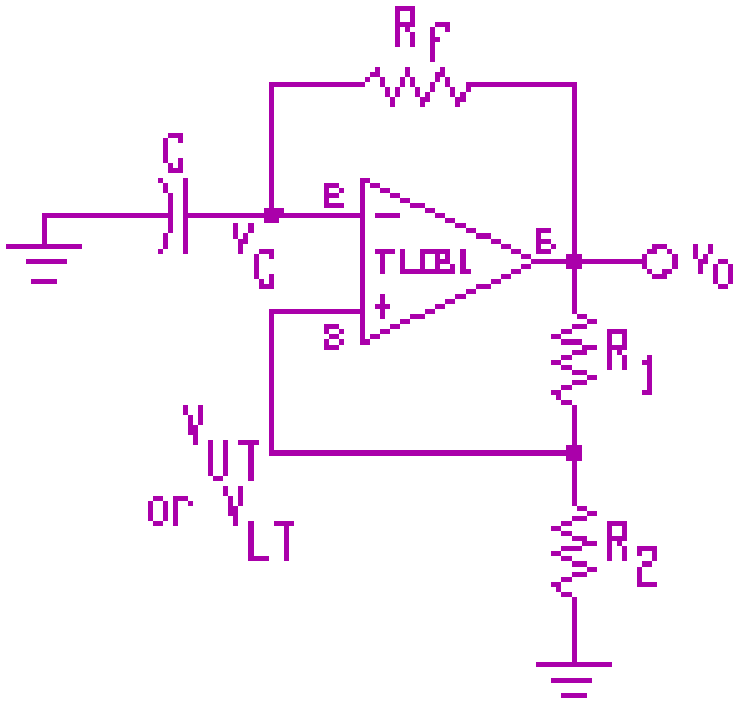
Astable multivibrator

Bistable multivibrator is one that maintains a given output voltage level unless an external trigger is applied . Application of an external trigger signal causes a change of state, and this output level is maintained indefinitely until an second trigger is applied . Thus, it requires two external triggers before it returns to its initial state

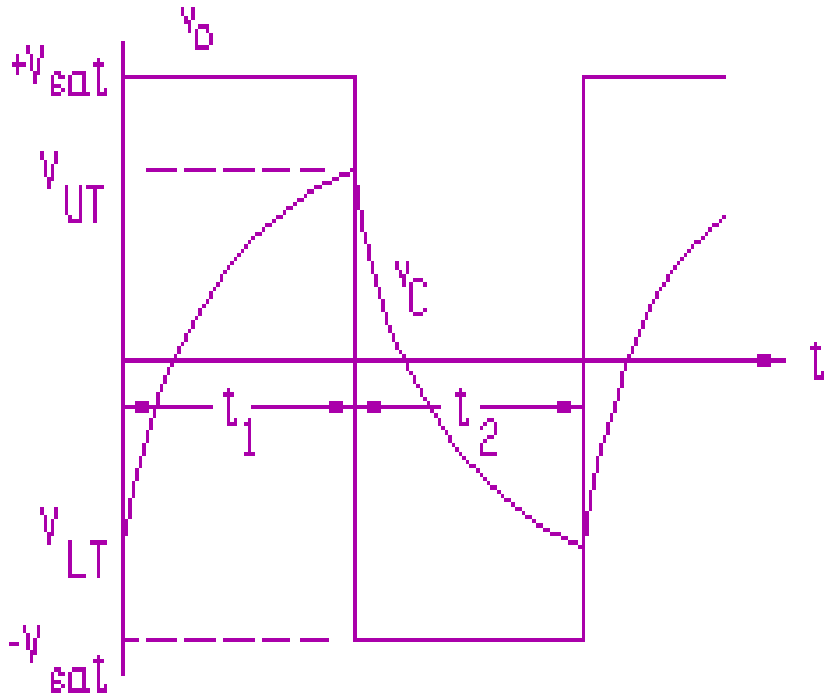
Bistable multivibrator

Bistable multivibrator is one that maintains a given output voltage level unless an external trigger is applied . Application of an external trigger signal causes a change of state, and this output level is maintained indefinitely until an second trigger is applied . Thus, it requires two external triggers before it returns to its initial state

Astable Multivibrator or Relaxation Oscillator



Circuit



Output waveform

Equations for Astable Multivibrator

$$V_{UT} = \frac{+V_{sat}R_2}{R_1 + R_2}; \quad V_{LT} = \frac{-V_{sat}R_2}{R_1 + R_2}$$

Assuming $|+V_{sat}| = |-V_{sat}|$

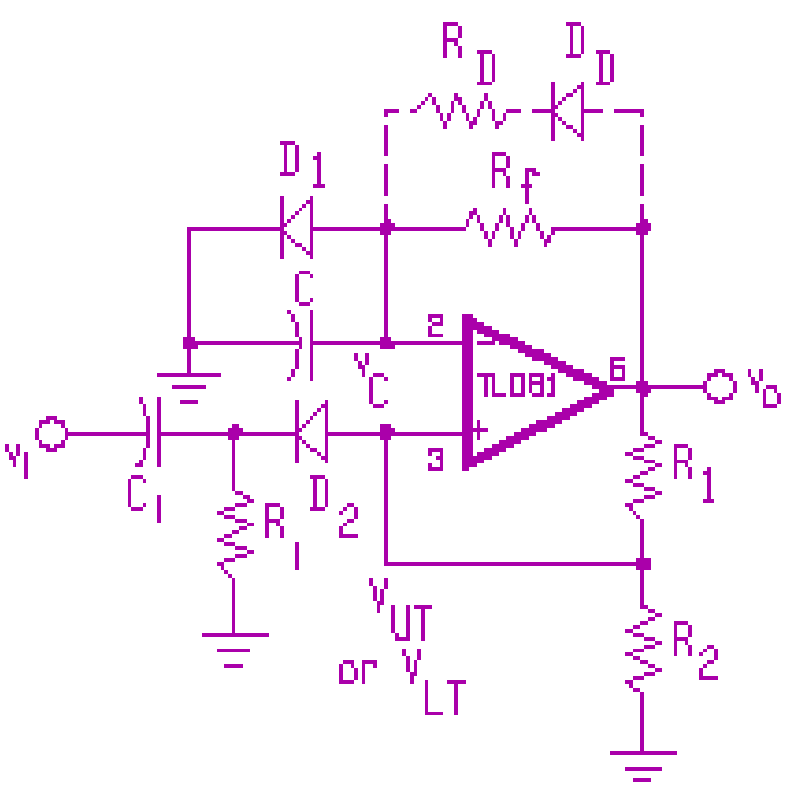
$$T = t_1 + t_2 = 2\tau \ln\left(\frac{R_1 + 2R_2}{R_1}\right)$$

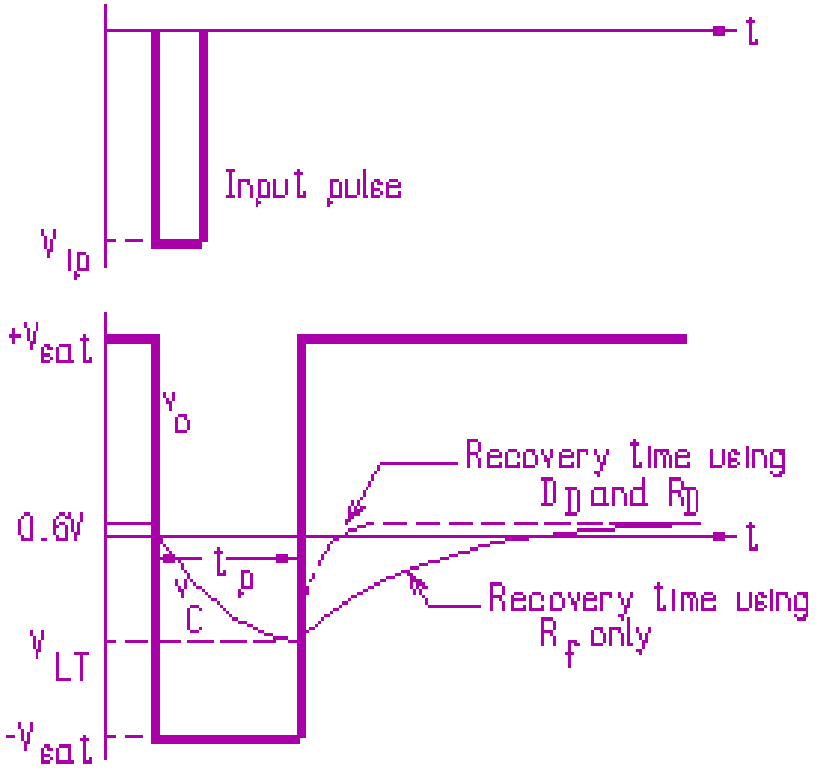
where ☺ = R_fC

If R_2 is chosen to be $0.86R_1$, then $T = 2R_fC$ and

$$f = \frac{1}{2R_fC}$$

Monostable (One-Shot) Multivibrator



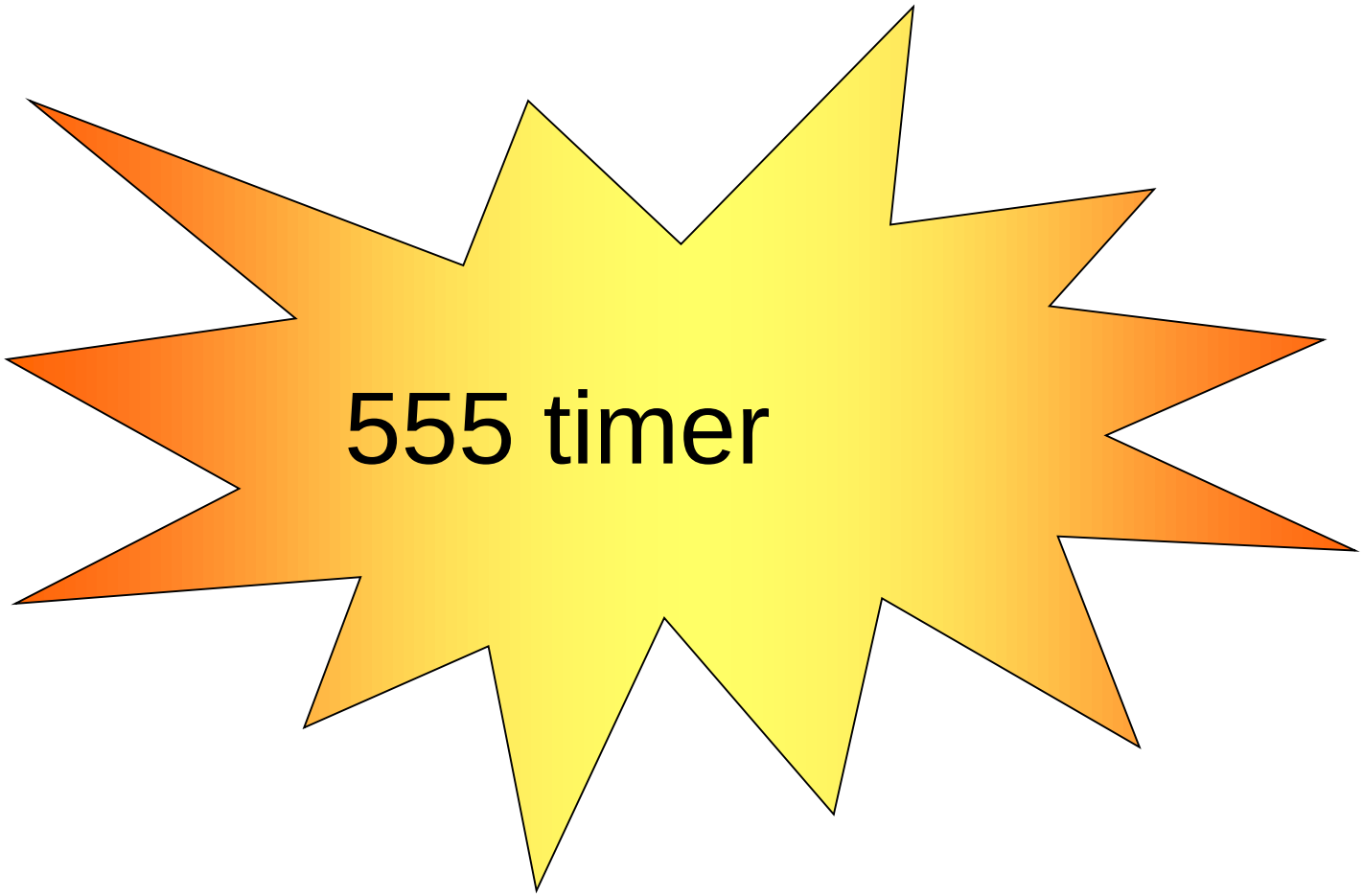


Circuit

Waveforms

Notes on Monostable Multivibrator

- Stable state: $v_o = +V_{sat}$, $V_C = 0.6$ V
- Transition to timing state: apply a -ve input pulse such that $|V_{ip}| > |V_{UT}|$; $v_o = -V_{sat}$. Best to select $R_iC_i \leq 0.1R_fC$.
- Timing state: C charges $t_p = R_f C \ln\left(\frac{|V_{sat}| + 0.6}{|V_{sat}| + V_{LT}}\right)$ through R_f. Width of timing pulse is:
  - If we pick $R_2 = R_1/5$, then $t_p = R_fC/5$.
  - Recovery state: $v_o = +V_{sat}$; circuit is not ready for retriggering until $V_C = 0.6$ V. The *recovery time* $\approx t_p$. To speed up the recovery time, R_D (= $0.1R_f$) & C_D can be added.


555 timer

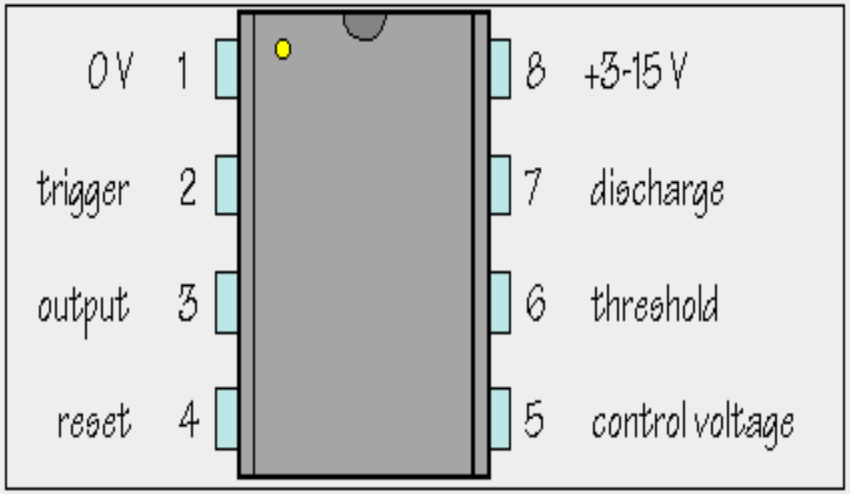
555 Timer;

The 555 timer is one of the most remarkable integrated circuits ever developed. It comes in a single or dual package and even low power cmos versions exist - ICM7555.

Common part numbers are;

LM555, NE555, LM556, NE556.

Pin configurations



The 555 timer consists of;

two voltage comparators
a bi-stable flip flop
a discharge transistor
and a resistor divider network.

Features of 555 Timer Basic blocks

1. It has two basic operating modes: monostable and astable
2. It is available in three packages. 8 pin metal can , 8 pin dip, 14 pin dip.
3. It has very high temperature stability

555 IC

The 555 timer is an integrated circuit specifically designed to perform signal generation and timing functions.

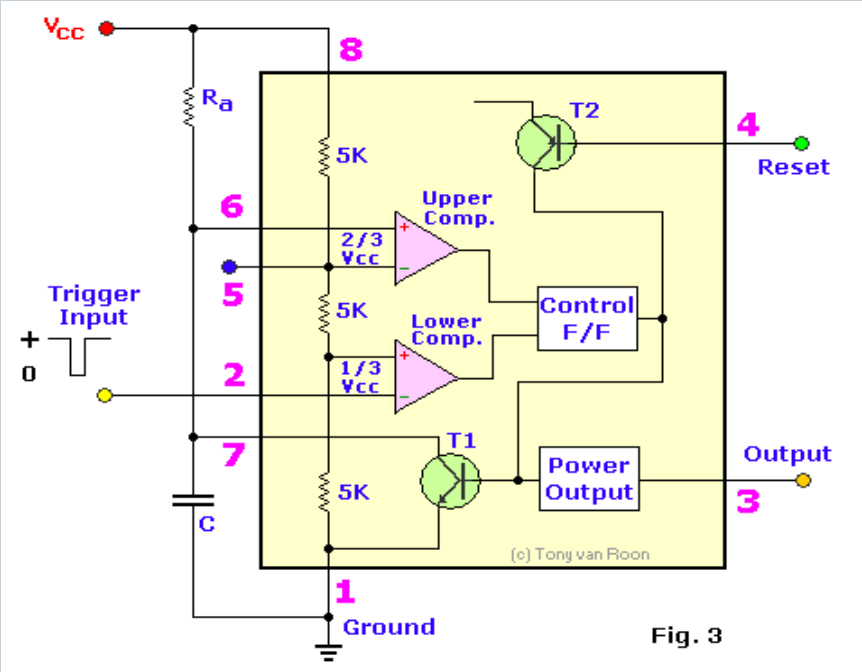
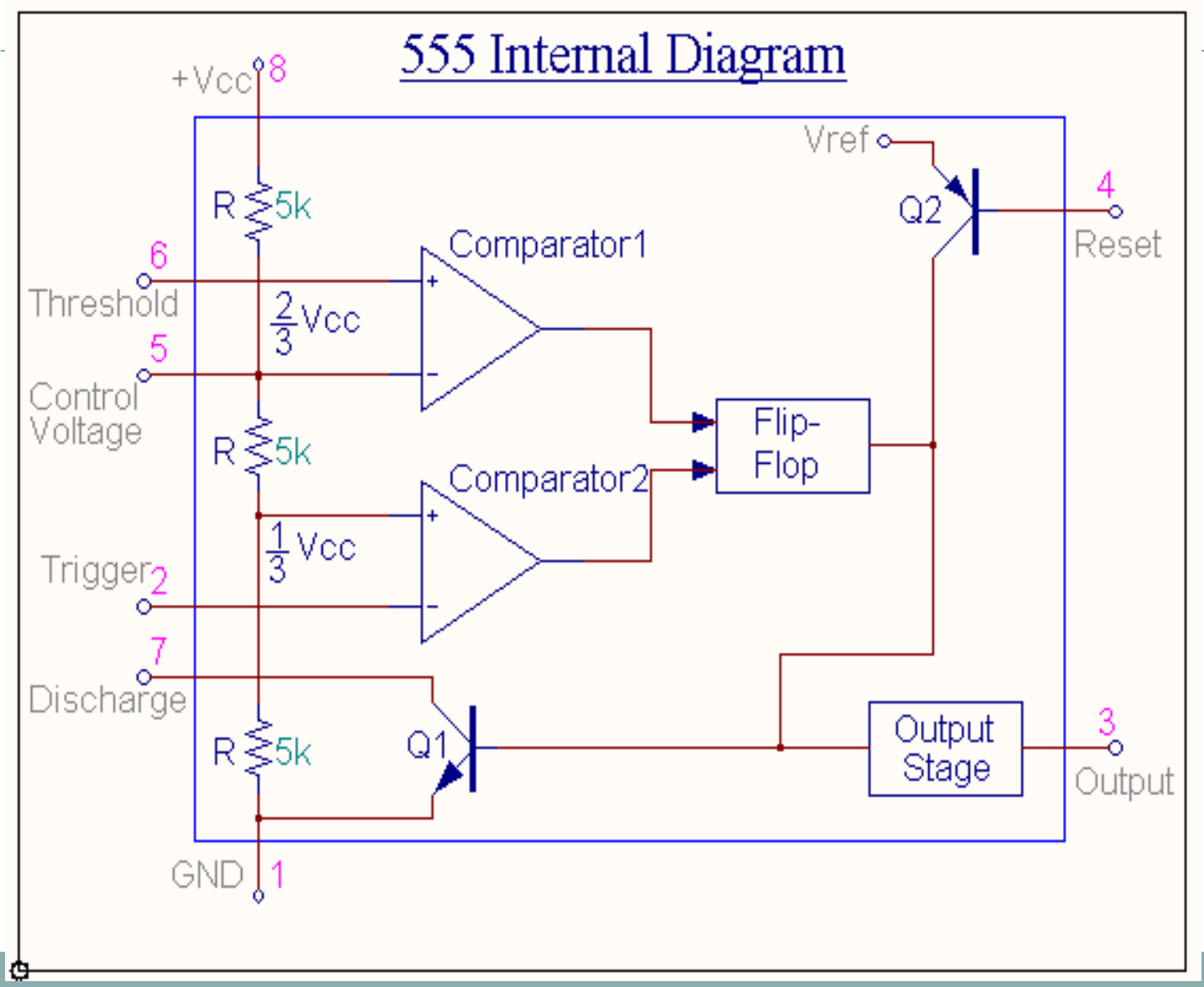


Fig. 3

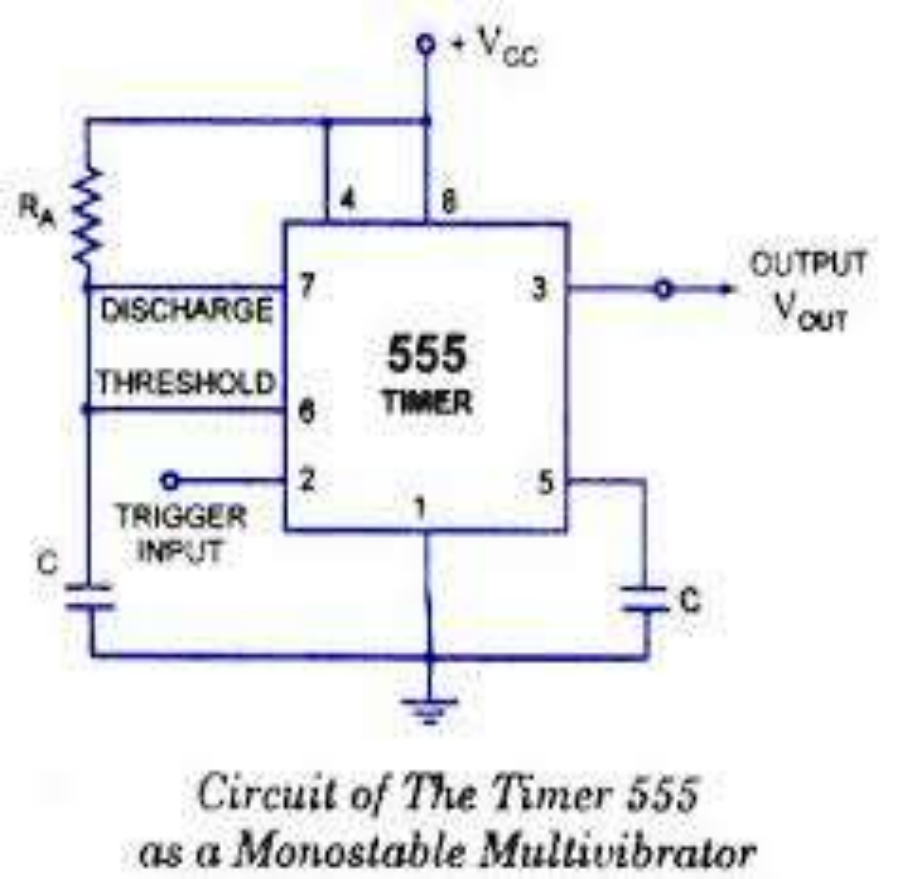
BLOCK DIAGRAM OF 555 IC



Applications of 555 Timer

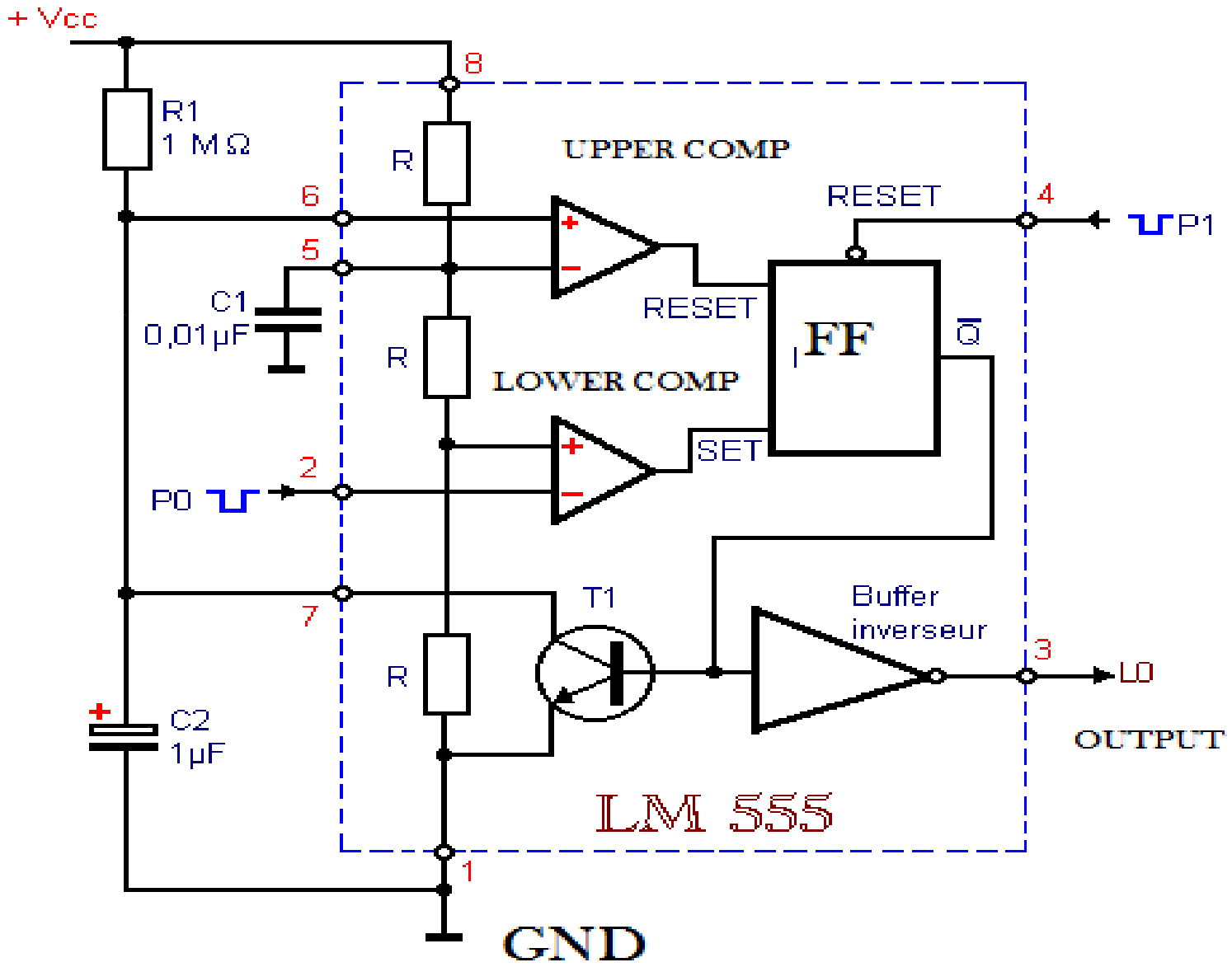
1. Astable Multivibrator
2. Monostable Multivibrator
3. Missing Pulse Detector
4. Linear Ramp Generator
5. Frequency Divider
6. Pulse Width Modulation
7. FSK Generator
8. Pulse Position Modulator
9. Schmitt Trigger

Monostable multivibrator

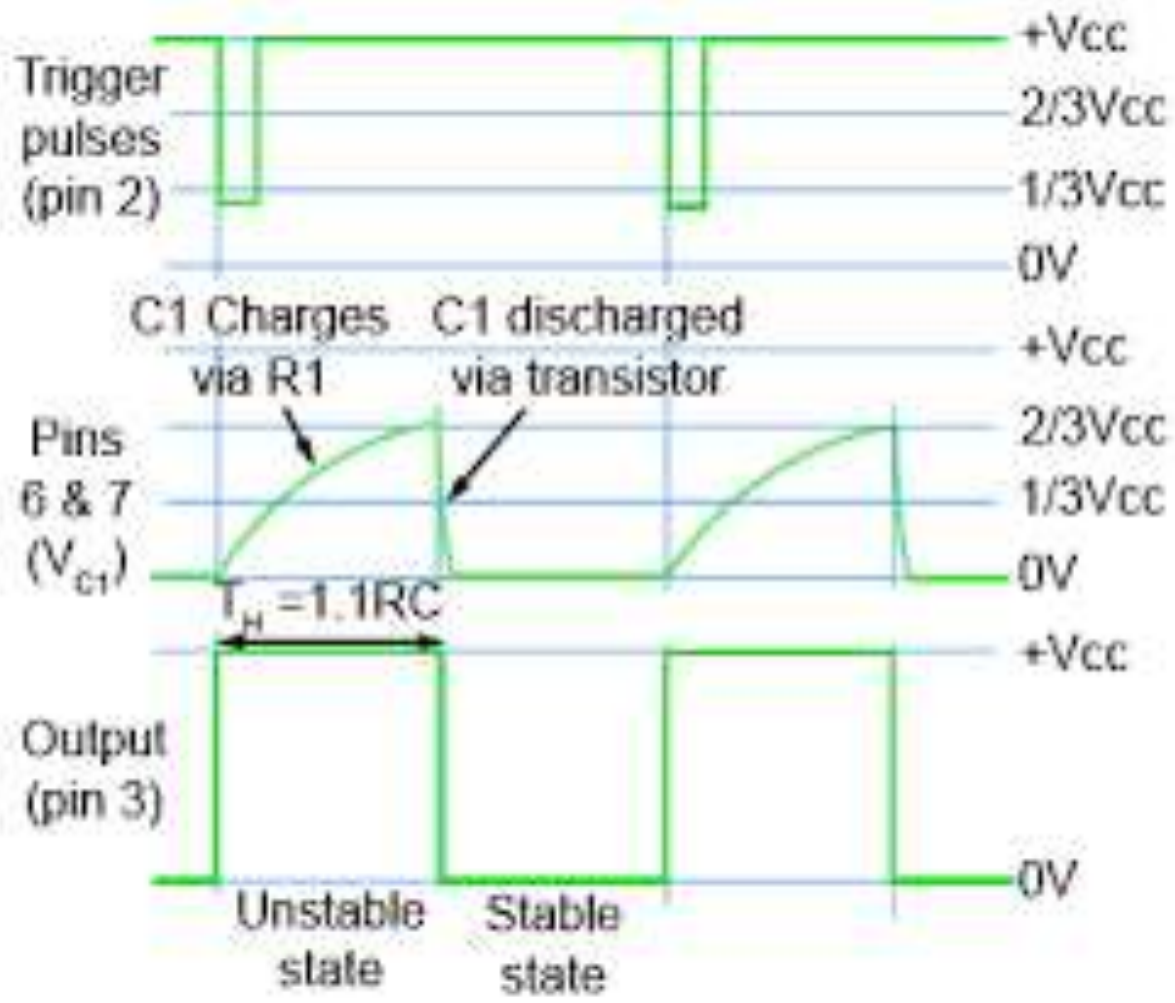


Circuit of The Timer 555 as a Monostable Multivibrator

Block diagram of Mono stable Multivibrator



Input and output waveforms



The capacitor C has to charge through resistance R_A. The larger the time constant R_AC, the longer it takes for the capacitor voltage to reach $+2/3V_{CC}$.

In other words, the RC time constant controls the width of the output pulse. The time during which the timer output remains high is given as

$$\mathbf{t_p = 1.0986 R_A C}$$

where R_A is in ohms and C is in farads. The above relation is derived as below. Voltage across the capacitor at any instant during charging period is given as

$$\mathbf{v_c = V_{CC}\,(1 - e^{-t/R_A C})}$$

Substituting $\mathbf{v_c = 2/3\ V_{CC}}$ in above equation we get the time taken by the capacitor to charge from 0 to $+2/3V_{CC}$.

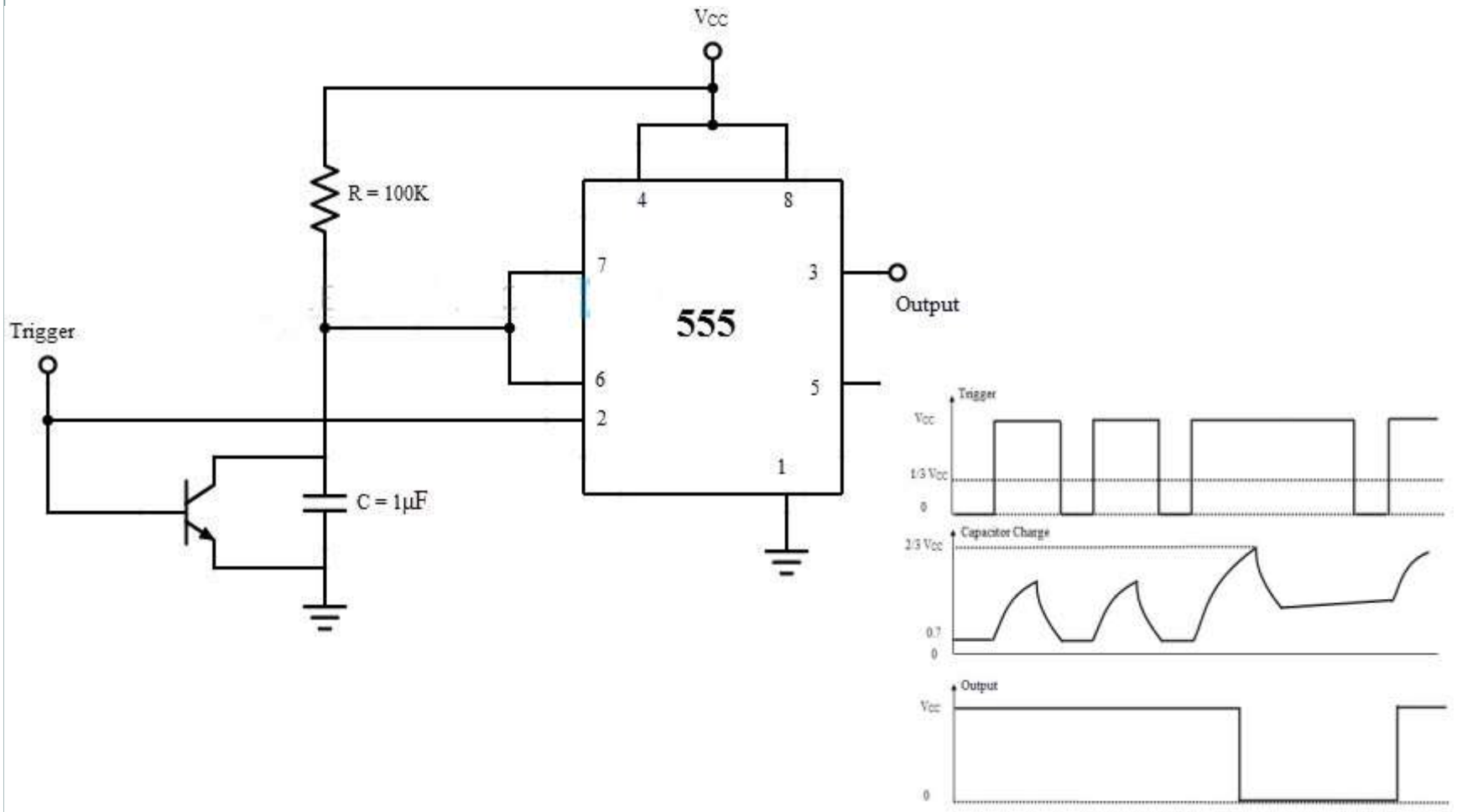
So $\mathbf{+2/3V_{CC}. = V_{CC}.\ (1 - e^{-t/RAC})}$ **or** $\mathbf{t - R_A C \log_e 3 = 1.0986\ R_A C}$

So pulse width, $\mathbf{t_P = 1.0986\ R_A C\ s\ 1.1\ R_A C}$

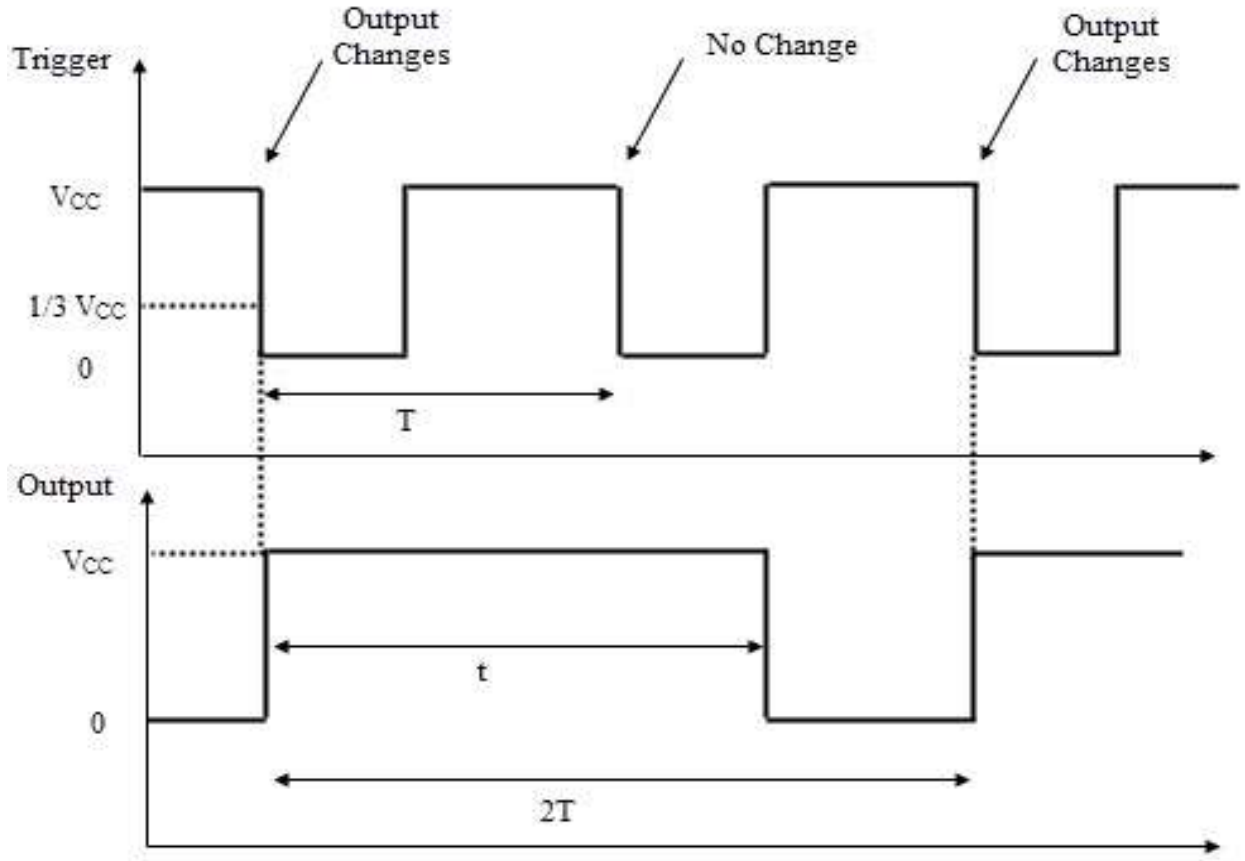
The pulse width of the circuit may range from micro-seconds to many seconds. This circuit is widely used in industry for many different timing applications.

Application of Monostable Multivibrator

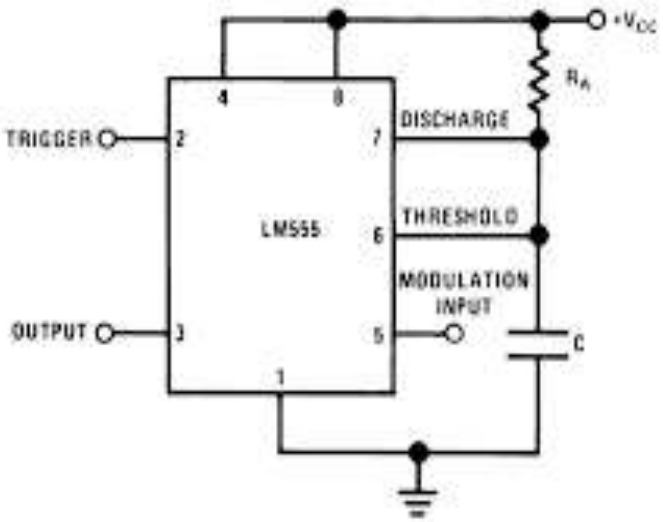
i) Missing Pulse detector

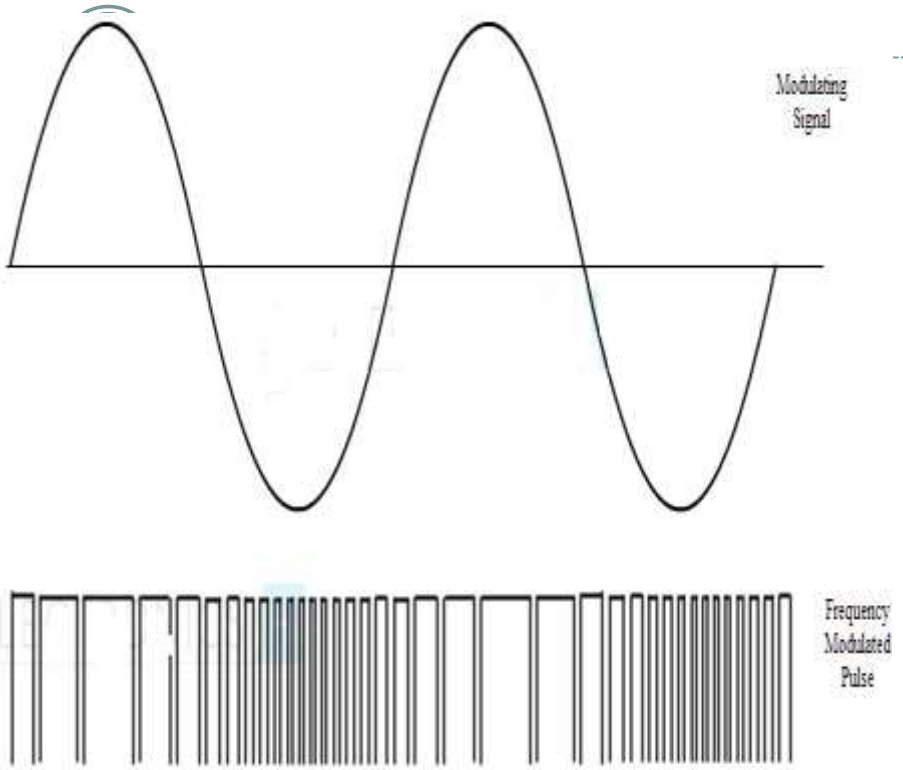


ii) Frequency divider



iii) Pulse width modulator

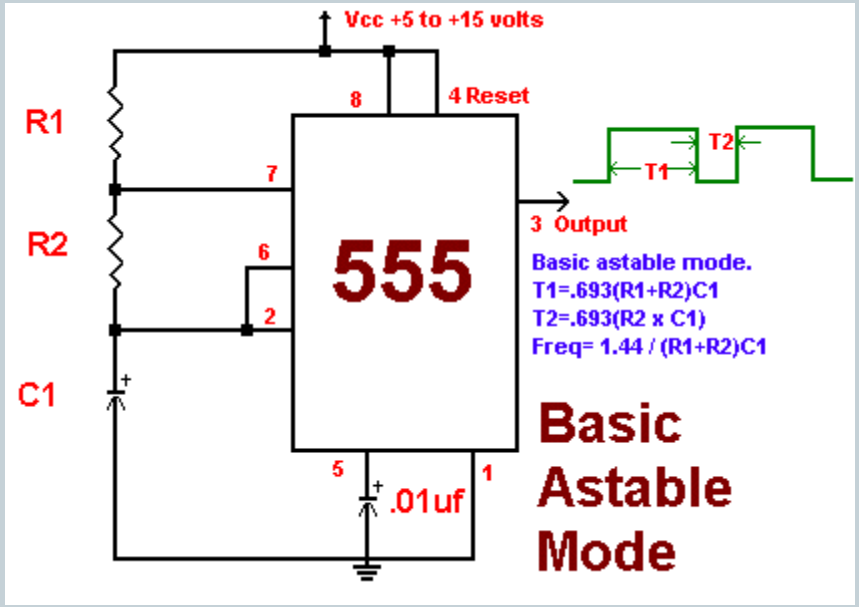




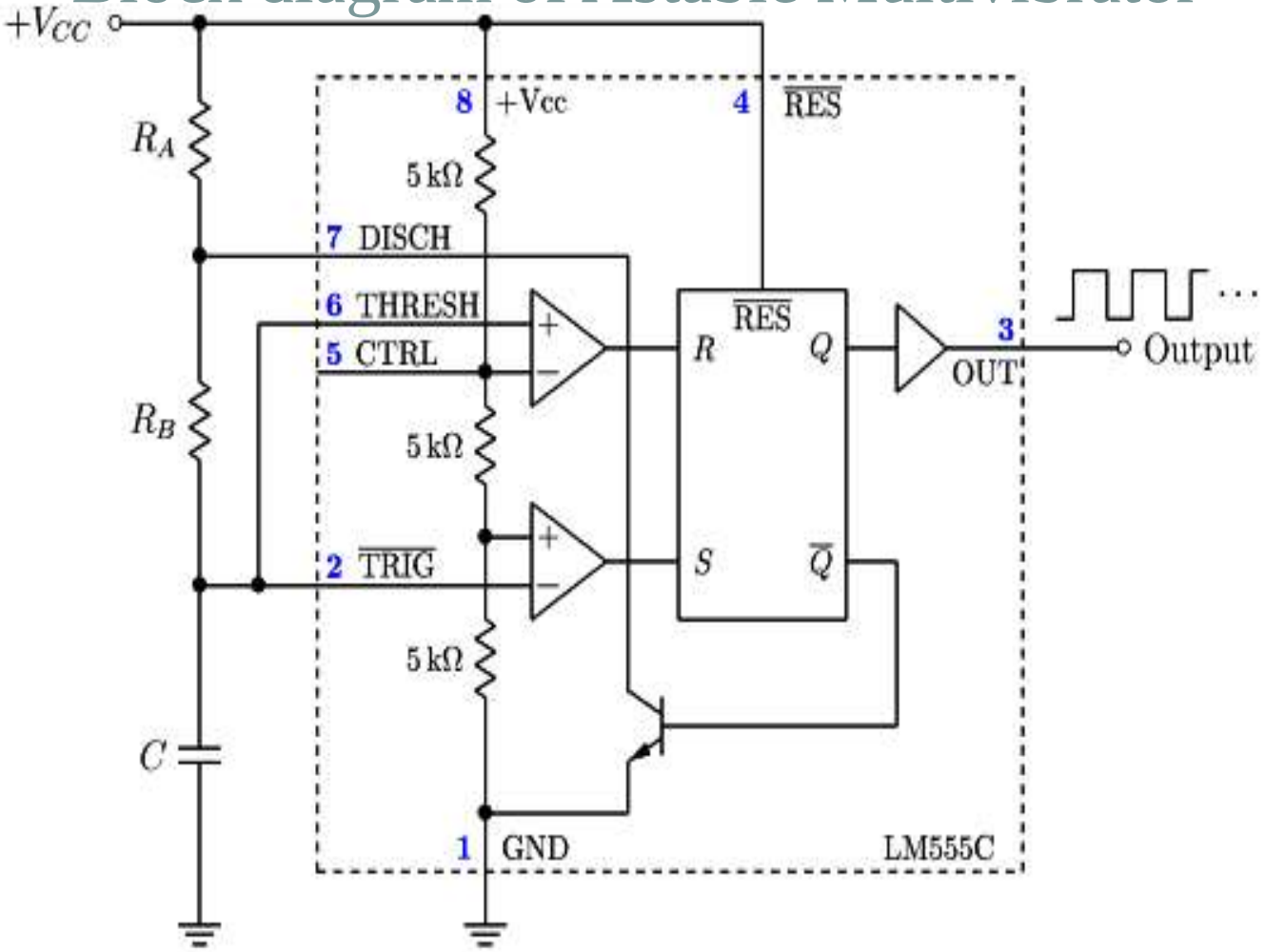
Astable multivibrator

- When the voltage on the capacitor reaches (2/3)Vcc, a switch is closed at pin 7 and the capacitor is discharged to (1/3)Vcc, at which time the switch is opened and the cycle starts over

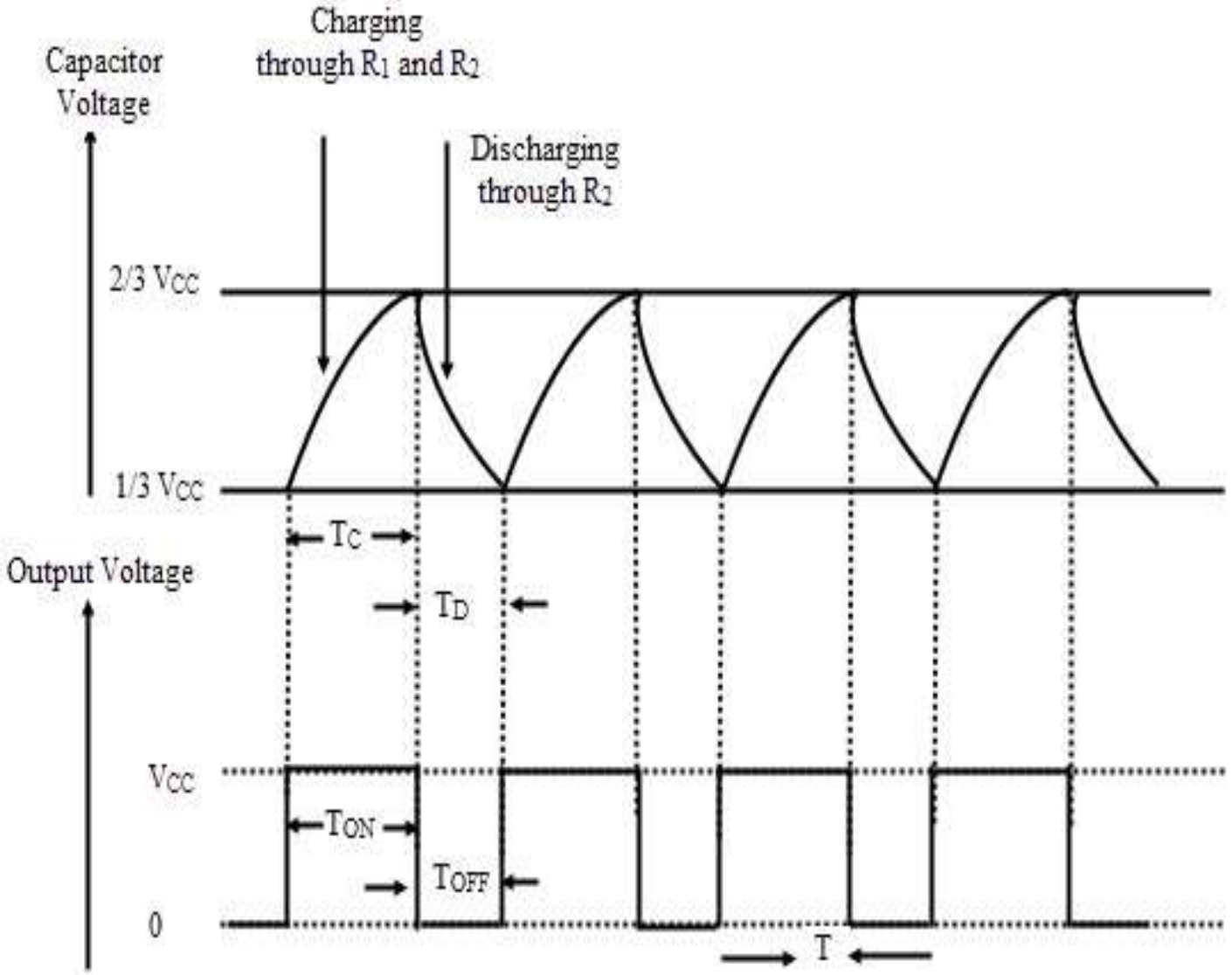
Astable multivibrator



Block diagram of Astable Multivibrator

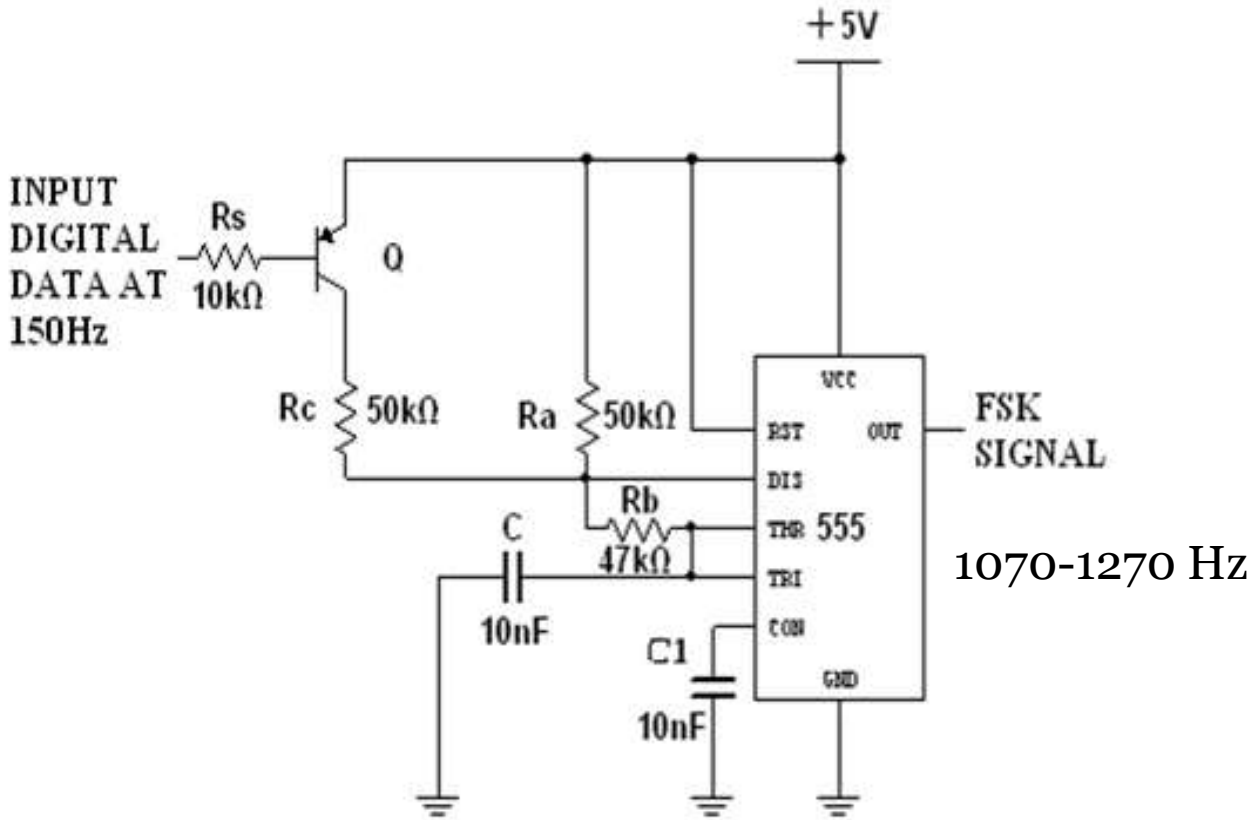


Output waveforms

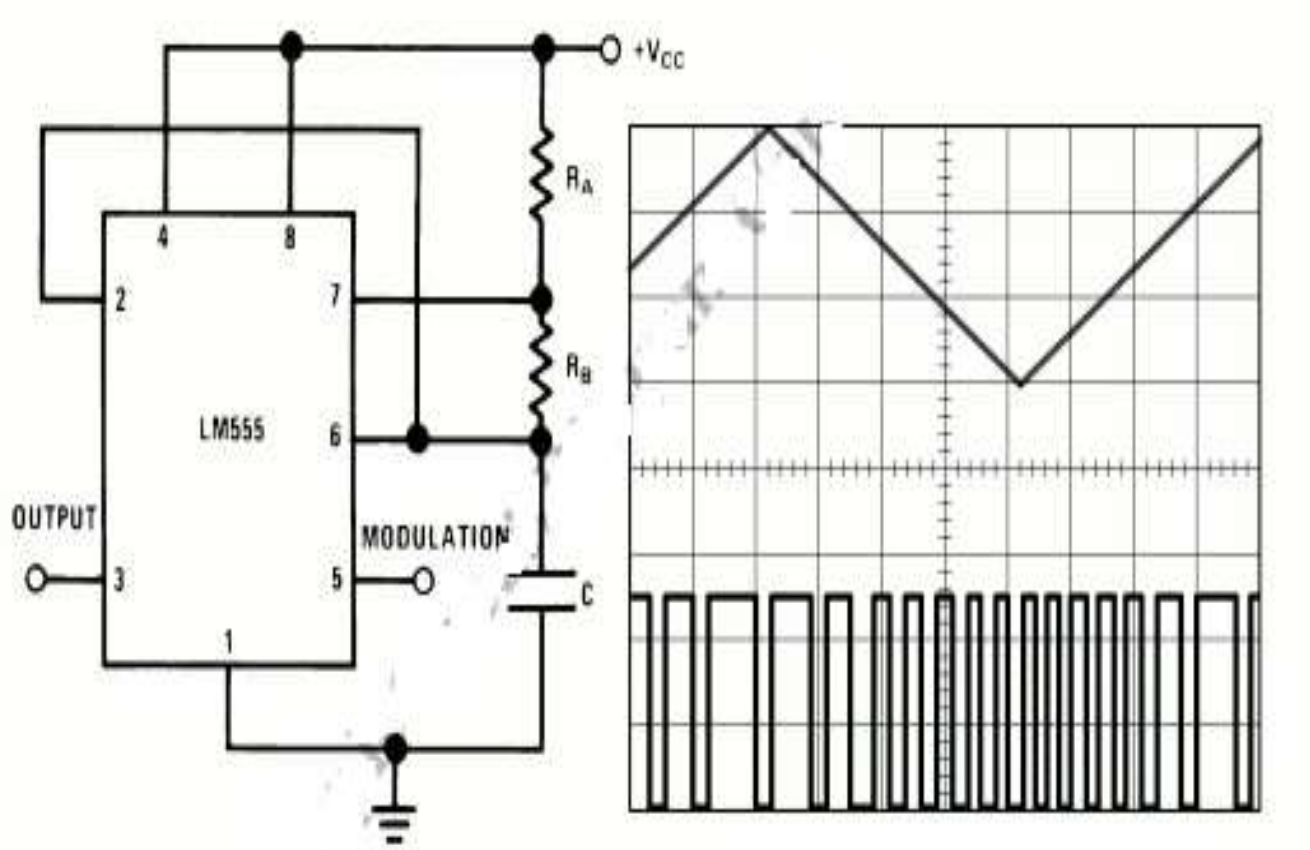


Application of Astable Multivibrator

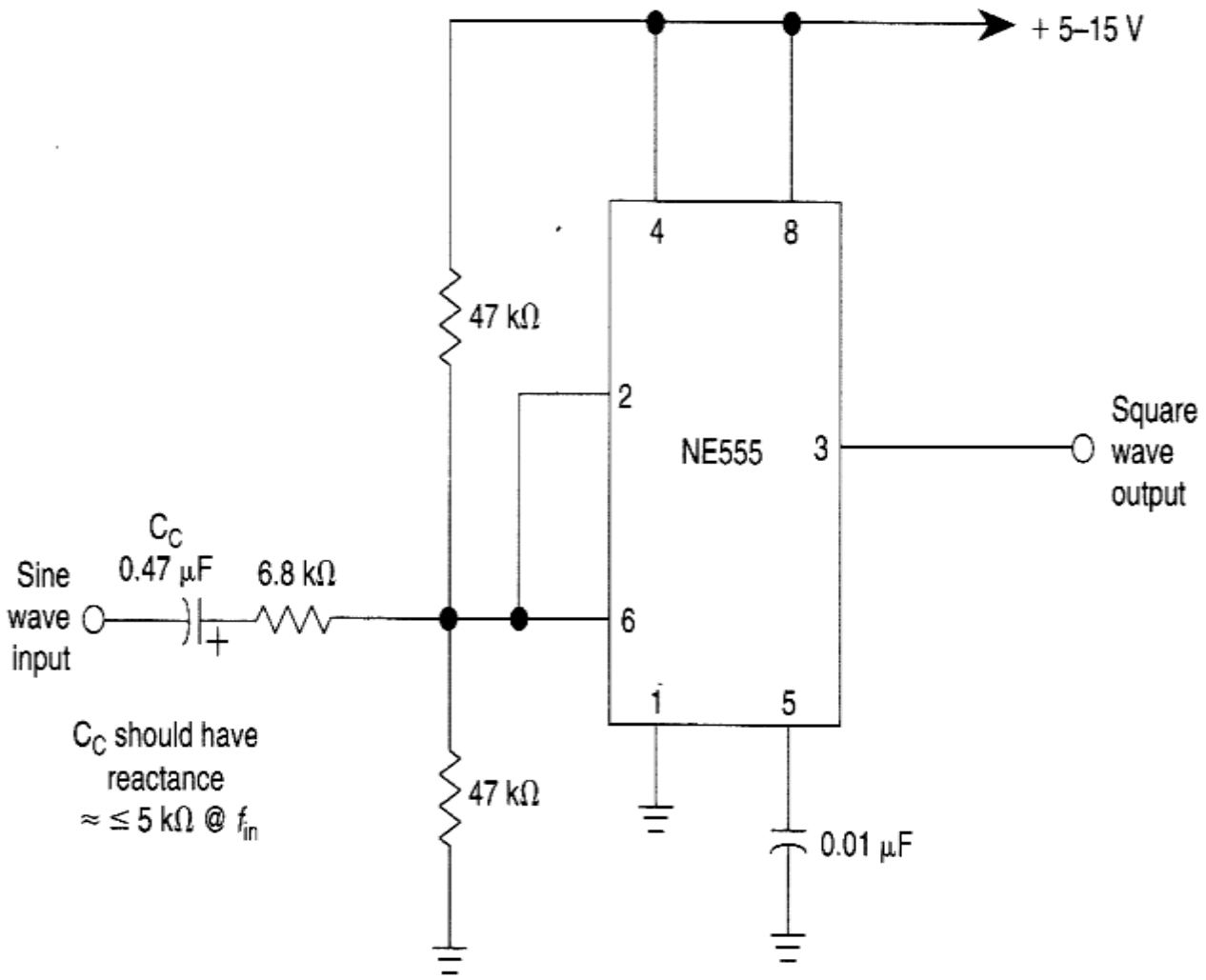
i) FSK Generator



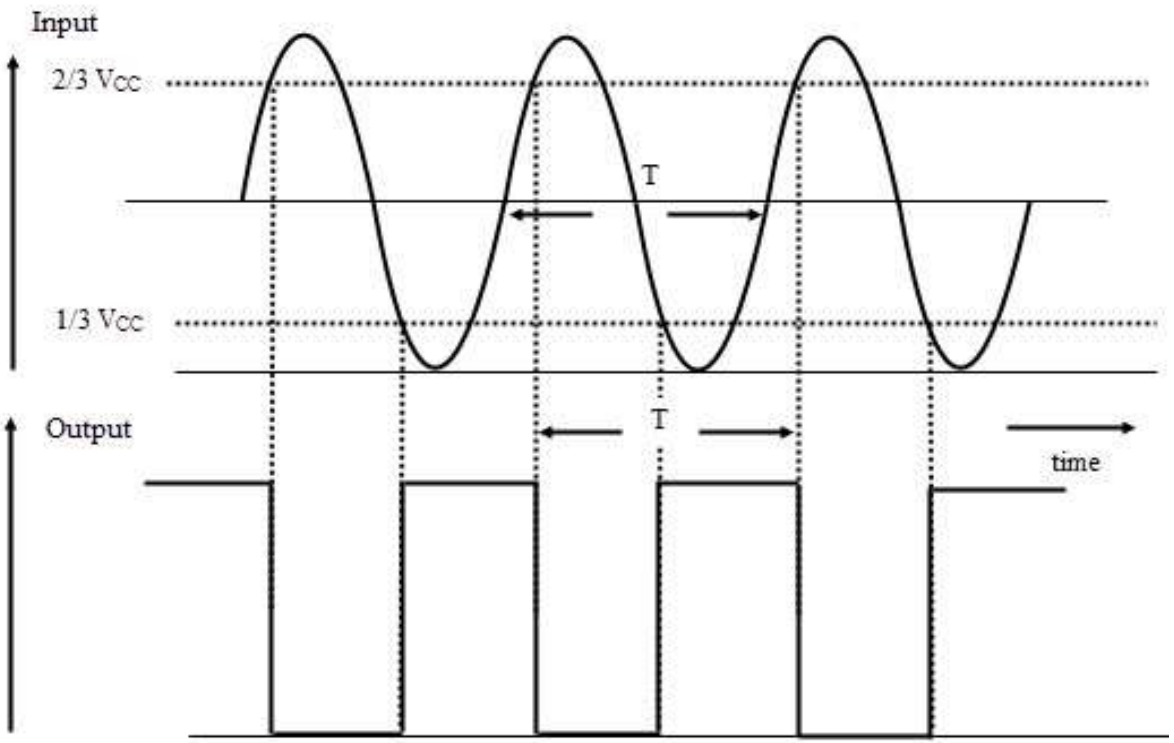
ii) Pulse Position Modulator



Schmitt Trigger using 555 IC



Input and output waveforms



Applications using 555 timer

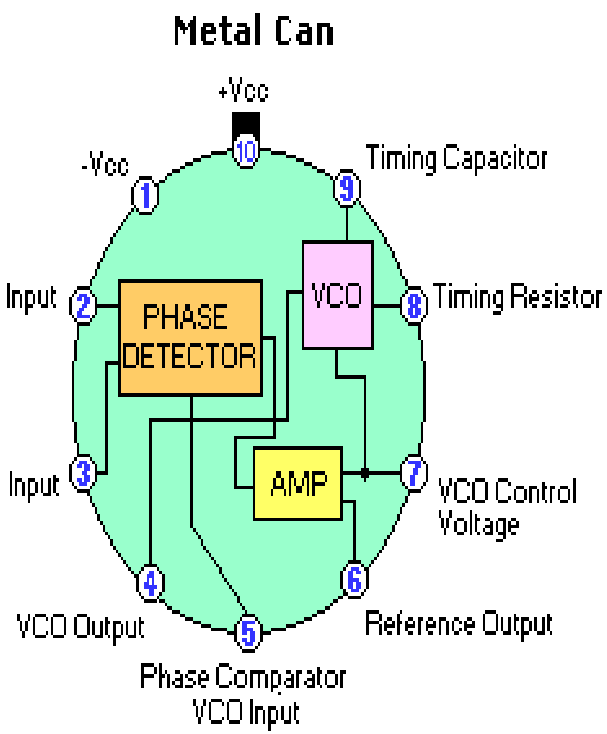
- Random Flashers
- A light dimmer
- A car tachometer
- Traffic Lights
- - Infra Red (IR) remote control

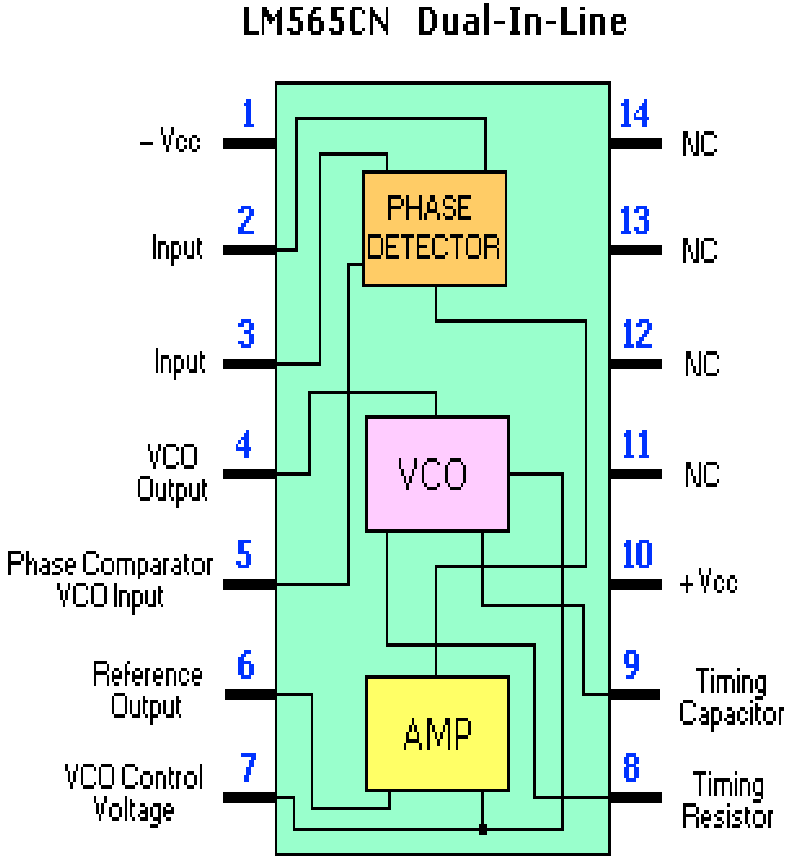
What is a PLL?

- A PLL is a negative feedback system where an oscillator-generated signal is phase and frequency locked to a reference signal.
- Analogous to a car's "cruise control"

Parts of a PLL

- Phase Detector
- Filter
- Voltage Controlled Oscillator
- Programmable Counter

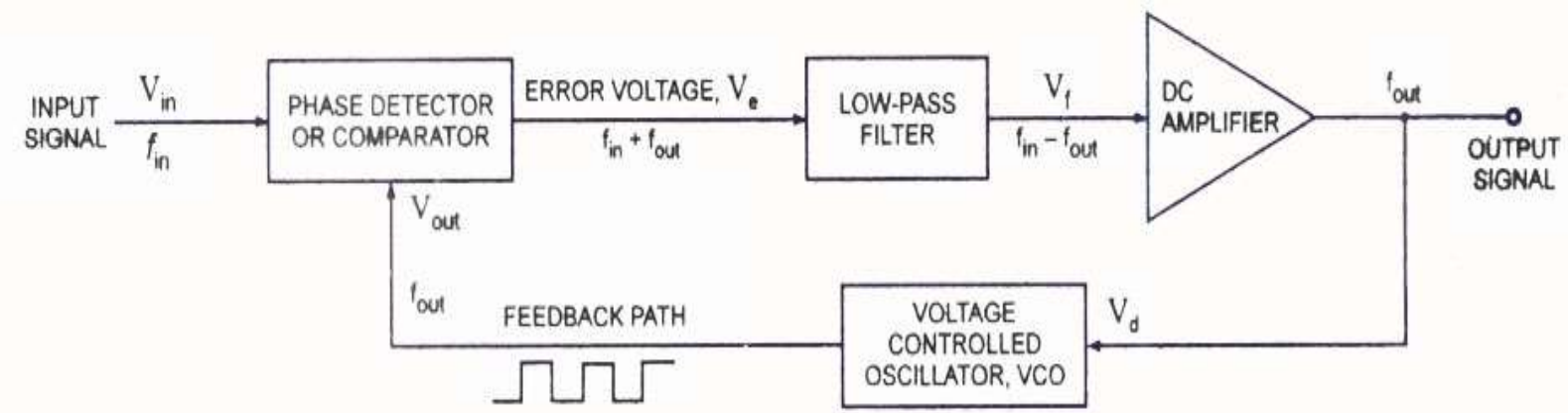

Metal Can
+Vcc
-Vcc
Timing Capacitor
Input
PHASE DETECTOR
VCO
Timing Resistor
Input
AMP
VCO Control Voltage
VCO Output
Reference Output
Phase Comparator VCO Input
LM565H or LM565CH


LM565CN Dual-In-Line
1
– Vcc
2
Input
3
Input
4
VCO Output
5
Phase Comparator VCO Input
6
Reference Output
7
VCO Control Voltage
14
NC
13
NC
12
NC
11
NC
10
+Vcc
9
Timing Capacitor
8
Timing Resistor
PHASE DETECTOR
VCO
AMP

Parts of a PLL

Phase Detector

- Acts as comparator
- Produces a voltage proportional to the phase difference between input and output signal
- Voltage becomes a control signal



Block Diagram of Basic Phase-Locked Loop (PLL)

The Voltage-Controlled Oscillator (VCO)

- Instantaneous output frequency is varied by the control voltage according to the following relation

$$\omega_o(t) = \omega_c + K_c v_c(t)$$

- The output v_o can be square wave, sine wave, or other types of periodic signal
  - For the NE565 PLL chip, it is a square wave
  - ω_c is the center or "free running" frequency of the VCO when the control voltage v_c is zero
  - K_c is a measure of the sensitivity of the VCO frequency to variations in the control voltage, called the VCO gain
- The NE565 VCO center frequency can be "tuned"

$$\omega_c = \frac{0.6\pi}{R_1 C_1}$$

The Phase Detector (PD)

- If inputs are periodic with same period, then dc component of output proportional to phase angle between inputs

$$x_{dc} = K_d \sin(\theta_i - \theta_o) = K_d \sin(\beta i$$

- is a measure of the sensitivity of the PD output to variations in the phase angle between the inputs
- This gain depends on amplitude and shape of the PD inputs
- The amplitude and the waveshape of is typically fixed, while the amplitude of may vary.
- For the NE565, if V_i is 200 mV peak-to-peak or greater, then the PD gain is constant at ~ volts/rad

$$1.4/\pi$$

- A four quadrant analog multiplier can function as a PD

The Amplified Loop Filter

- The loop filter is usually realized with external discrete components allowing ready tuning
  - Typically a passive low pass filter such as a RC lag filter
- Assume the filter transfer function G(s) is given by

$$G(s) = \frac{Vc(s)}{X(s)} = \frac{A}{(1 + \tau s)} \text{ where } \tau = R_2 C_2$$

- The purpose of the filter is to extract the dc component from the PD output $x(t)$
- In addition to a dc component, the PD output will typically contain frequencies corresponding to sums and differences of frequencies present in the PD inputs

The Amplified Loop Filter

- Normally, the lowest frequency present in the PD output (excluding dc) will be
- Thus, the 3-db cutoff frequency of the low-pass filter should be considerably below f_i so that the filter output has low ripple when in phase lock
- When the circuit is in phase lock, the input frequency . equals the output frequency f_o and the filter output voltage is constant $\mathbf{V}_c$

Maintaining Phase Lock

- If the input frequency increases slightly, the phase angle difference will increase with time
- As a result, the dc component of the phase detector output will then increase, causing the dc component of the filter output/VCO input voltage to increase
- The increasing VCO input voltage causes an increase in the VCO output frequency, i.e., causing the output frequency to match the new input frequency
- The phase angle thus stabilizes at a new equilibrium, and phase lock is maintained
- In phase lock, the control circuit, i.e., the PD, amplifier, and filter, continuously adjust the VCO frequency to match the input frequency

The Lock Range

- The lock range specifies frequency limits beyond which a “locked” loop will become “unlocked,” i.e., the output frequency will no longer track the input frequency
- For the NE565 chip, the loop gain depends on both the center frequency and the differential supply voltage
- To determine the lock range experimentally:
  - Apply a periodic input of sufficient amplitude and frequency to attain a phase lock.
  - Slowly increase/decrease the input frequency until the locked condition is lost

The Capture Range

- The range of frequencies over which an unlocked loop will always become locked is called the capture range
  - A simple approximation for the capture range
- The capture range can be controlled by varying the pole location of the loop filter (can’t exceed the lock range)
- In order to determine the capture range experimentally
  - Start out with an unlocked loop and very slowly increase or decrease the input in such a way that it approaches the center frequency of the VCO
  - The instant the loop becomes locked, the boundary of the capture range has been crossed

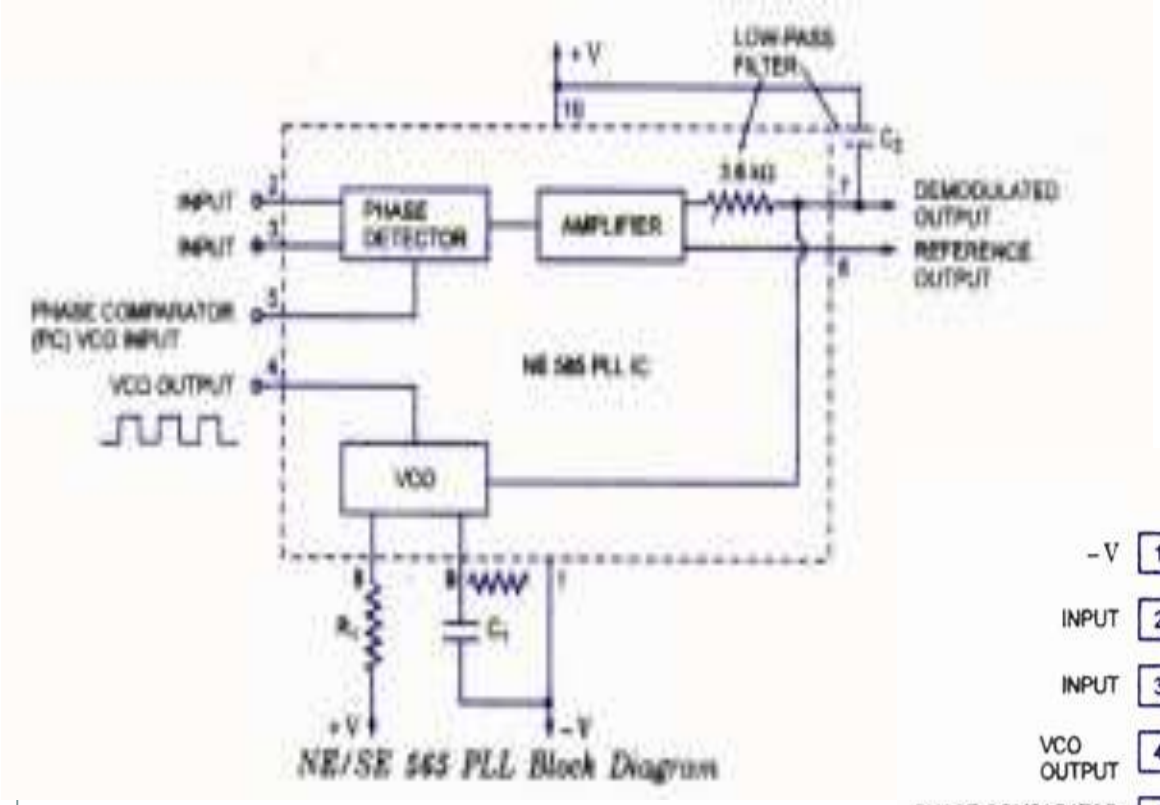
Voltage controlled oscillator

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage

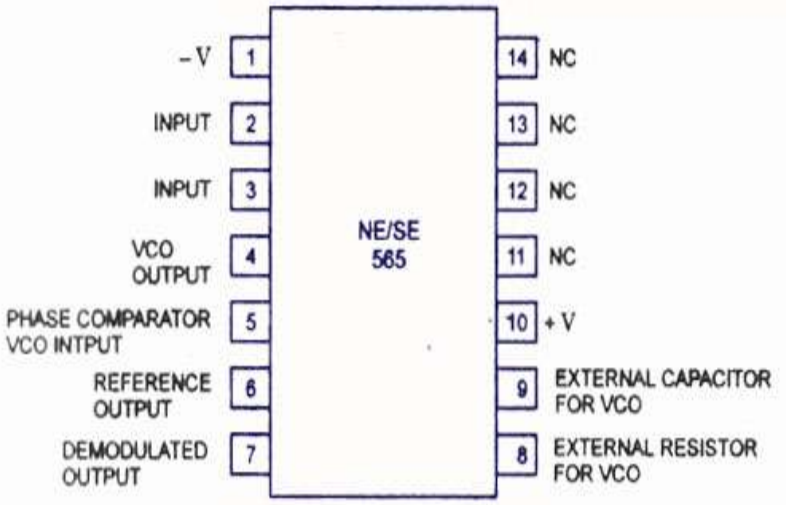
The features of 566 VCO

1. Wide supply voltage range(10- 24V)
2. Very linear modulation characteristics
3. High temperature stability

NE/SE PLL Block diagram



NE/SE 565 PLL Block Diagram



14-Pin DIP Package

Phase Lock Looped

A PLL is a basically a closed loop system designed to lock output frequency and phase to the frequency and phase of an input signal

Applications of 565 PLL

1. Frequency multiplier
2. Frequency synthesizer
3. FM detector

Characteristics of SE/NE 565 PLL IC

Operating frequency range : 0.001 Hz to 500 kHz.

Operating voltage range : ± 6 to ± 12 V.

Input impedance : 10 k Q typically.

Output sink current :1mA typically.

Output source current : 10 m A typically.

Drift in VCO centre frequency with temperature : 300 ppm/ °C typically.

Drift in VCO centre frequency with supply voltage : 1.5 %/V maximum.

Input level required for tracking : 10 mV_{rms} minimum to 3 V peak-to-peak maximum.

Bandwidth adjustment range : < ± 1 to > ± 60 %.

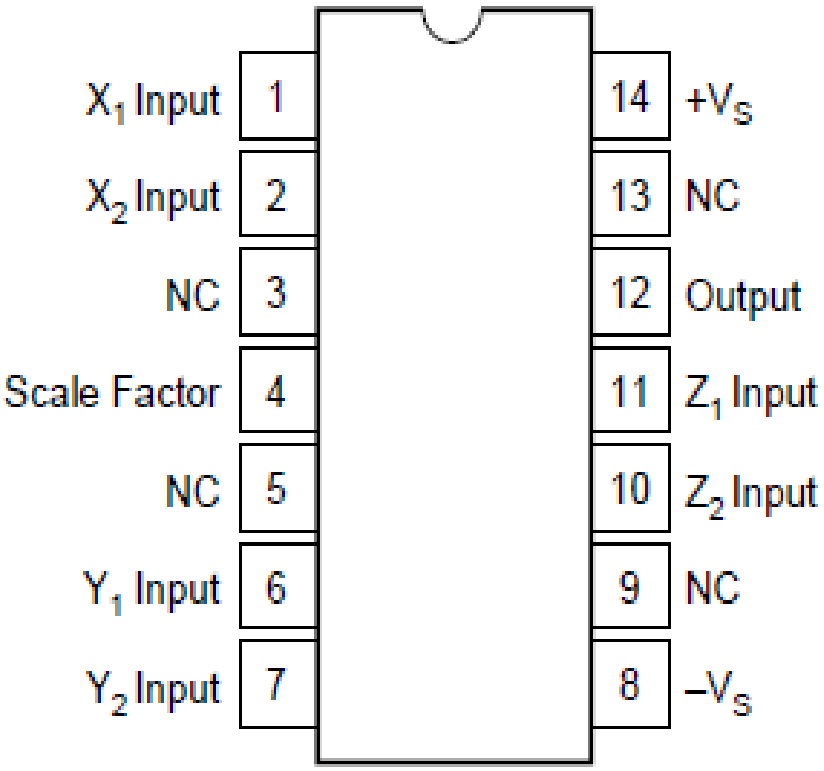
MPY 634 IC

The MPY634 is a wide bandwidth, high accuracy, four-quadrant analog multiplier. Its accurately laser-trimmed multiplier characteristics make it easy to use in a wide variety of applications with a minimum of external parts, often eliminating all external trimming. Its differential X, Y, and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter, and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows signal processing at IF, RF, and video frequencies. The internal output amplifier of the MPY634 reduces design complexity compared to other high frequency multipliers and balanced modulator circuits. It is capable of performing frequency mixing, balanced modulation, and demodulation with excellent carrier rejection.

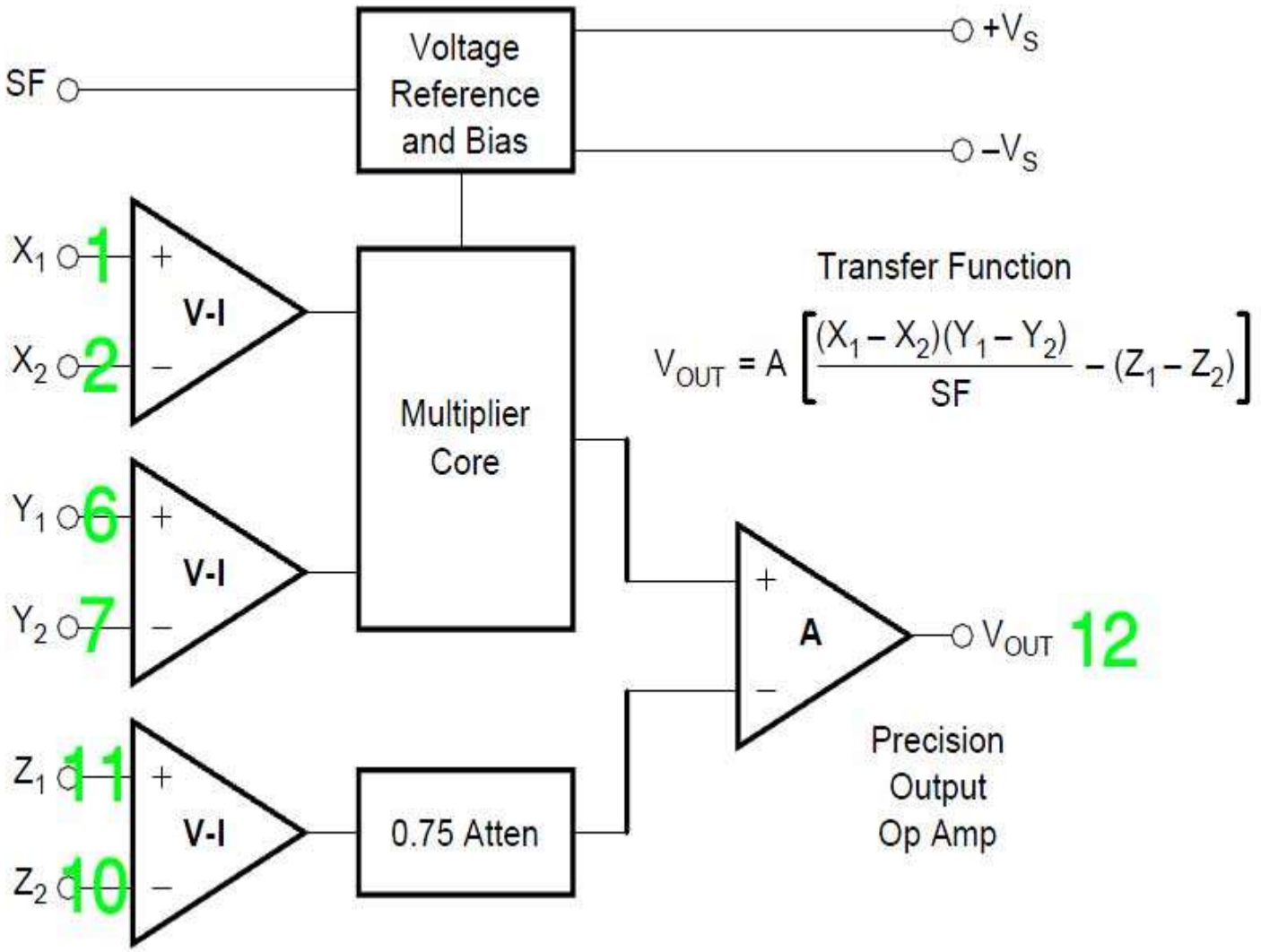
An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user-selected scale factors from 0.1 to 10 using external feedback resistors.

PIN CONFIGURATION



DIP: MPY634KP

IC MODEL


Voltage Reference and Bias
SF
+VS
–VS
X1
1
X2
2
V-I
Y1
6
Y2
7
V-I
Z1
11
Z2
10
V-I
Multiplier Core
0.75 Atten
A
VOUT
12
Precision Output Op Amp
Transfer Function
VOUT = A [(X1 – X2)(Y1 – Y2) / SF – (Z1 – Z2)]

FEATURES &APPLICATIONS

FEATURES

WIDE BANDWIDTH: 10mhz typ
±0.5% max four-quadrant accuracy
Internal wide-bandwidth op amp
Easy to use
Low cost

APPLICATIONS

Precision analog signal processing
Modulation and demodulation
Voltage-controlled amplifiers
Video signal processing
Voltage-controlled filters and oscillators

UNIT-V
A/D & D/A CONVERTERS

Analog Signals

Analog signals – directly measurable quantities in terms of some other quantity

Examples:

- Thermometer – mercury height rises as temperature rises
- Car Speedometer – Needle moves farther right as you accelerate
- Stereo – Volume increases as you turn the knob.

Examples of A/D Applications

- Microphones - take your voice varying pressure waves in the air and convert them into varying electrical signals
- Strain Gages - determines the amount of strain (change in dimensions) when a stress is applied
- Thermocouple – temperature measuring device converts thermal energy to electric energy
- Voltmeters
- Digital Multi meters

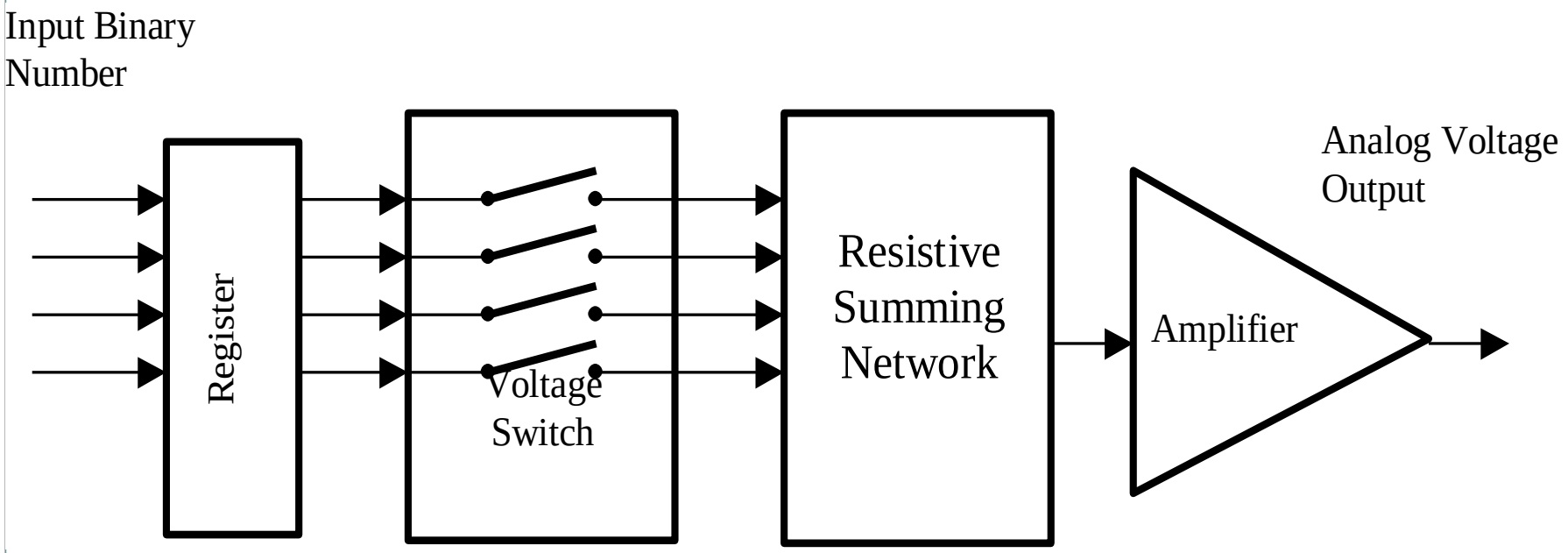
1. DAC

In an electronic circuit, a combination of high voltage (+5V) and low voltage (0V) is usually used to represent a binary number. For example, a binary number 1010 is represented by

Weighting	2^3	2^2	2^1	2^0
Binary Digit	1	0	1	0
State	+5V	0V	+5V	0V

DACs are electronic circuits that convert digital, (usually binary) signals (for example, 1000100) to analog electrical quantities (usually voltage) directly related to the digitally encoded input number.

DACs are used in many other applications, such as voice synthesizers, automatic test system, and process control actuator. In addition, they allow computers to communicate with the real (analog) world.



Register: Use to store the digital input (let it remain a constant value) during the conversion period.

Voltage: Similar to an ON/OFF switch. It is ‘closed’ when the input is ‘1’. It is ‘opened’ when the input is ‘0’.

Resistive Summing Network: Summation of the voltages according to different weighting.

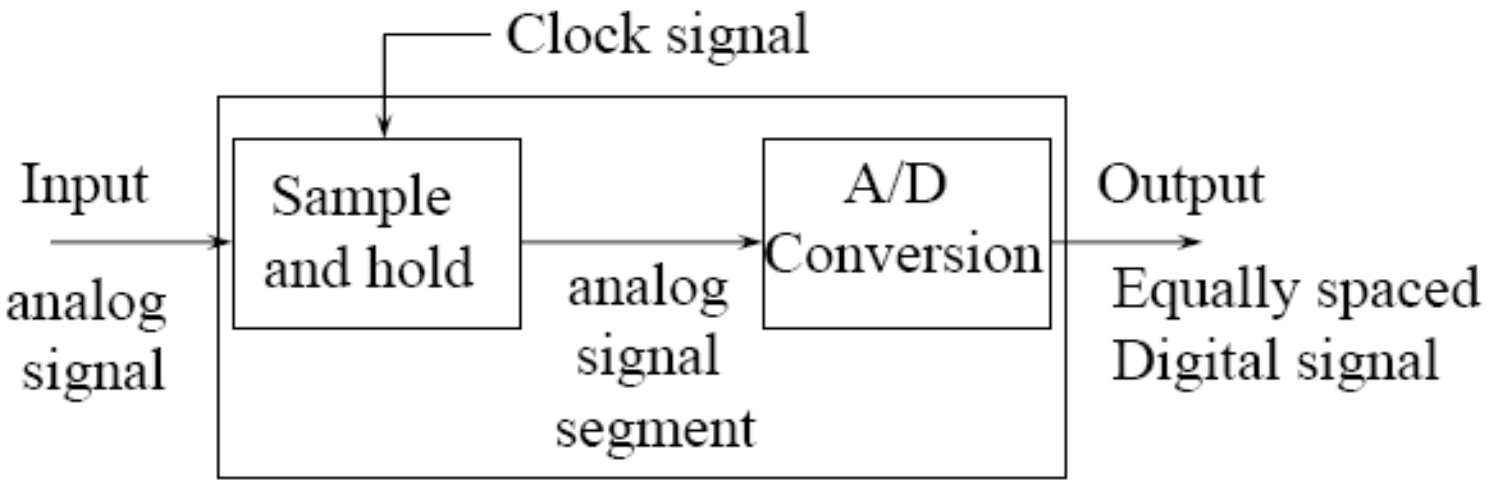
Amplifier: Amplification of the analog according to a pre-determined output voltage range. For example, an operation amplifier

The two most popular types of resistive summing networks are:

- Weighted binary resistance type, and
- Ladder resistance (R-2R) type

Just what does an A/D converter DO?

- Converts analog signals into binary words



Analog → Digital Conversion
2-Step Process:

- Quantizing - breaking down analog value is a set of finite states
- Encoding - assigning a digital word or number to each state and matching it to the input signal

Classification of ADCs

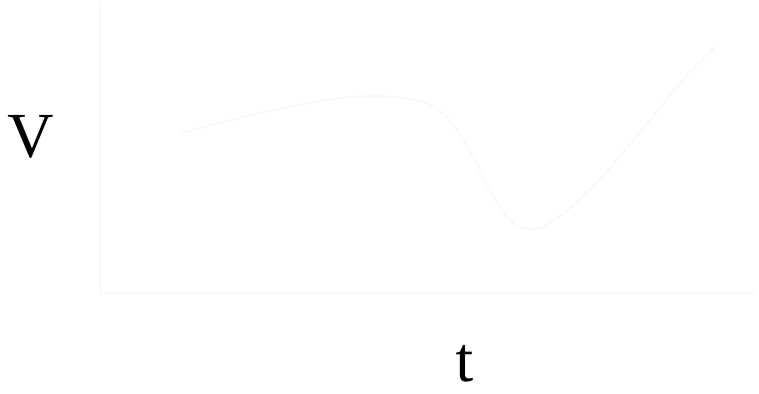
1. Direct type ADC.
2. Integrating type ADC

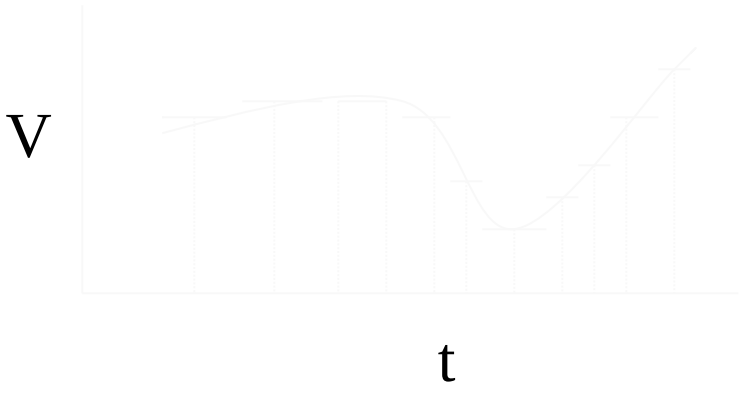
Direct type ADCs

1. Flash (comparator) type converter
2. Counter type converter
3. Tracking or servo converter.
4. Successive approximation type converter

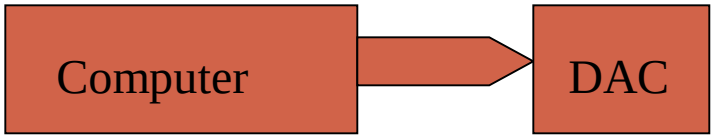
Real world (lab) is analog

Computer (binary) is digital

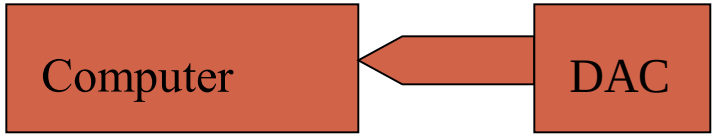




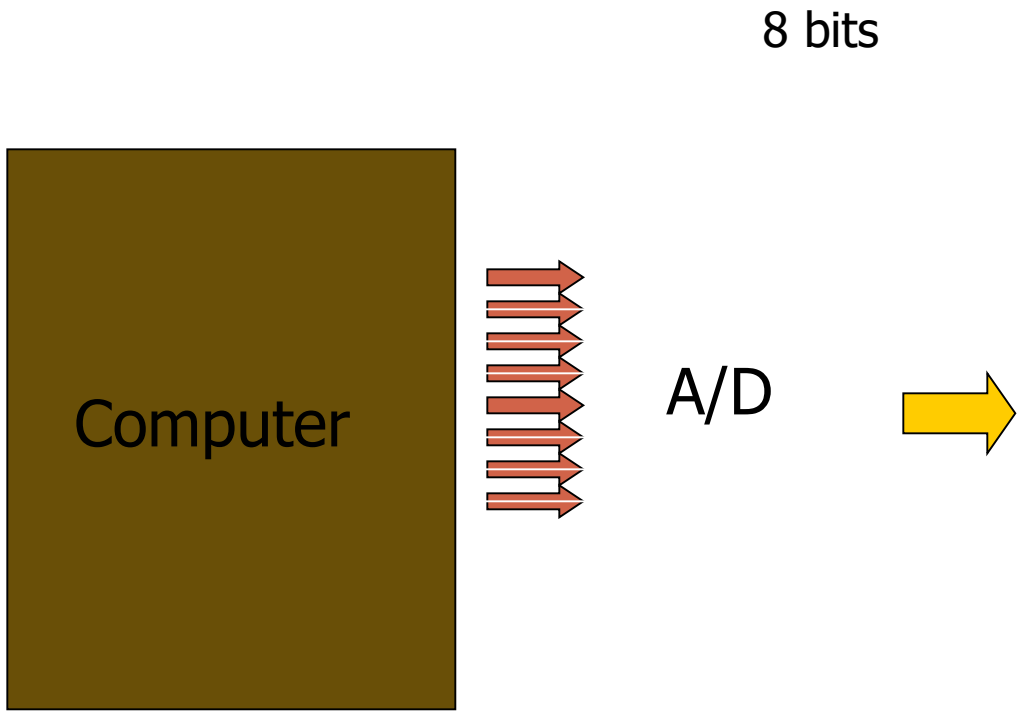
D/A Conversion



A/D Conversion



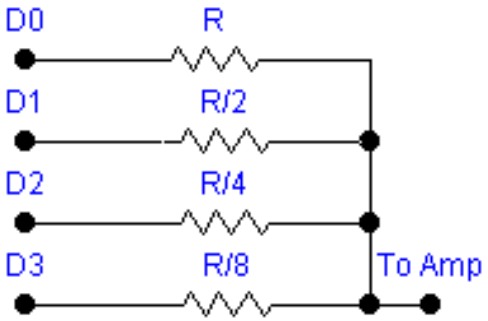
Digital to Analog Conversion (DAC or D/A)



Digital to Analog conversion involves transforming the computer's binary output in 0's and 1's (1's typically = 5.0 volts) into an analog representation of the binary data

D/A conversion can be as simple as a weighted resistor network

4 - bit DAC Converter



Resistor values correspond to binary weights of the number D_3 D_2 D_1 D_0 , i.e. 1/8, 1/4, 1/2, and 1

Using EWB we can model this device

Difficulties:

1. This setup requires a wide range of precision resistors

   A 10 bit DAC needs resistors ranging from R to R/1024.

2. The circuit driving the DAC (usually a computer) must supply a wide range of currents for a constant V_{out}

As was seen in the Workbench example, the output voltage from a DAC can change by only discrete amounts, corresponding to the level associated with a 1 bit binary change.

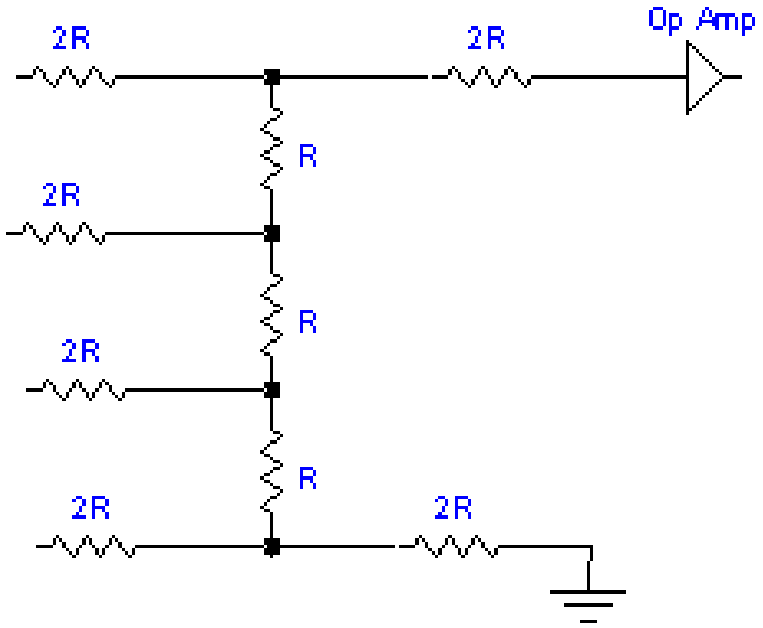
For a 8-bit DAC

Smallest step in output voltage is v/256

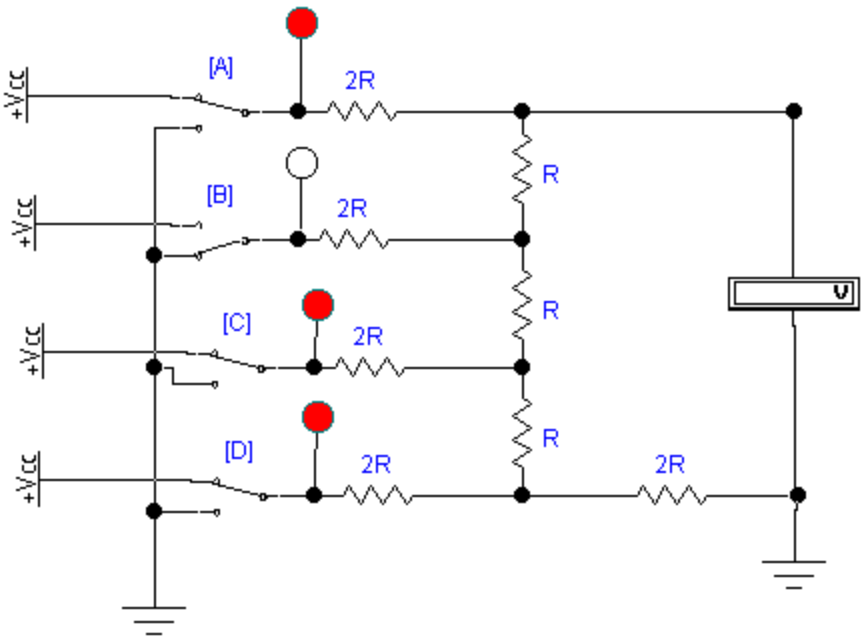
8 bits corresponds to 256 different values

For a 5.0 volt DAC this step size is ~ 19.5 mV

A modification of the weighted resistor DAC is the so called R-2R LADDER DAC, that uses only 2 different resistances



An actual R-2R DAC showing input 1 0 1 1



Voltmeter reading is determined by the binary number ABCD and the resistor weights

MSB = 1/2 of V_{ref}

= 1/4 of V_{ref}

= 1/8 of V_{ref}

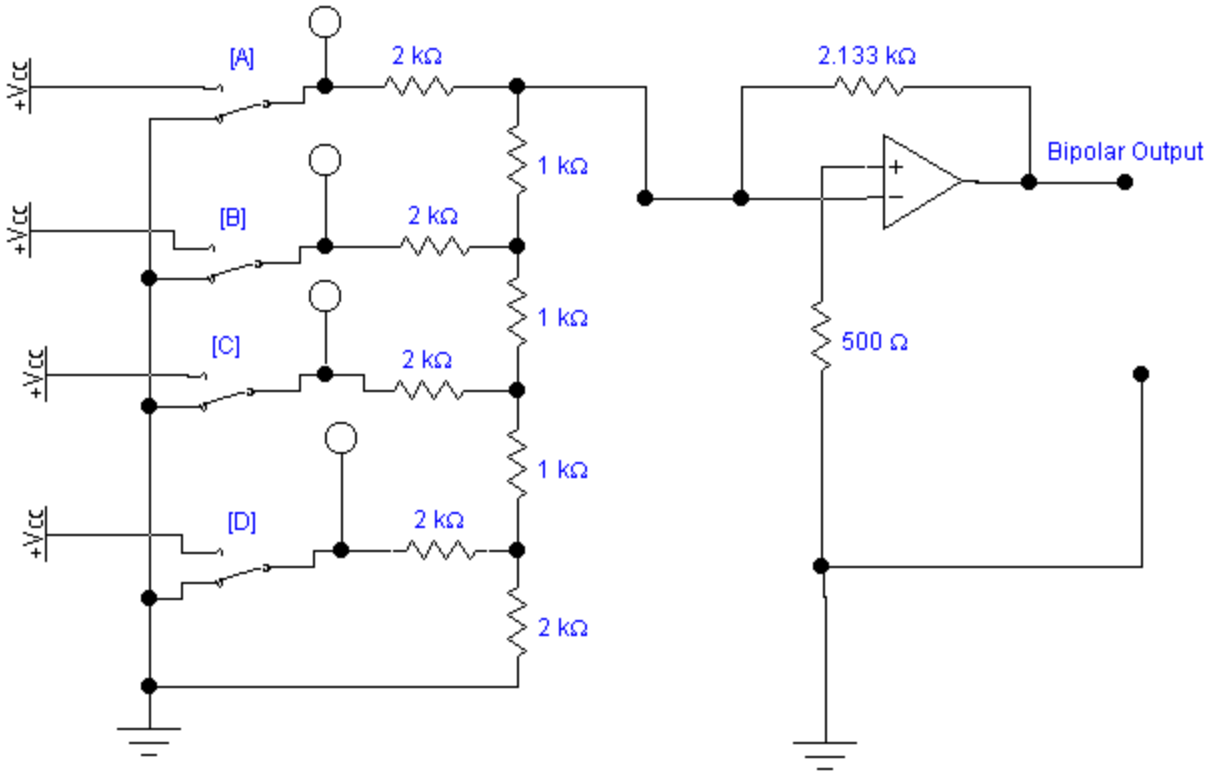
LSB = 1/16 of V_{ref}

1 0 1 1 = 1/2 (5) + 1/4 (0) + 1/8 (5) + 1/16 (5)

$\cong$ 3.4 volts

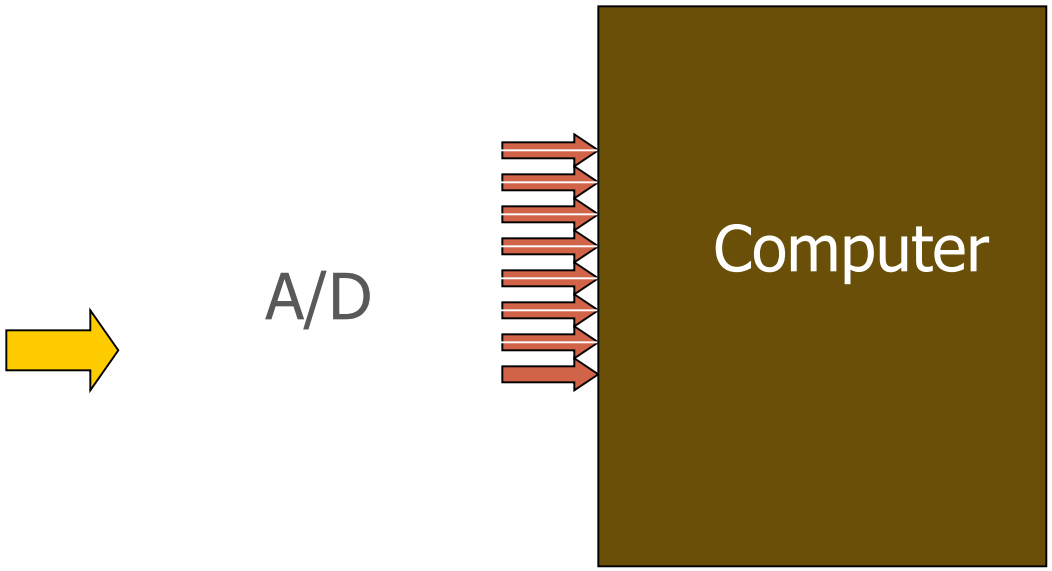
In actual DACs, the converters will drive amplifier circuits in most cases

Amplified DAC with bipolar (± V_{out}) output



r2rdac.ewb

Analog-to Digital Conversion (ADC or A/D)



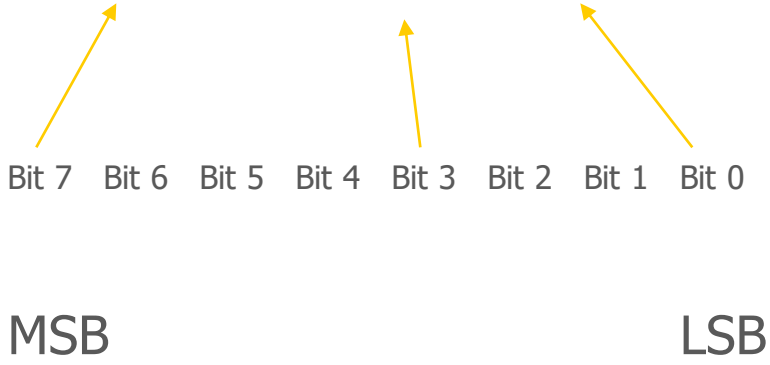
An ideal A/D converter takes an input analog voltage and converts it to a perfectly linear digital representation of the analog signal

If you are using an 8-bit converter, the binary representation is 8-bit binary number which can take on 2^8 or 256 different values. If your voltage range were 0 - 5 volts, then

0 VOLTS	0000 0000
5 VOLTS	1111 1111

An 8-bit converter can represent a voltage to within one part in 256, or about 0.25 %. This corresponds to an inherent uncertainty of ± ½ LSB (least significant bit).

Decimal 128 = 0 1 1 1 1 1 1 1



Notice the bits are designated B7 - B0. Bit B7 is the Most Significant Bit while B0 is the Least Significant Bit

Analog Voltage

1 LSB

Voltage (Volts)

00000000

00000001

00000010

00000011

. . . . . .

11111100

11111101

11111110

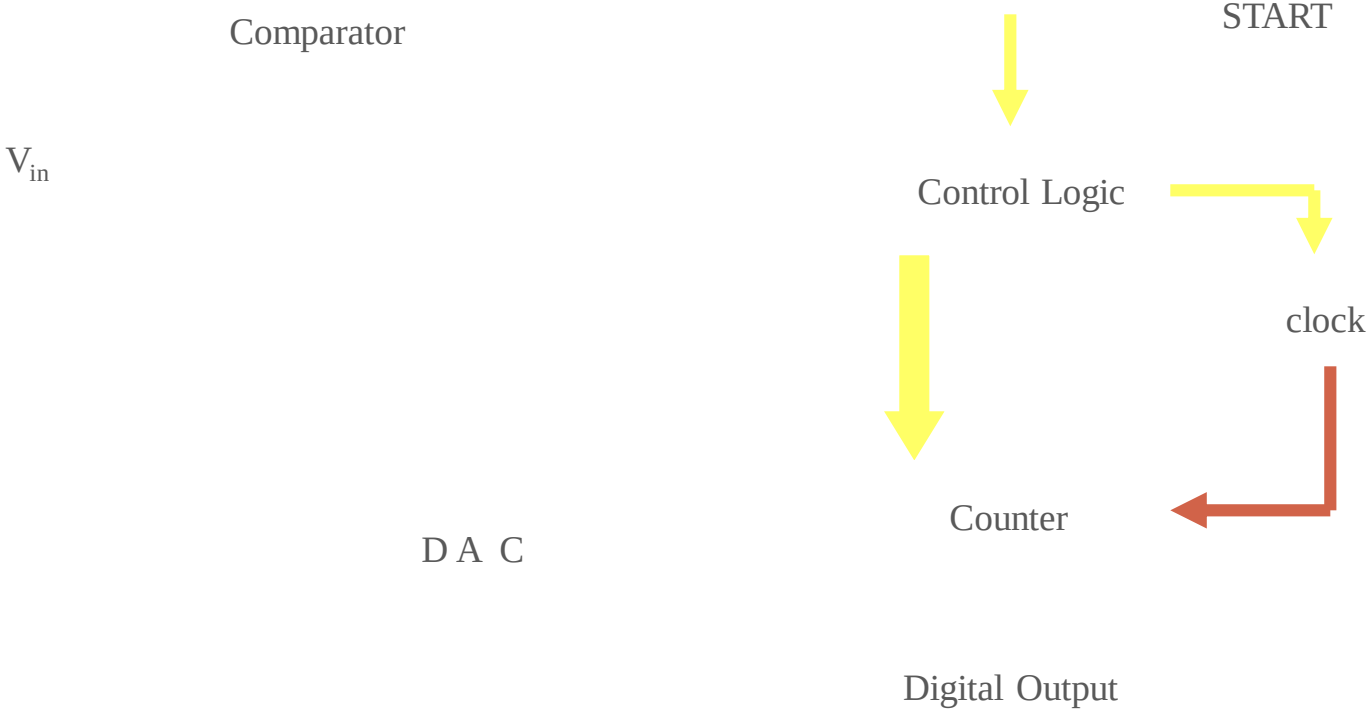
11111111

Number of Bits (N)	Resolution ($1/2^N$)	Increment (mV) for 5 volts
6	1/64	78.1
8	1/256	19.6
10	1/1024	4.9
12	1/4096	1.2
14	1/16384	0.3
16	1/65536	0.07

Types of Analog to Digital Converters

1. Counter Type
2. Integrating or Dual Slope
3. Parallel or Flash
4. Successive Approximation

Counter Type

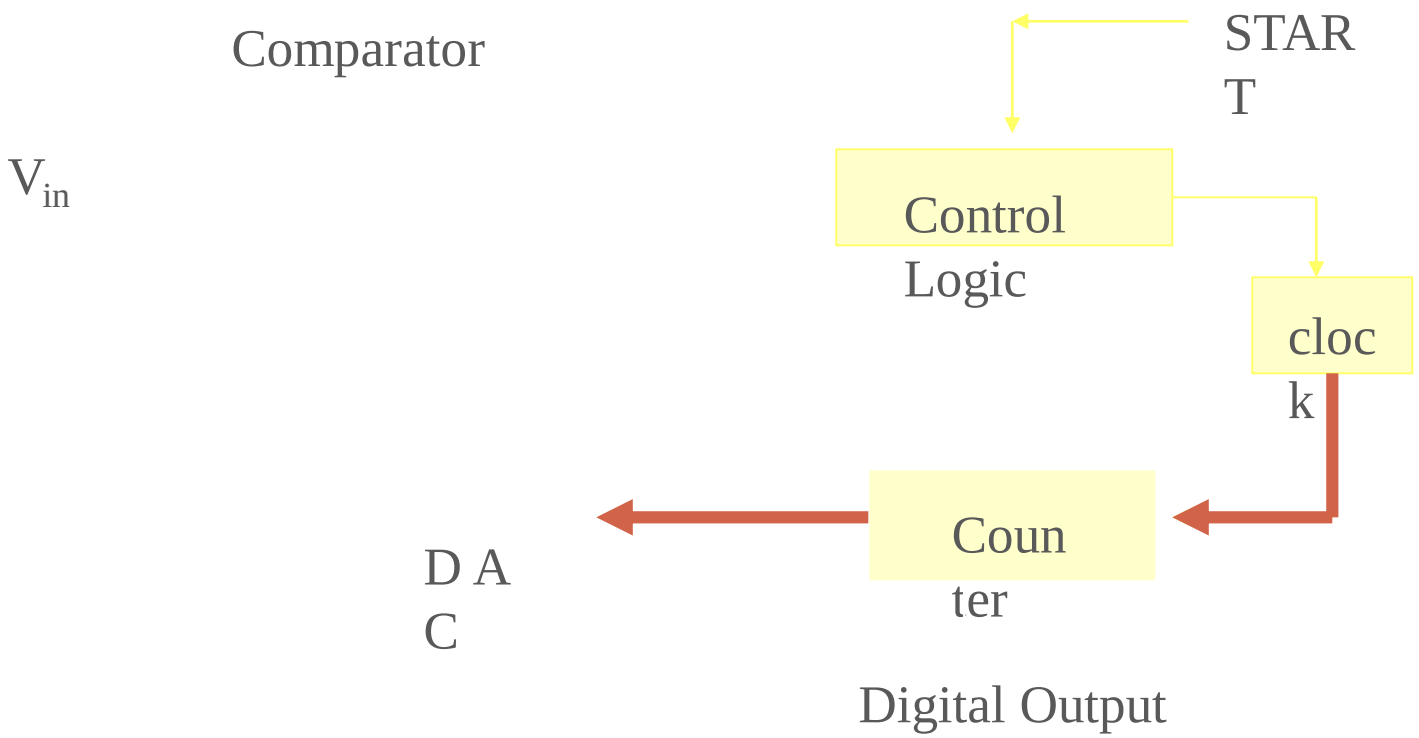


•When START is received,

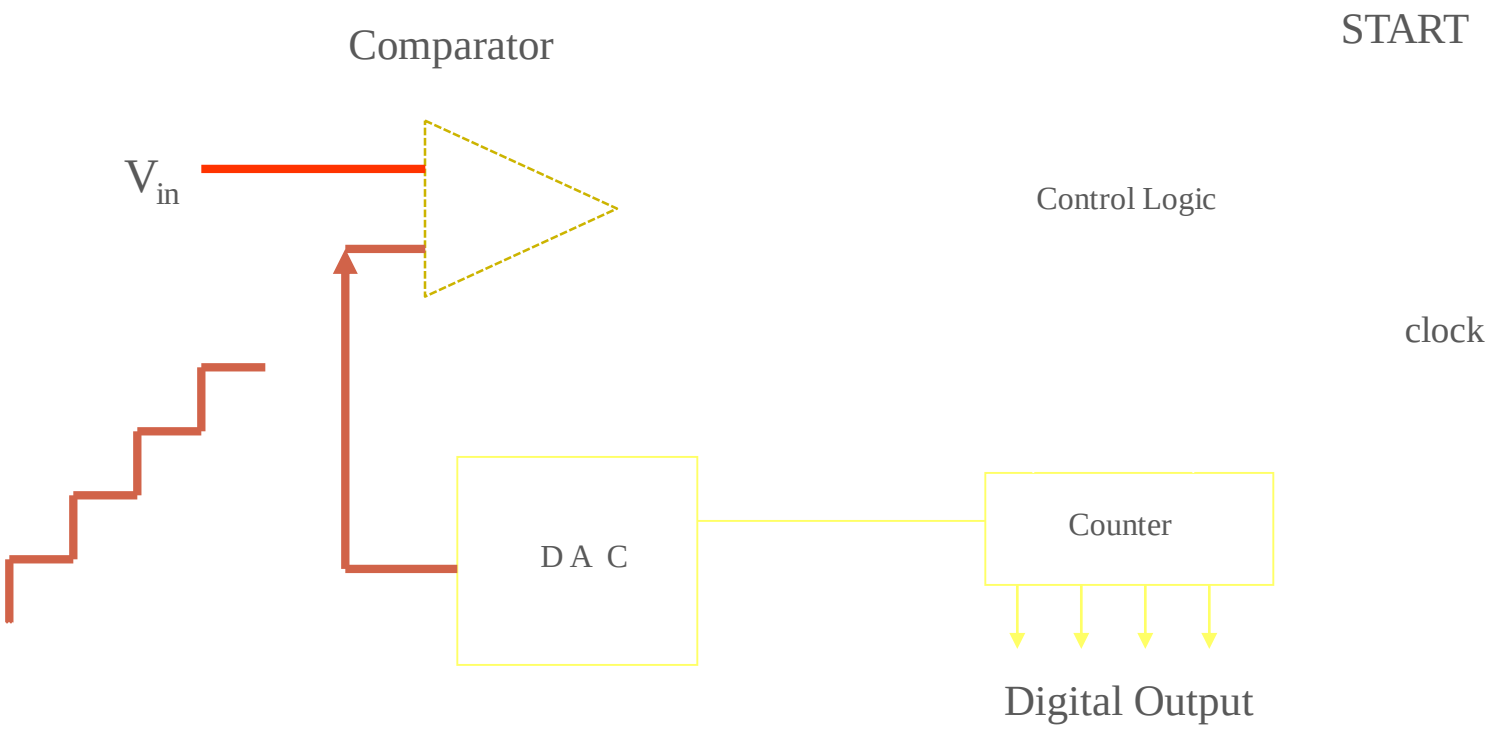
•control logic initializes the system, (sets counter to 0), and

•turns on Clock sending regular pulses to the counter.

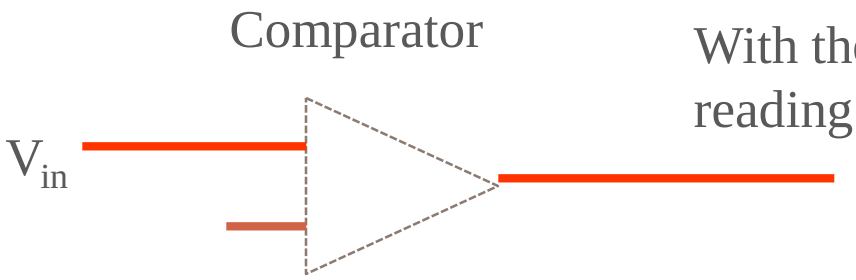
As the Clock sends regular pulses to the counter, the counter outputs a digital signal to the Digital-to-Analog converter



As the ramp voltage increases to the comparator, it rises closer and closer to V_{in} at which point the comparator shifts states

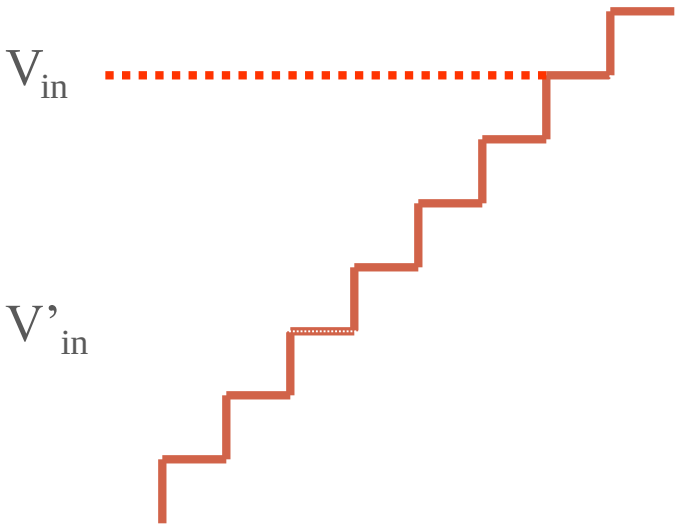


When the ramp voltage exceeds V_{in} , the comparator output shifts which signals the control logic to turn off the clock



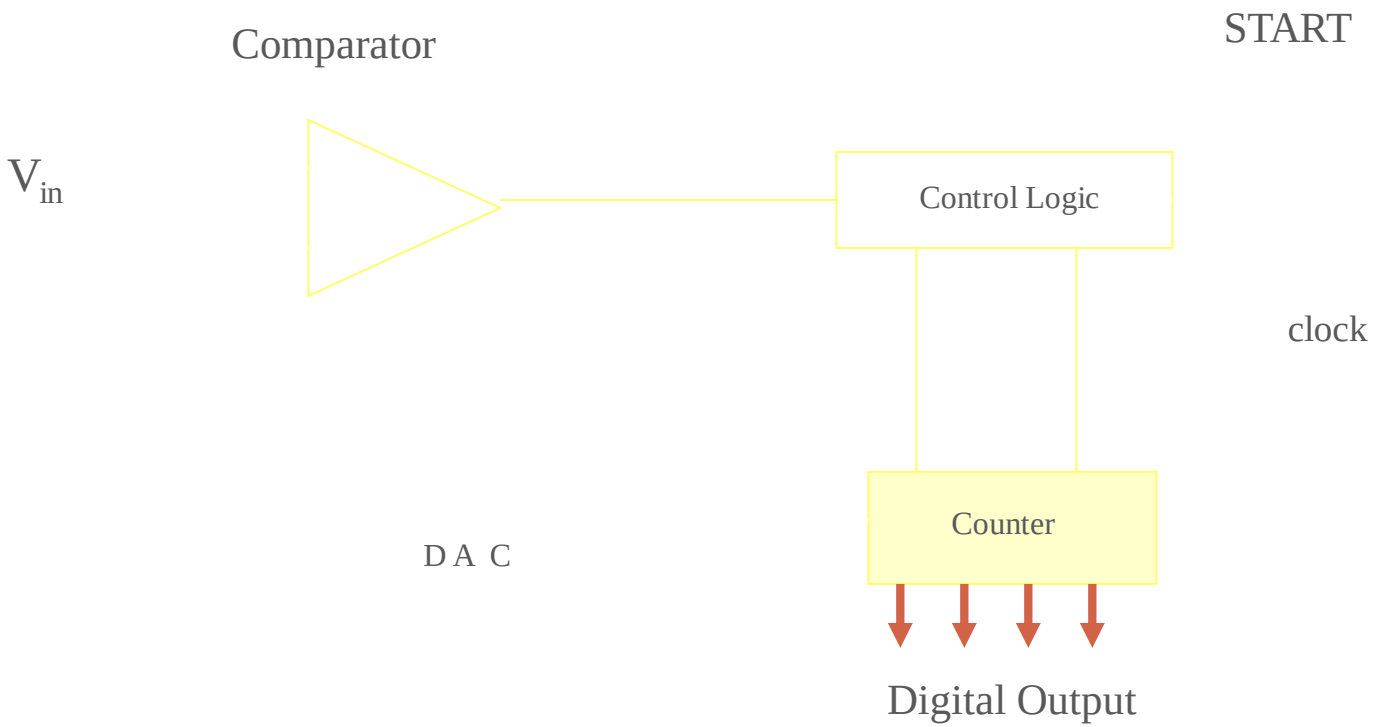
With the clock off, the counter reading is proportional to V_{in}

Note that the conversion time depends on the size of the input signal



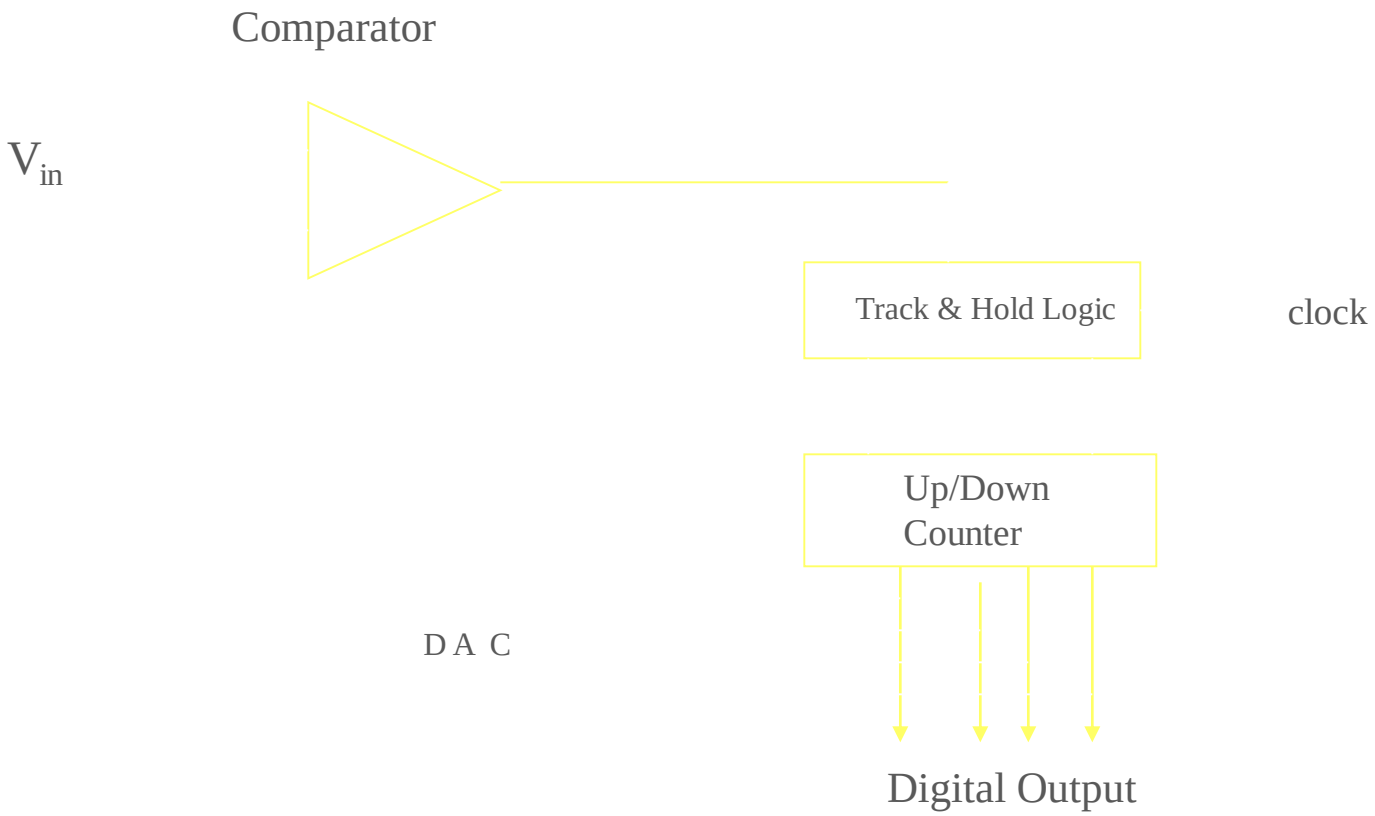
Conversion time Conv.time

Once the digital output has been read by the associated circuitry, a new start signal is sent, repeating the cycle.

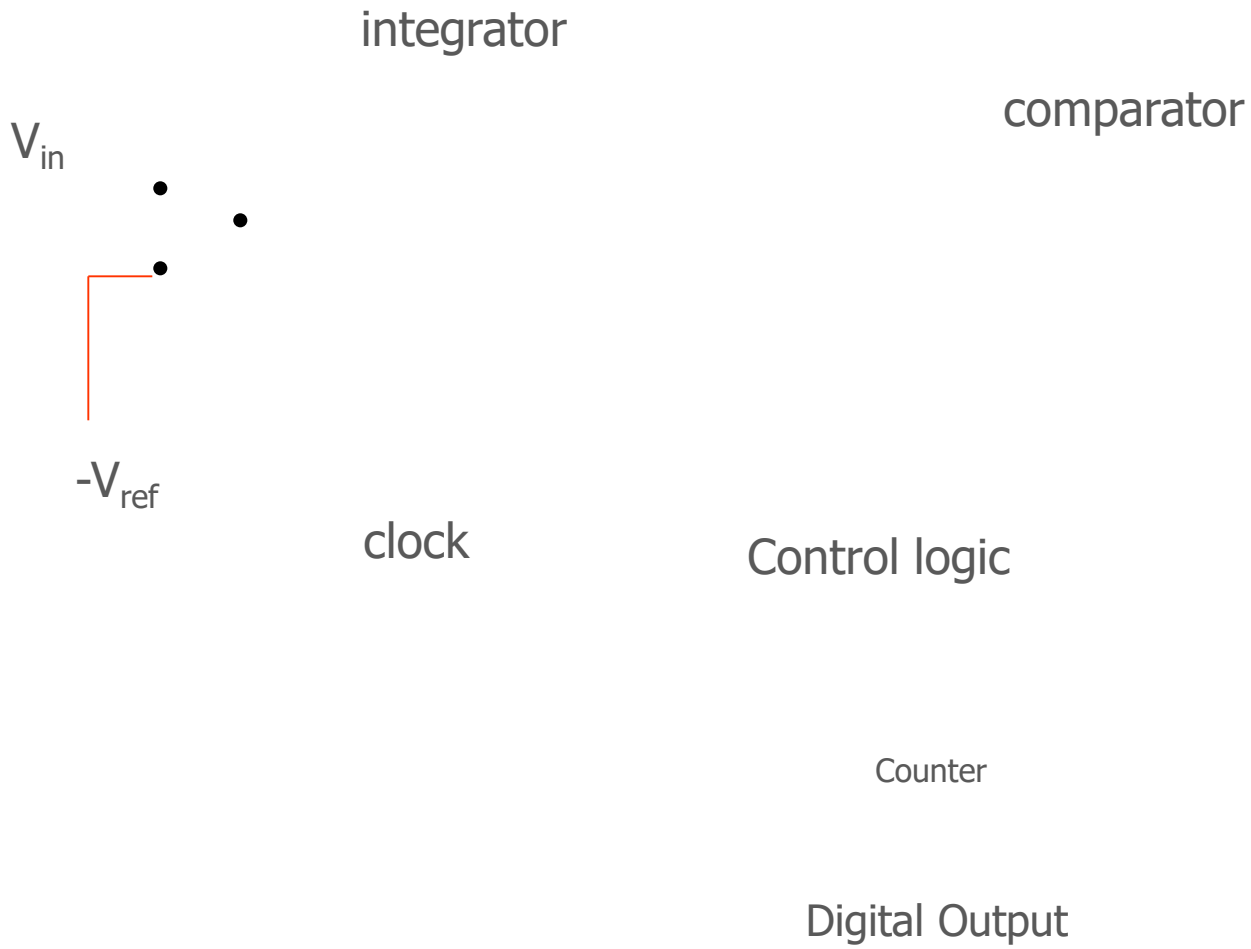


With a counter type A/D, if the signal is varying rapidly, the counter must count up and reset before each cycle can begin, making it difficult to follow the signal.

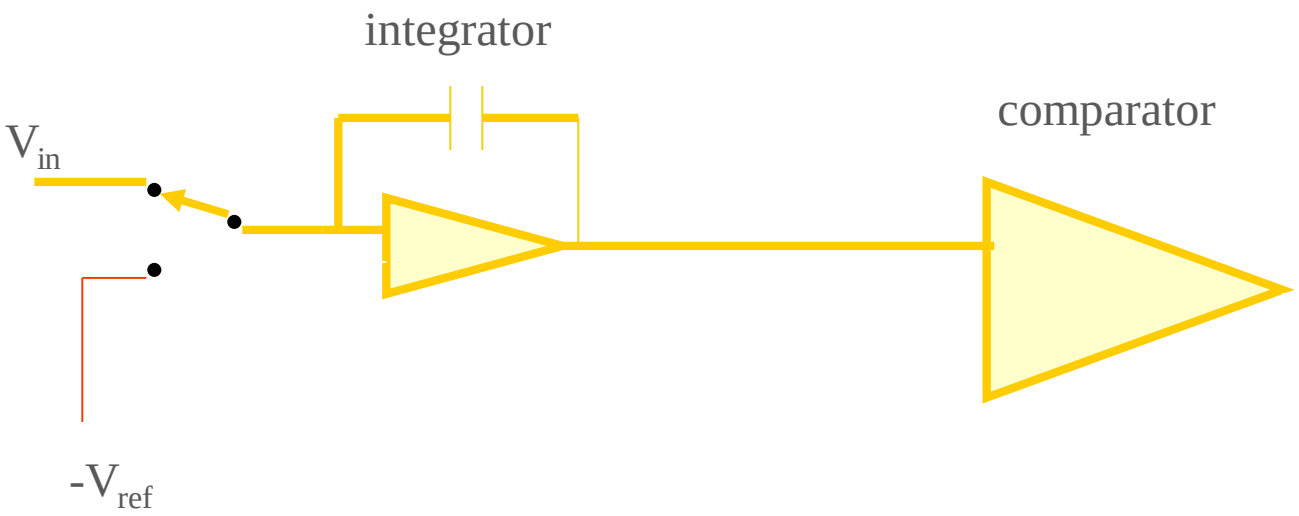
Tracking ADC - similar to the counter type except it uses an up/down counter and can track a varying signal more quickly



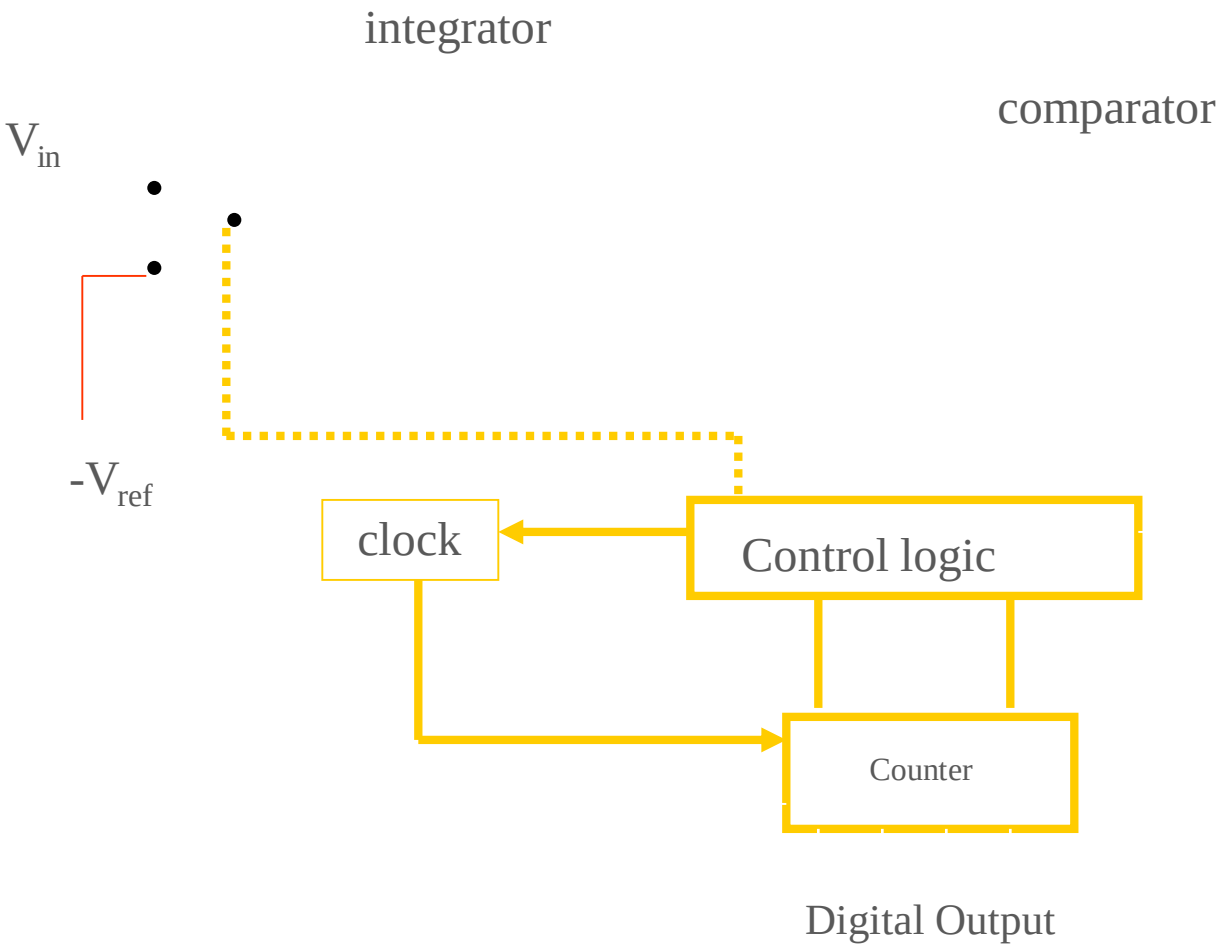
Integrating or Dual Slope A/D



When conversion is initialized, the switch is connected to V_{in} which is applied to the op amp integrator. The integrator output (>0) is applied to the comparator

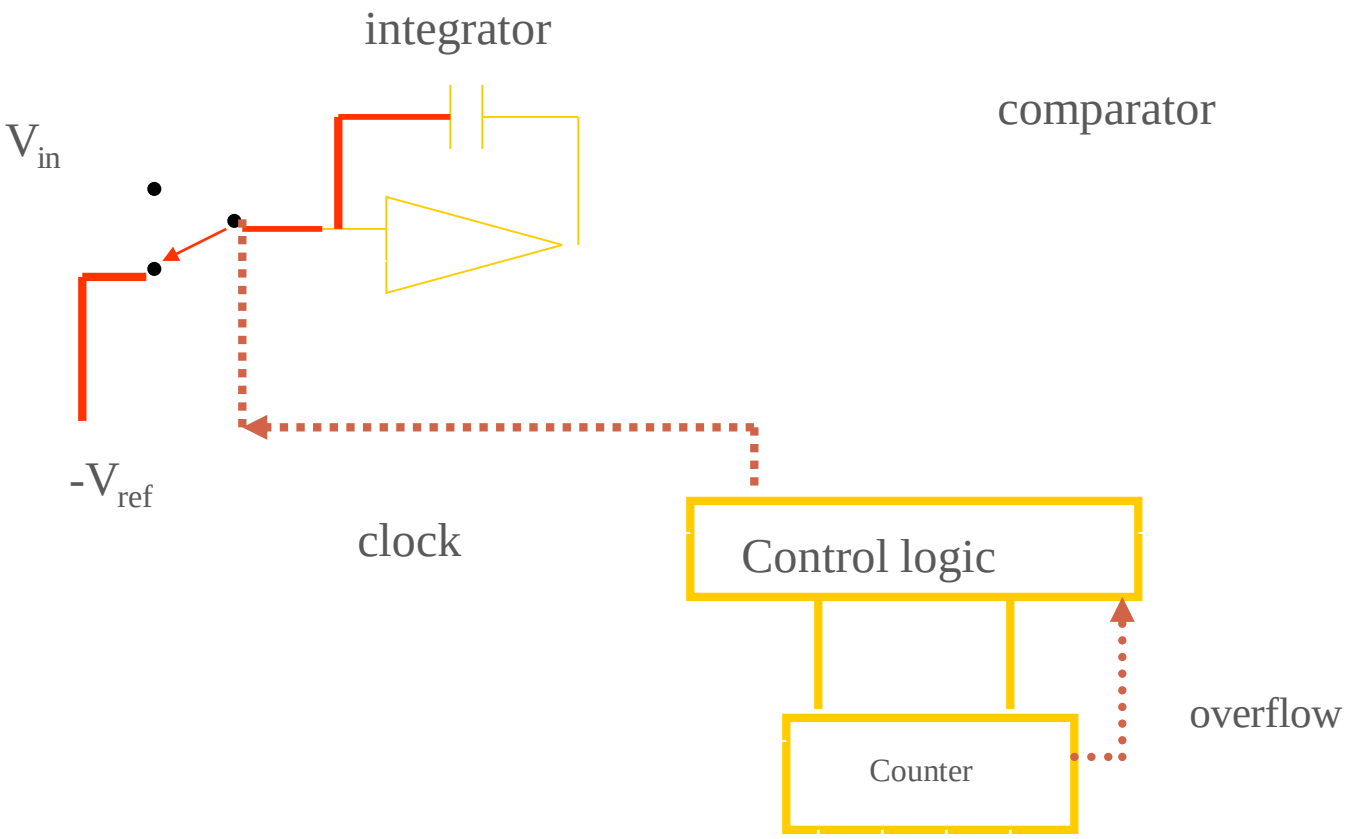


As conversion is initiated, the control logic enables the clock which then sends pulses to the counter until the counter fills (9999)



As the counter resets (9999 → 0000), an overflow signal is sent to the control logic

this activates the input switch from V_{in} to $-V_{ref}$, applying a negative reference voltage to the integrator

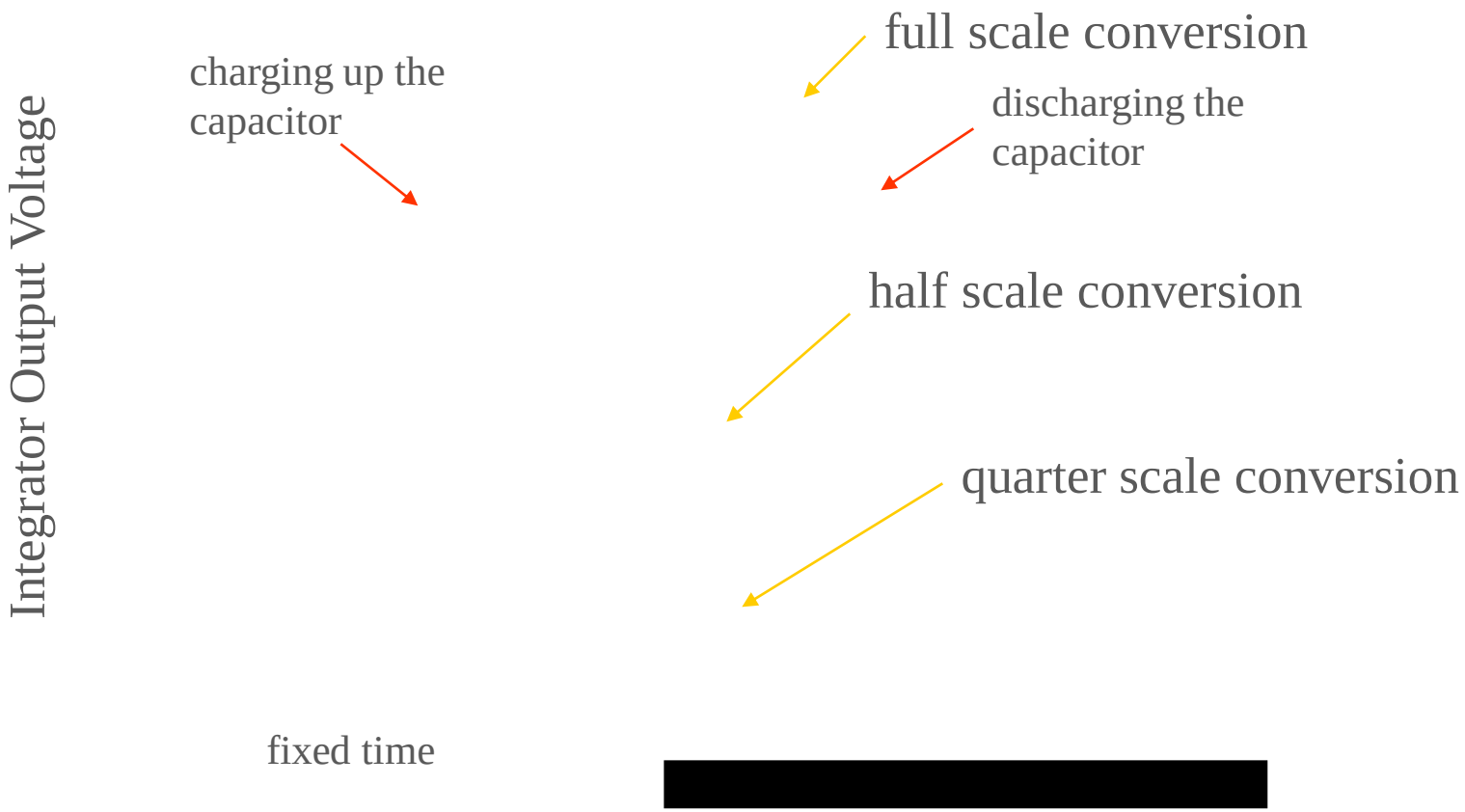


The negative reference voltage removes the charge stored in the integrator until the charge becomes zero.

At this point, the comparator switches states producing a signal that disables the clock and freezes the counter reading.

The total number of counts on the counter (determined by the time it took the fixed voltage V_{ref} to cancel V_{in}) is proportional to the input voltage, and thus is a measure of the unknown input voltage.

The operation of this A/D requires 2 voltage slopes, hence the common name DUAL-SLOPE.



Since this A/D integrates the input as part of the measuring process, any random noise present in the signal will tend to integrate to zero, resulting in a reduction in noise.

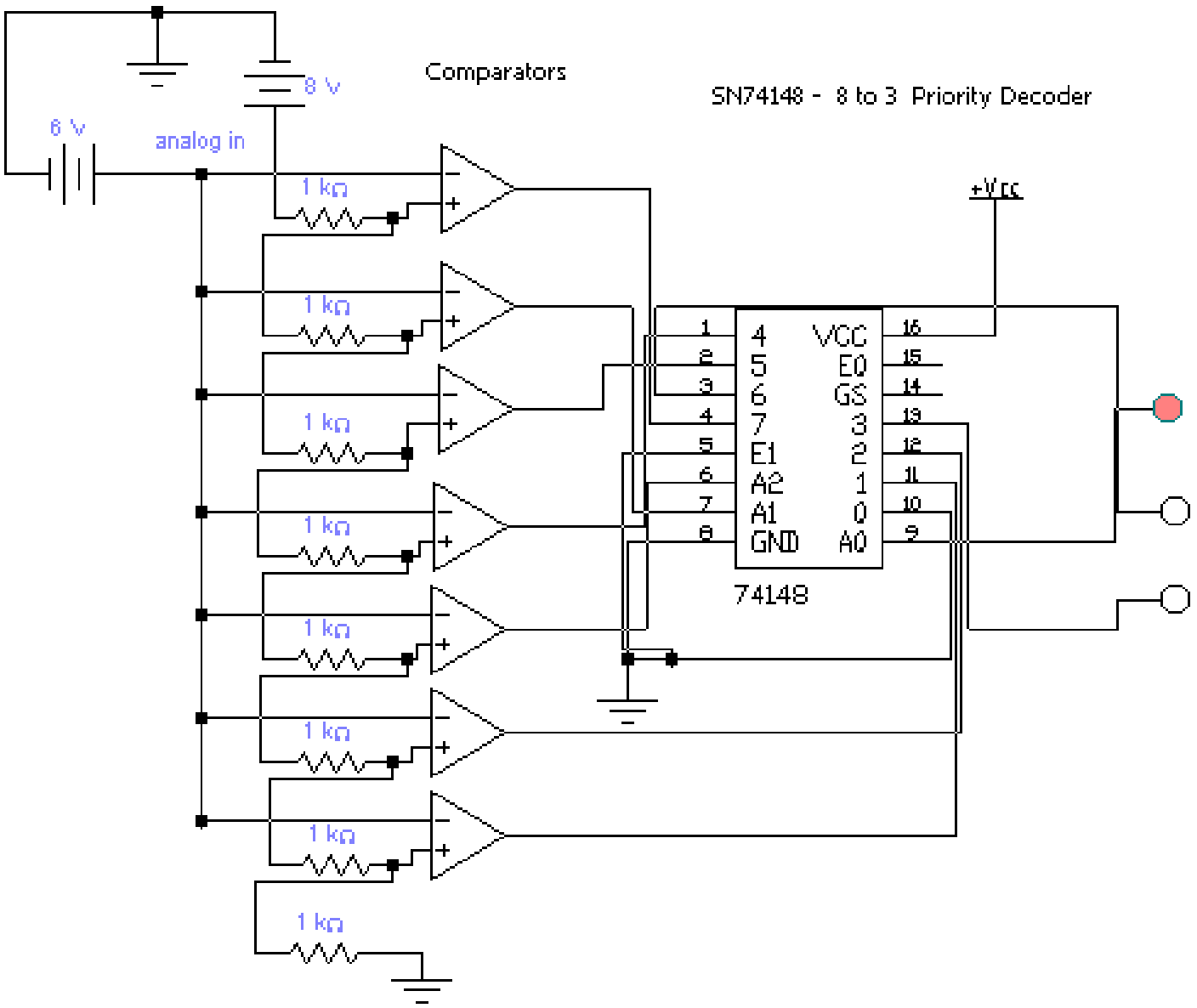
These type of A/D s are used in almost all digital meters. Such meters usually are not used to read rapidly changing values in the lab. Consequently the major disadvantage of such converters (very low speeds) is not a problem when the readout update rate is only a few times per second.

Flash Converters

If very high speed conversions are needed, e.g. video conversions, the most commonly used converter is a Flash Converter.

While such converters are extremely fast, they are also very costly compared to other types.

3 BIT FLASH A/D CONVERTER



Parallel or Flash Converters

The resistor network is a precision voltage divider, dividing V_{ref} (8 volts in the sample) into equal voltage increments (1.0 volts here) to one input of the comparator. The other comparator input is the input voltage

Each comparator switches immediately when V_{in} exceeds V_{ref} . Comparators whose input does not exceed V_{ref} do not switch.

A decoder circuit (a 74148 8-to-3 priority decoder here) converts the comparator outputs to a useful output (here binary)

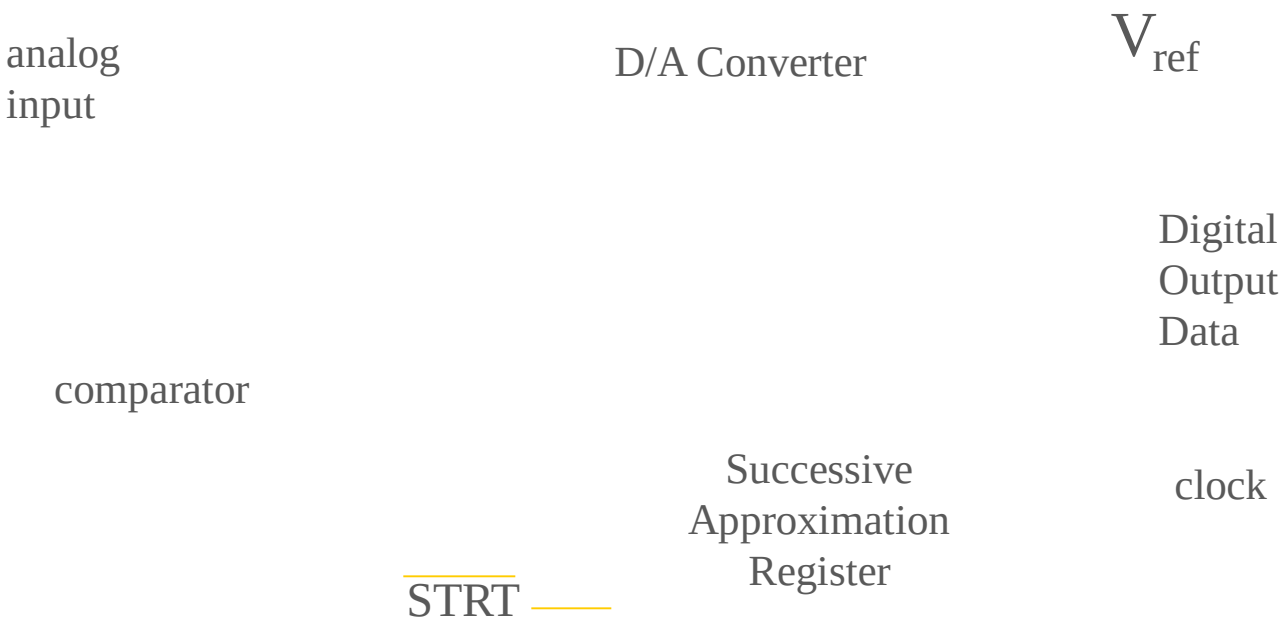
The speed of the converter is limited only by the speeds of the comparators and the logic network. Speeds in excess of 20 to 30 MHz are common, and speeds > 100 MHz are available

The cost stems from the circuit complexity since the number of comparators and resistors required increases rapidly. The 3-bit example required 7 converters, 6-bits would require 63, while an 8-bits converter would need 256 comparators and equivalent precision resistors.

While integrating or dual-slope A/Ds are widely used in digital instruments such as DVMs, the most common A/D used in the laboratory environment is the successive approximation.

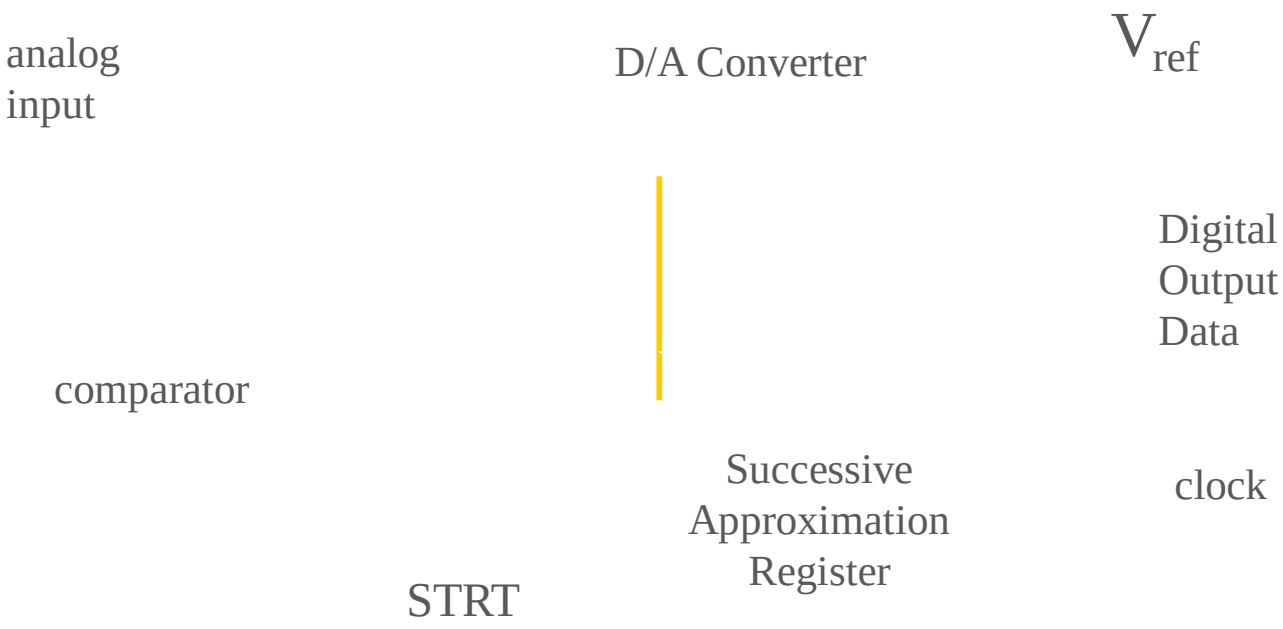
Successive approximation converters are reasonably priced for large bit values, i.e. 10, 12 and even 16 bit converters can be obtained for well under $100. Their conversion times, typically ~ 10-20 μs, are adequate for most laboratory functions.

Successive-Approximation A/D

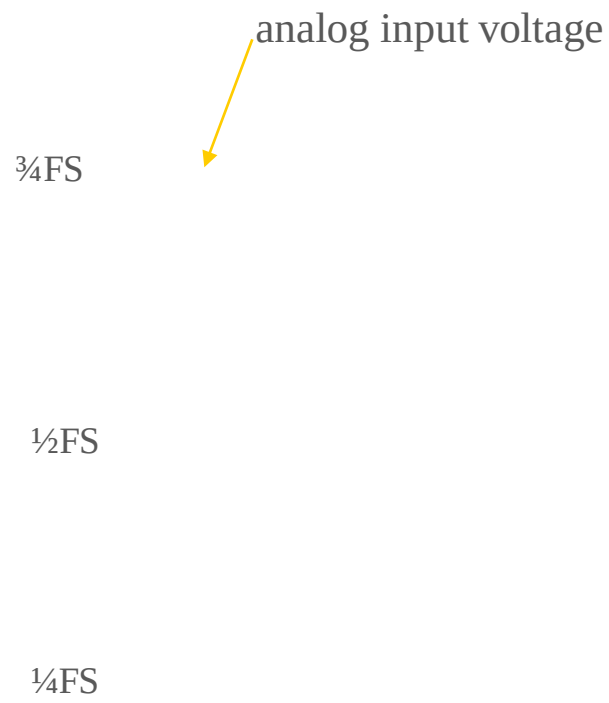


At initialization, all bits from the SAR are set to zero, and conversion begins by taking STRT line low.

Successive-Approximation A/D



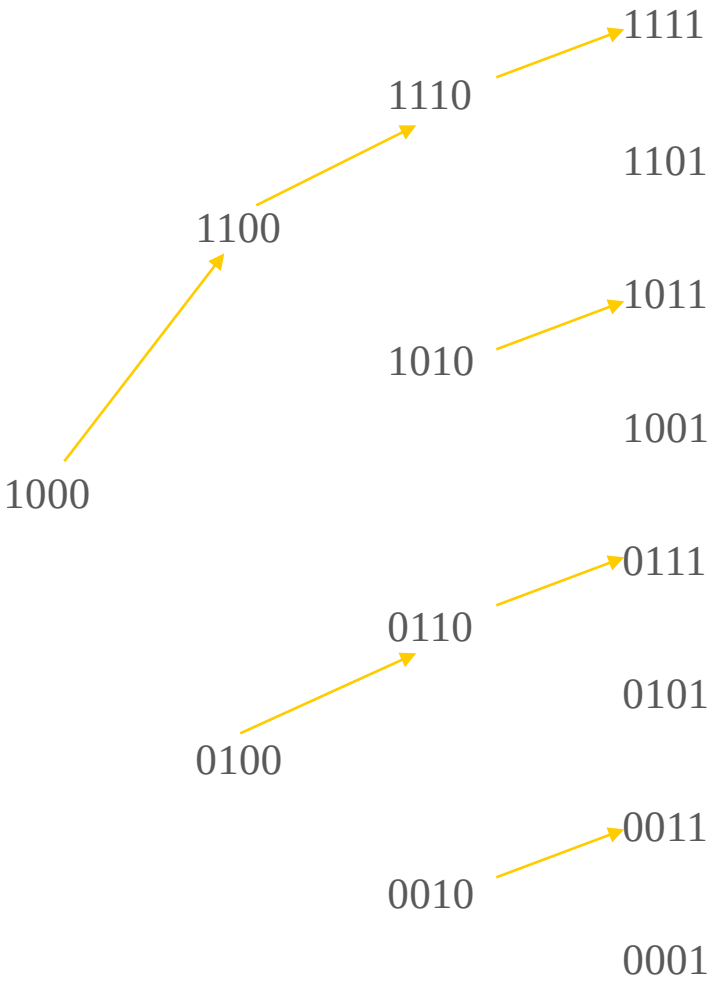
First the logic in the SAR sets the MSB bit equal to 1 (+5 V). Remember that a 1 in bit 7 will be half of full scale.



D/A output for 8-bit conversion with output code 1011 0111

Successive approximation search tree for a 4-bit A/D

D/A output compared with V_{in} to see if larger or smaller



Integrating type converters

An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time or frequency and then to a digital code is known as integrating type A/D converter

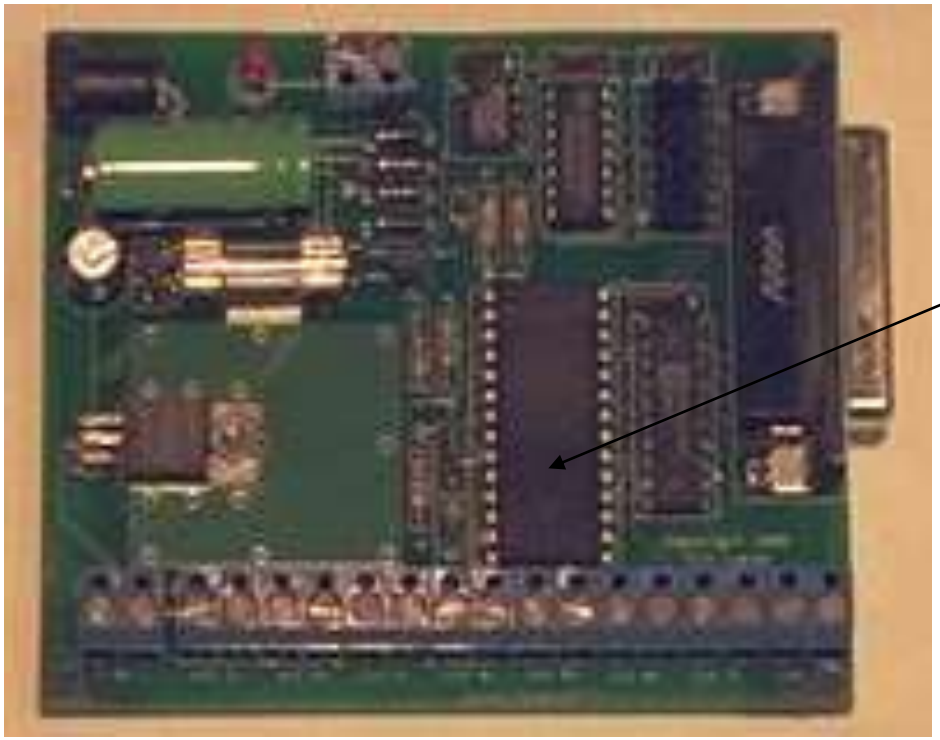
Sample and hold circuit

A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems.

Sample and hold circuit

The time during which the voltage across the capacitor in sample and hold circuit is equal to the input voltage is called sample period.The time period during which the voltage across the capacitor is held constant is called hold period

In practice, an ADC is usually in form of an integrated circuit (IC). ADC0808 and ADC0809 are two typical examples of 8-bit ADC with 8-channel multiplexer using successive approximation method for its conversion.



ADC0809
National
Semiconductor

For more information,

http://www.national.com/ads-cgi/viewer.pl/ds/AD/ADC0808.pdf

3. Selection of DAC

For the selection of an IC DAC, there are several parameters that can determine the suitability of a particular device.

Resolution

The number of bits making up the input data word that will ultimately determine the output step voltage as a percentage of full-scale output voltage.

Example: Calculate the resolution of an 8-bit DAC.

Solution: Resolution = 8 bits

Output Voltage Range

This is the difference between the maximum and minimum output voltages expressed in volts.

Example:

Calculate the output voltage range of a 4-bit DAC if the output voltage is +4.5V for an input of 0000 and +7.5V for an input of 1111.

Solution:

Output voltage range = 7.5 – 4.5 = 3.0V

Accuracy

The accuracy is usually expressed by the error in output voltage compared with the expected output voltage. The higher the accuracy, the lower will be the error. Due to the incremental nature of the digital input word, an error can be tolerated but it should not exceed ±½LSB or ½resolution.

Example. The error at full-scale for an 8-bit DAC with 10V maximum output is 50mV. Calculate the error and compare it with the resolution.

The accuracy is not as good as the error = ½ resolution, but for many applications, it is quite satisfactory. Some commercially available DACs have their accuracy specified as worse than ½ resolution.

Sources of errors may be broadly classified under four categories:

- Non-monotonicity
- Non-linearity
- Scale-factor error
- Offset error

Settling time

The time taken for the applied digital input to be converted to an analog output. Typical period can be as low as 100ns, making DA conversion a very fast process compared with those of AD conversion.

Input coding

The digital input can be in binary format or it can be in binary coded decimal format depending on the application. Binary format is more commonly used.

It should be noted in the table above that the BCD coding is the binary equivalent of the decimal digit. However, BCD and binary are not the same.

For example,

$$49_{10} \text{ in binary is } 110001_{2},$$

but

$$49_{10} \text{ in BCD is } 01001001_{\text{BCD}}.$$

Each decimal digit is converted to its binary equivalent.

4. Selection of ADC

The parameters used in selecting an ADC are very similar to those considered for a DAC selection.

- Error/Accuracy: Quantising error represents the difference between an actual analog value and its digital representation. Ideally, the quantising error should not be greater than ± ½ LSB.
- Resolution: DV to cause 1 bit change in output
- Output Voltage Range ⇒ Input Voltage Range
- Output Settling Time ⇒ Conversion Time
- Output Coding (usually binary)

Thank you