(20A04101T) ELECTRONIC DEVICES & CIRCUITS

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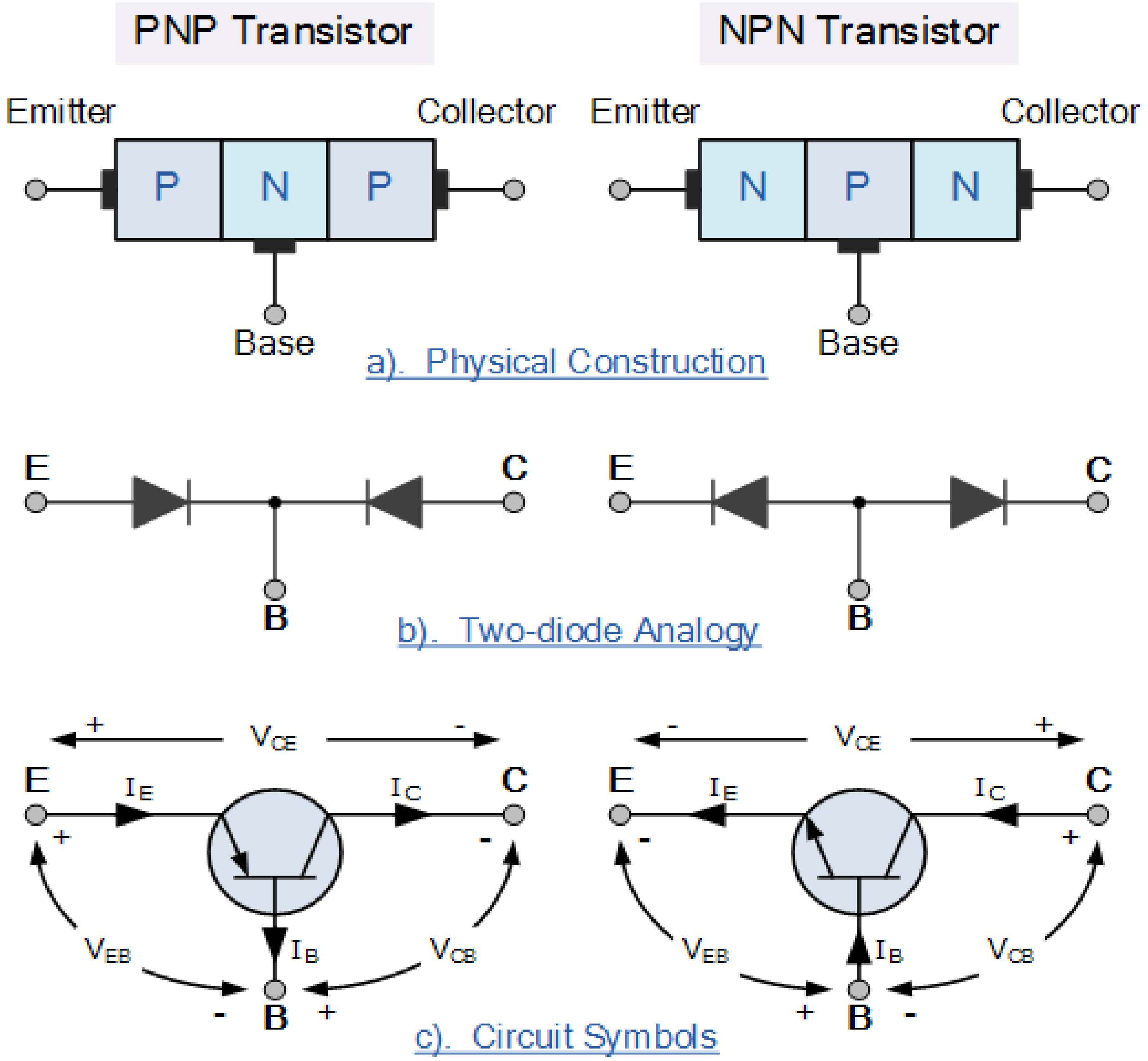
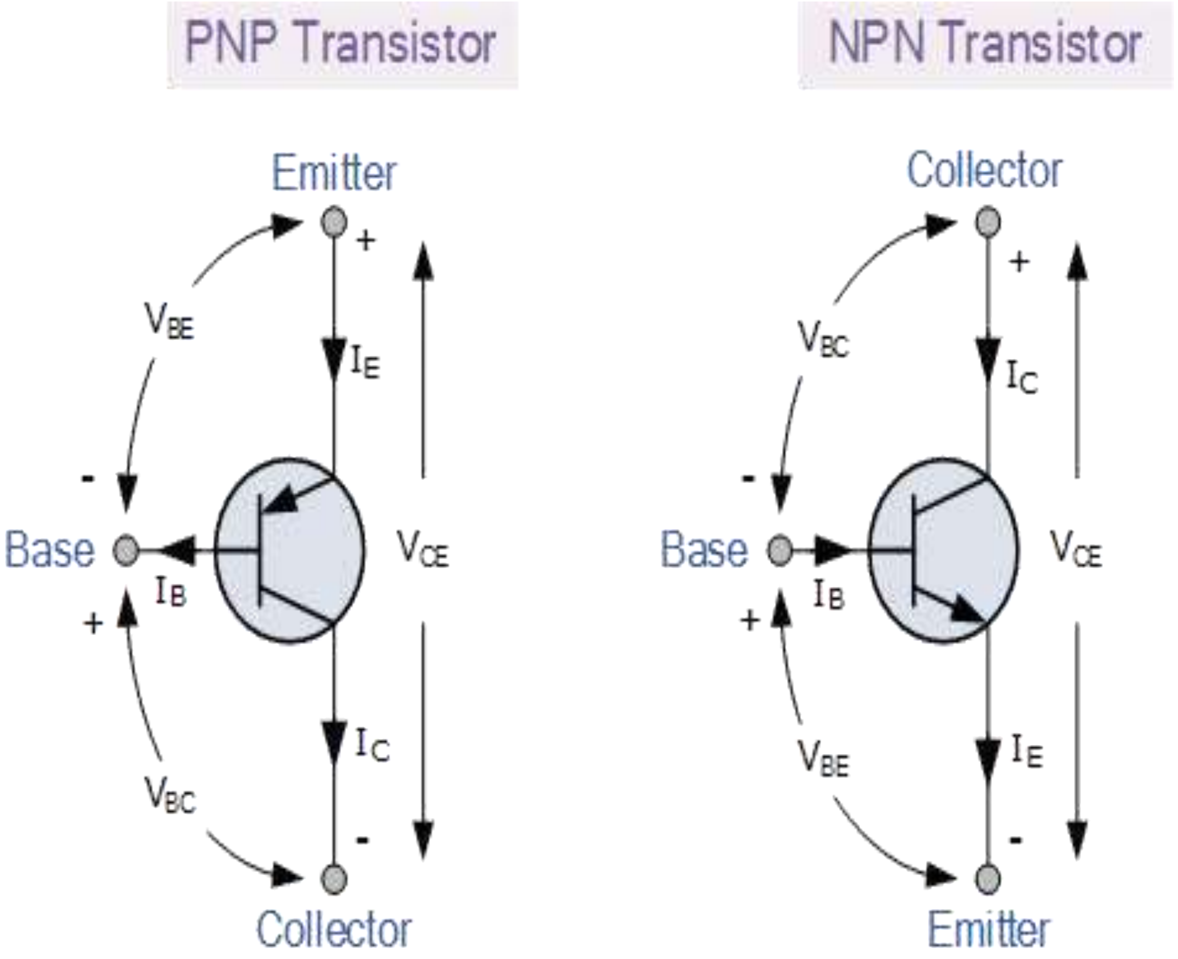
Unit- 3

- BJT Circuits at DC
- Applying the BJT in Amplifier Design
  - Voltage Amplifier
  - Voltage Transfer Characteristic (VTC)
  - Small-Signal Voltage Gain
  - Determining the VTC by Graphical Analysis
  - Q-POINT
- Small-Signal Operation and Models
  - **Transconductance**
  - **Input Resistance** at the Base
  - **Input Resistance** at the Emitter
  - **Voltage Gain**
  - Separating the Signal and the DC Quantities
  - The **Hybrid-π Model**
  - the **T Model**

- Basic BJT Amplifier Configurations
  - Common-Emitter (CE) amplifier without and with emitter resistance
  - Common-Base (CB) amplifier
  - Common-Collector (CC) amplifier or Emitter Follower
- Biasing in BJT Amplifier Circuits
  - Fixed bias
  - Self bias
  - Voltage Divider Bias Circuits
- Biasing using a Constant-Current Source
- CE amplifier – Small Signal Analysis and Design
- Transistor breakdown and Temperature Effects
- Problem solving.

BJT


PNP Transistor
NPN Transistor
Emitter
Collector
P N P
N P N
Base
a). Physical Construction
E
C
B
b). Two-diode Analogy
V_{CE}
I_E
I_C
I_B
V_{EB}
V_{CB}
c). Circuit Symbols


PNP Transistor
NPN Transistor
Emitter
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Base
V_{BE}
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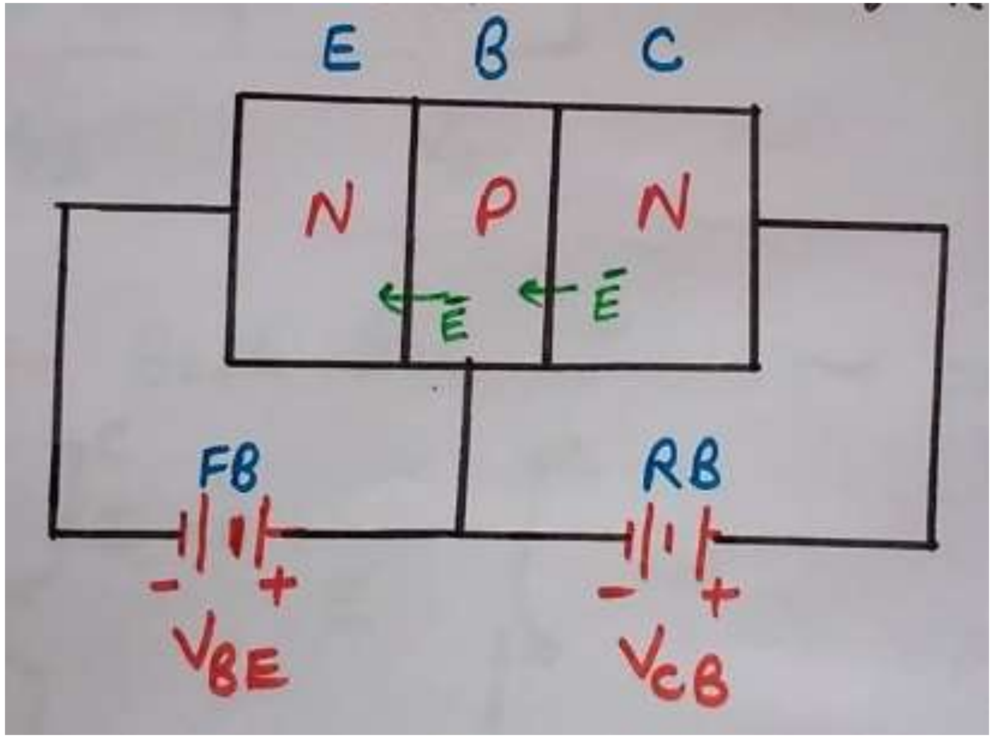
I_E
I_C
I_B

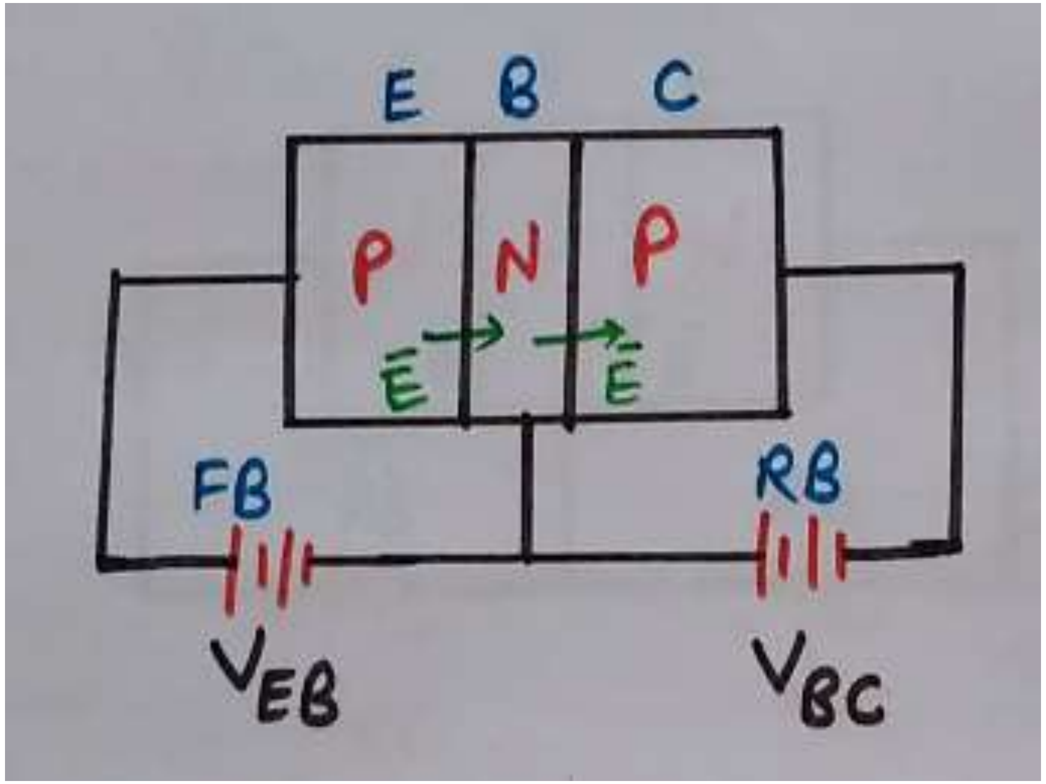
BJT

Operation Modes of BJT
***Active mode**
***Saturation mode**
***Cutoff mode**

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward



Active Mode Operation of BJT Transistor(NPN BJT)



Active Mode Operation of PNP BJT

BJT

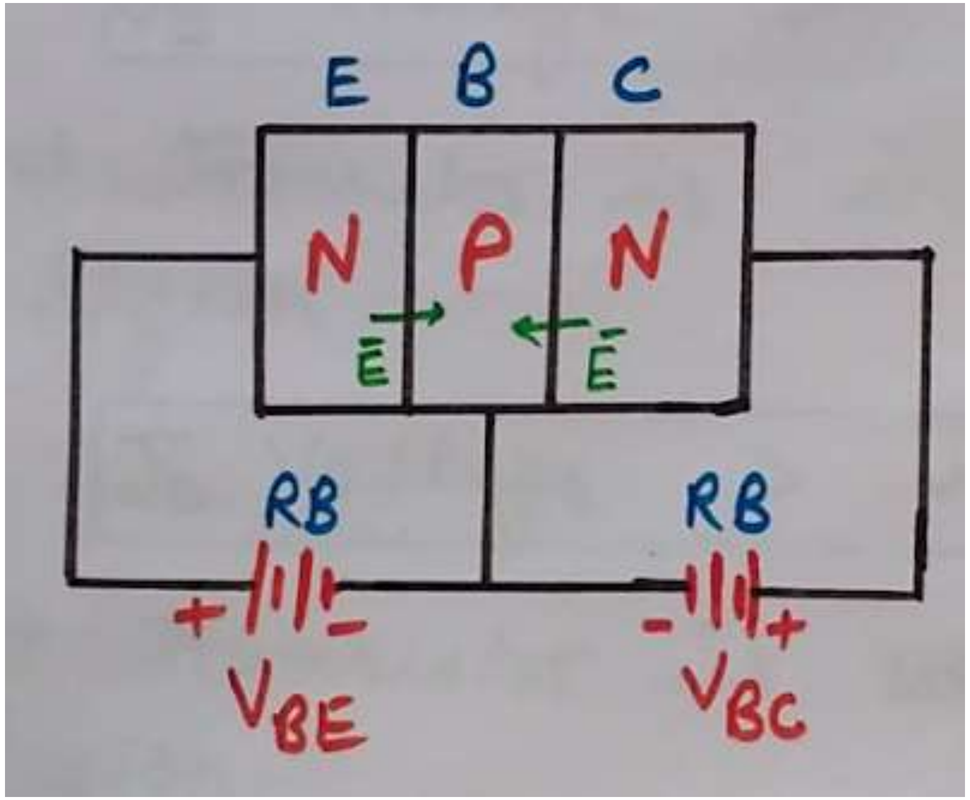
<u>**Operation Modes of BJT**</u>

***Active mode**

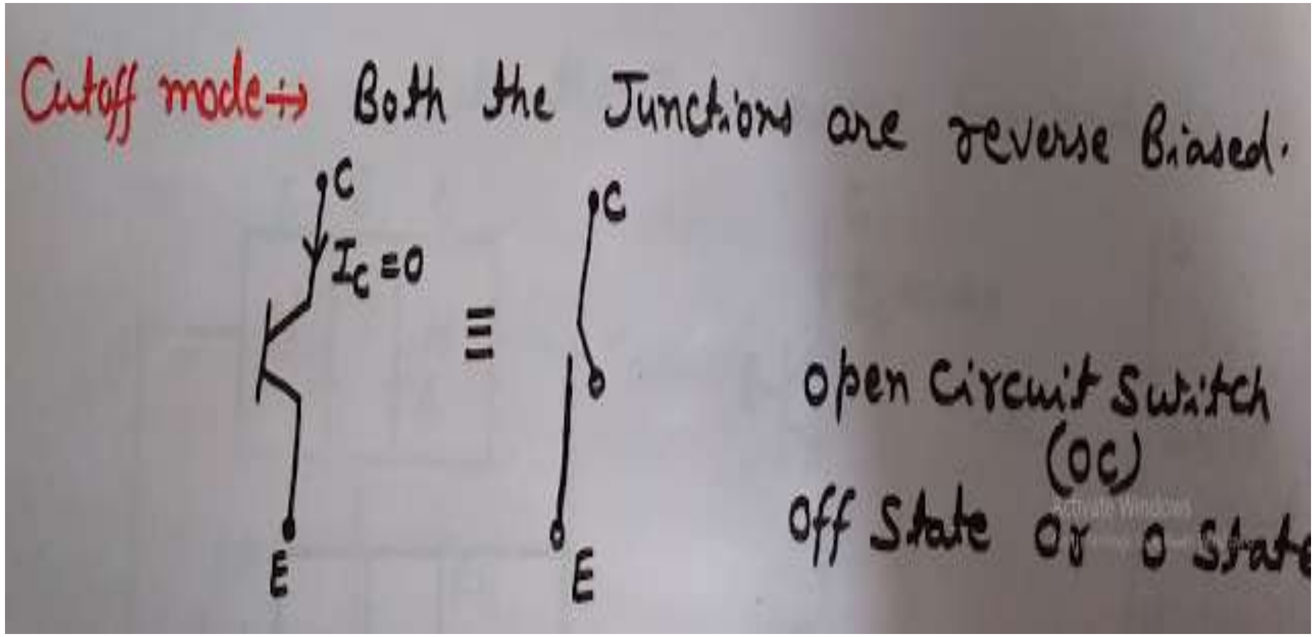
***Saturation mode**

***Cutoff mode**

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward



Cut off Mode Operation of BJT



BJT

Operation Modes of BJT
***Active mode**
***Saturation mode**
***Cutoff mode**

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
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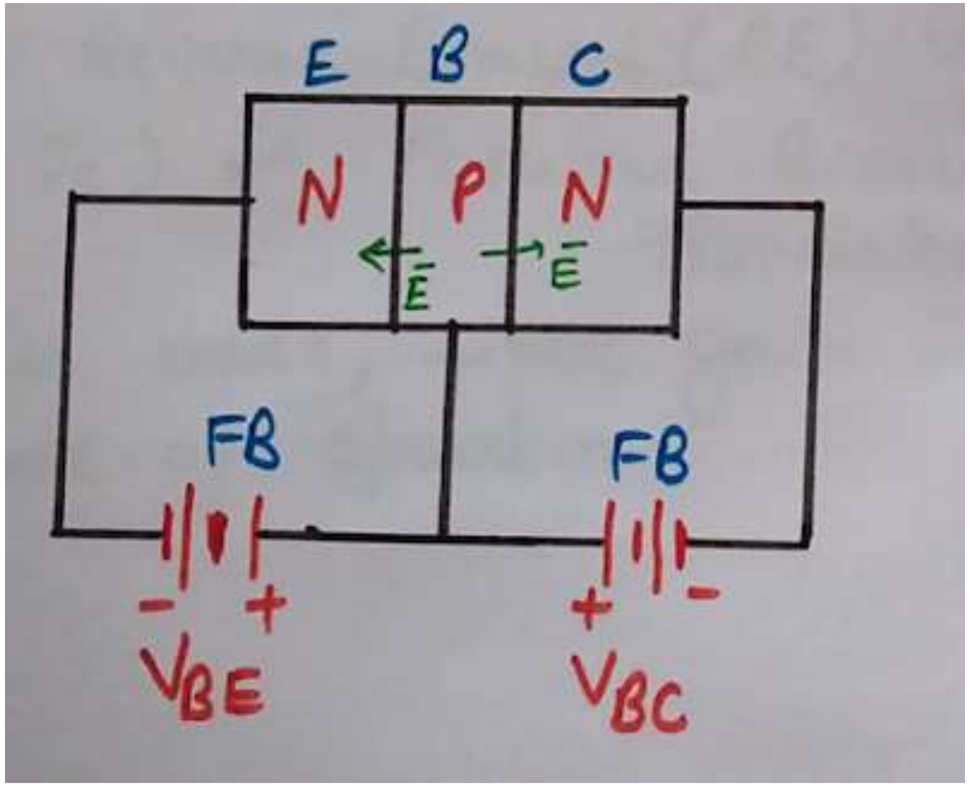
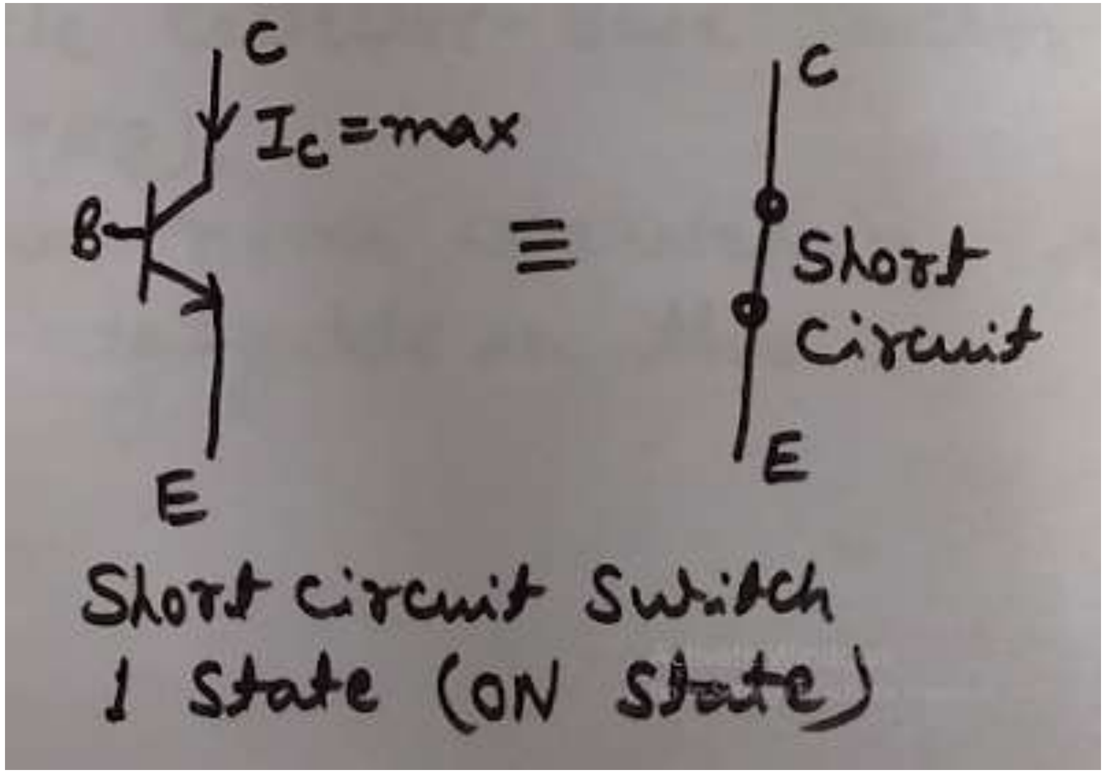
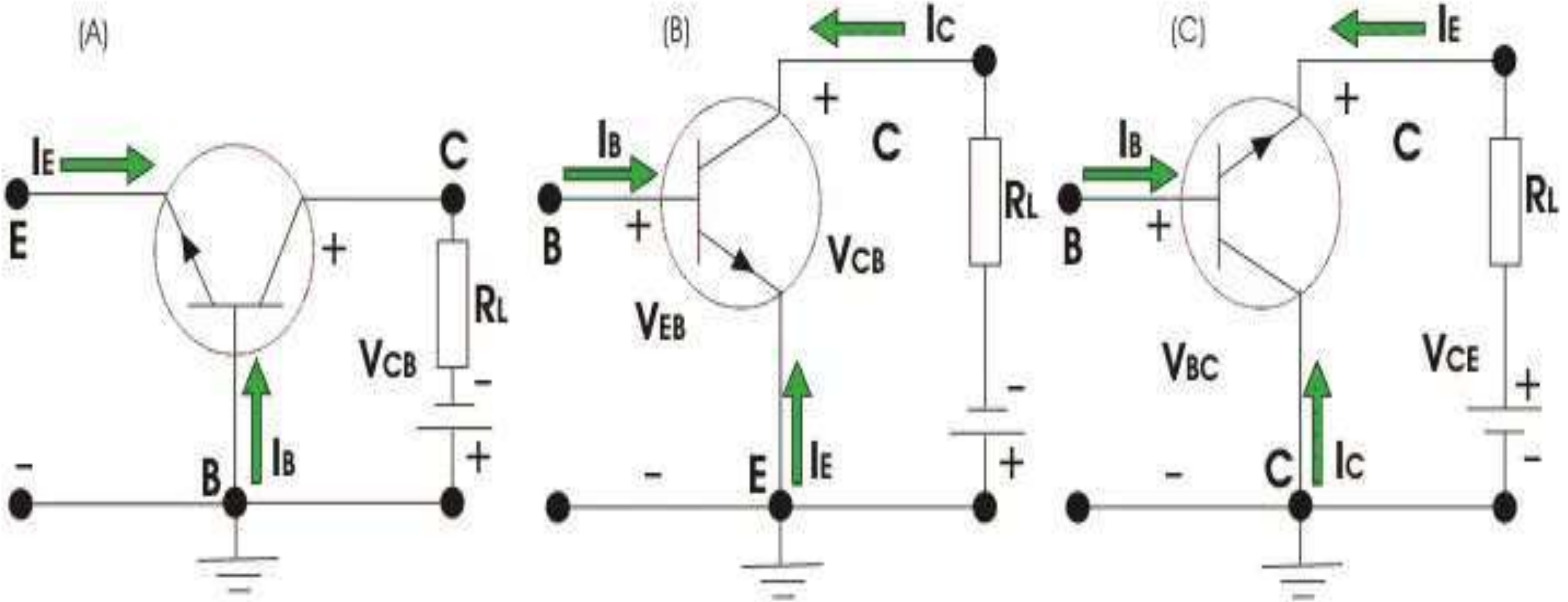
Saturation	Forward	Forward





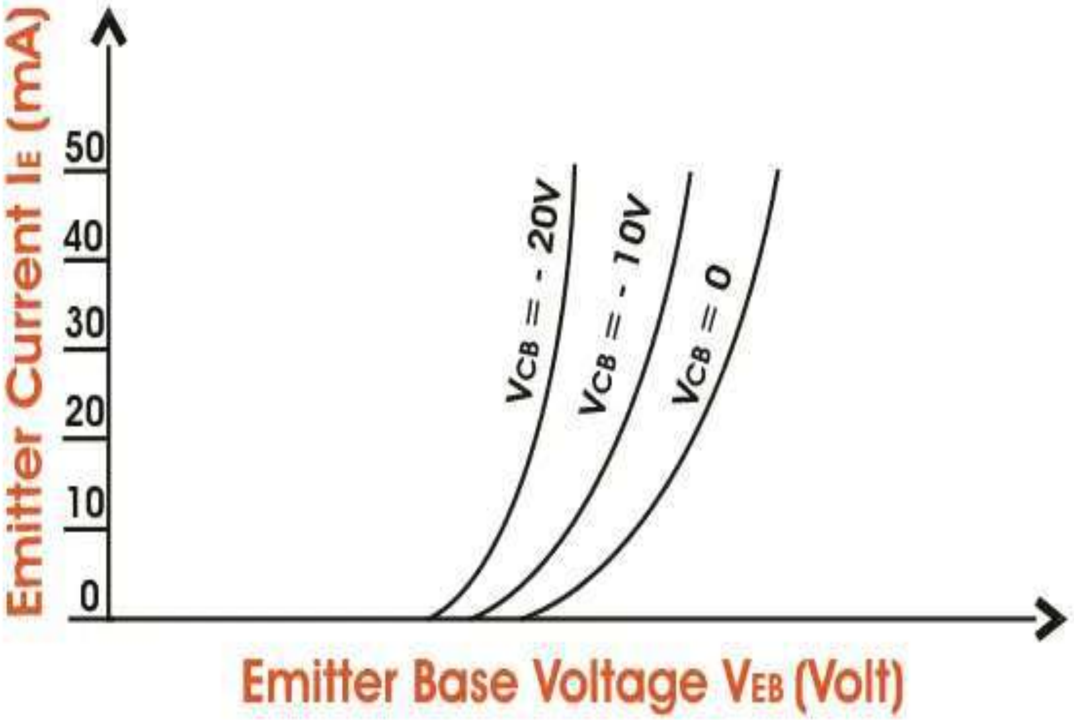
Saturation Mode Operation of BJT

BJT

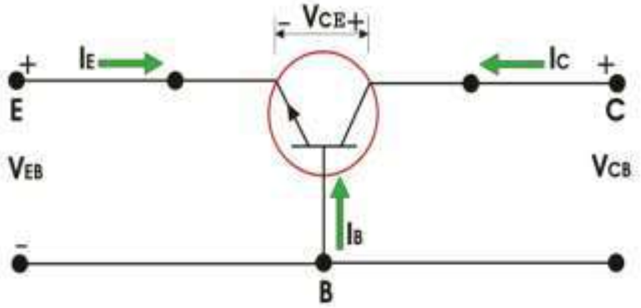


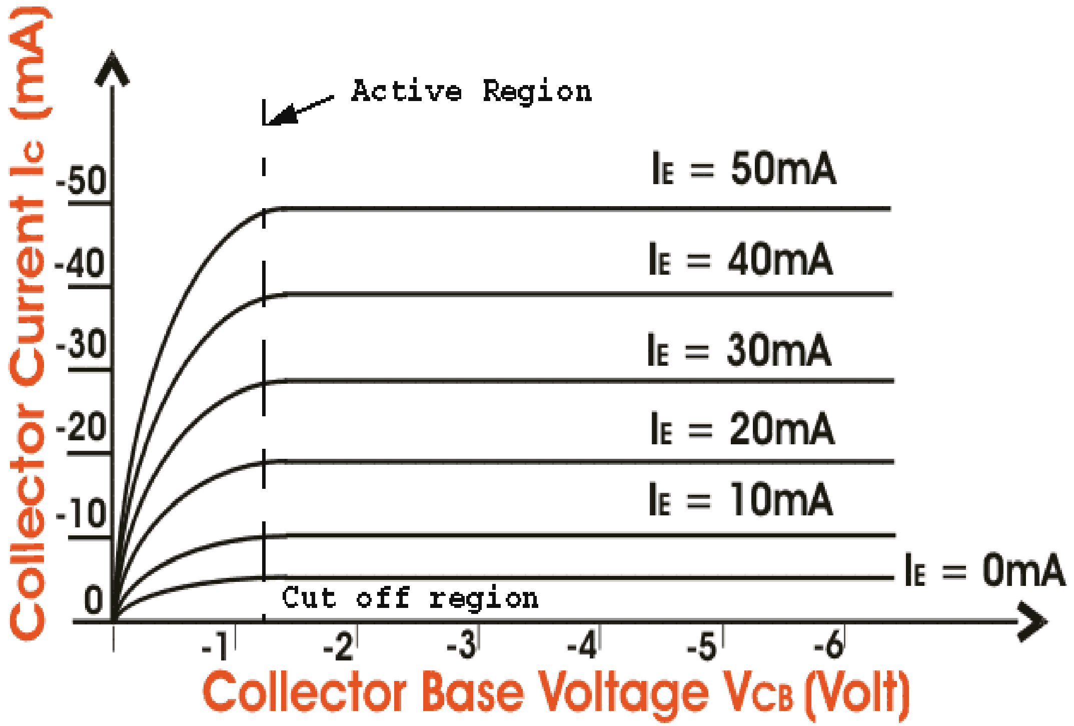
BJT

Common Base Characteristics
Input Characteristics



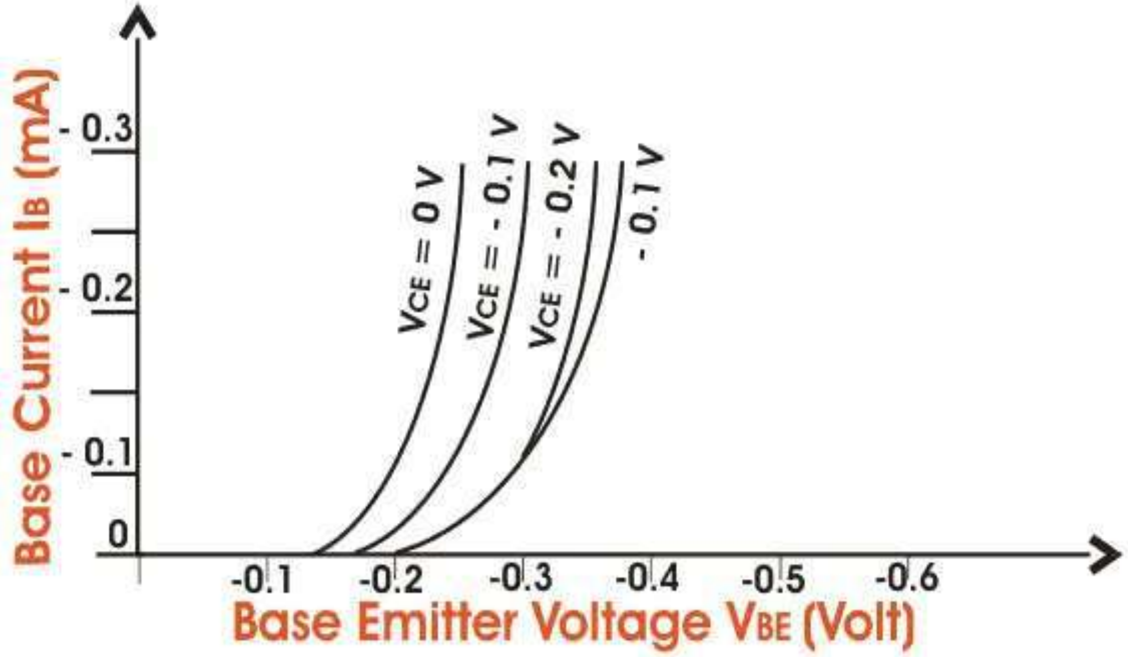
Output Characteristics



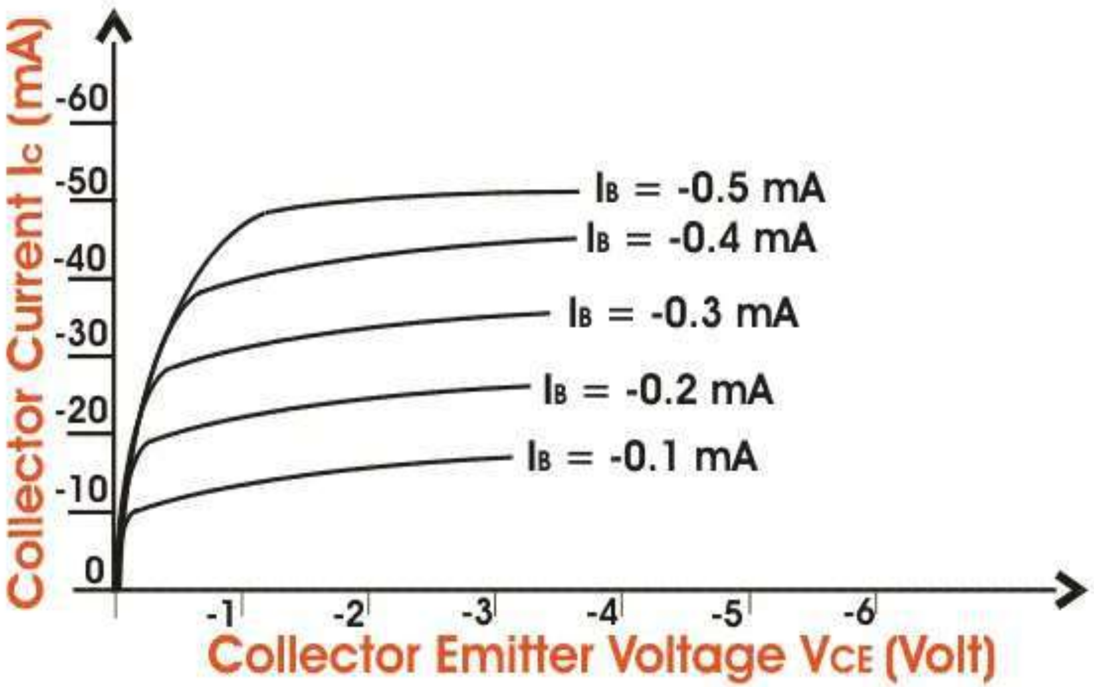


BJT

Common Emitter Characteristics
Input Characteristics



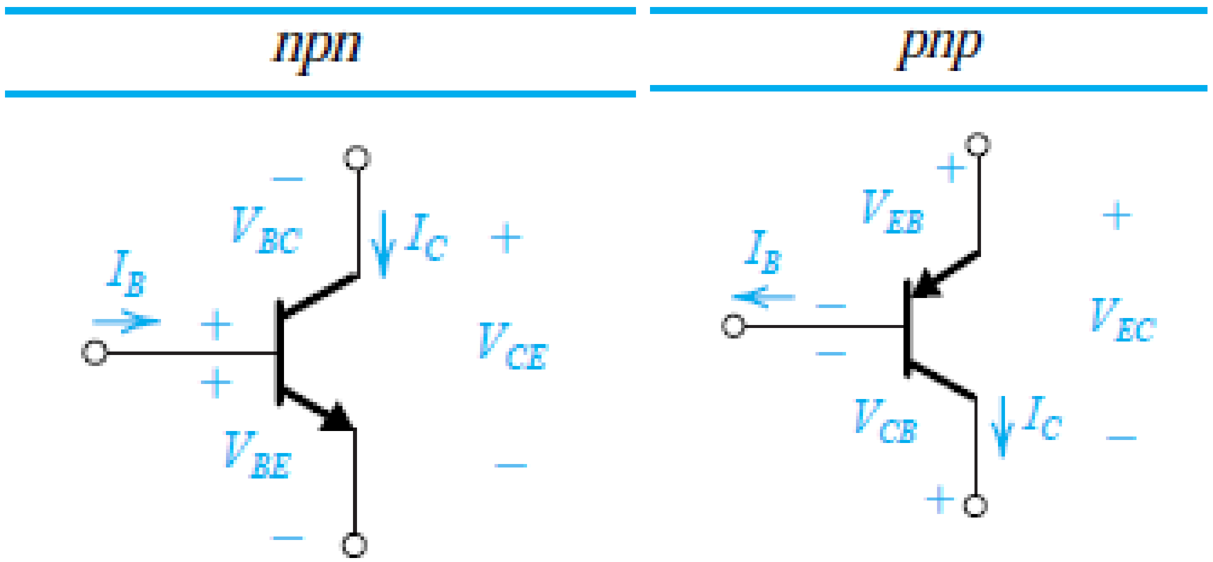
Output Characteristics

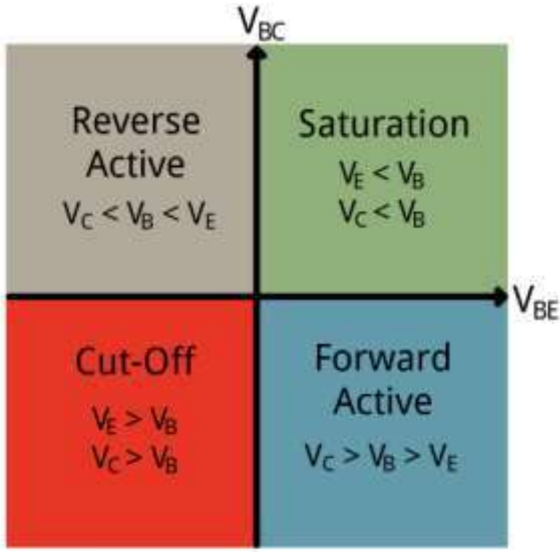


BJT Circuits at DC

Conditions and Models for the Operation of the BJT in Various Modes

- Only DC Voltages are applied
- Vbe=0.7 V and Vce=0.2 V

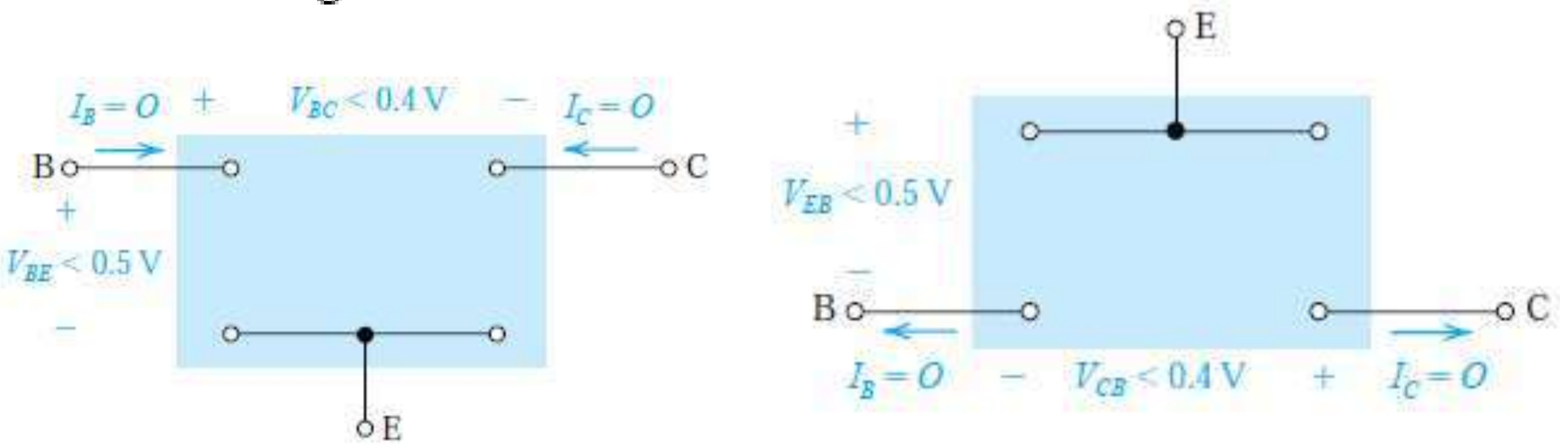




Cutoff

EJB: Reverse Biased

CBJ: Reverse Biased



BJT Circuits at DC

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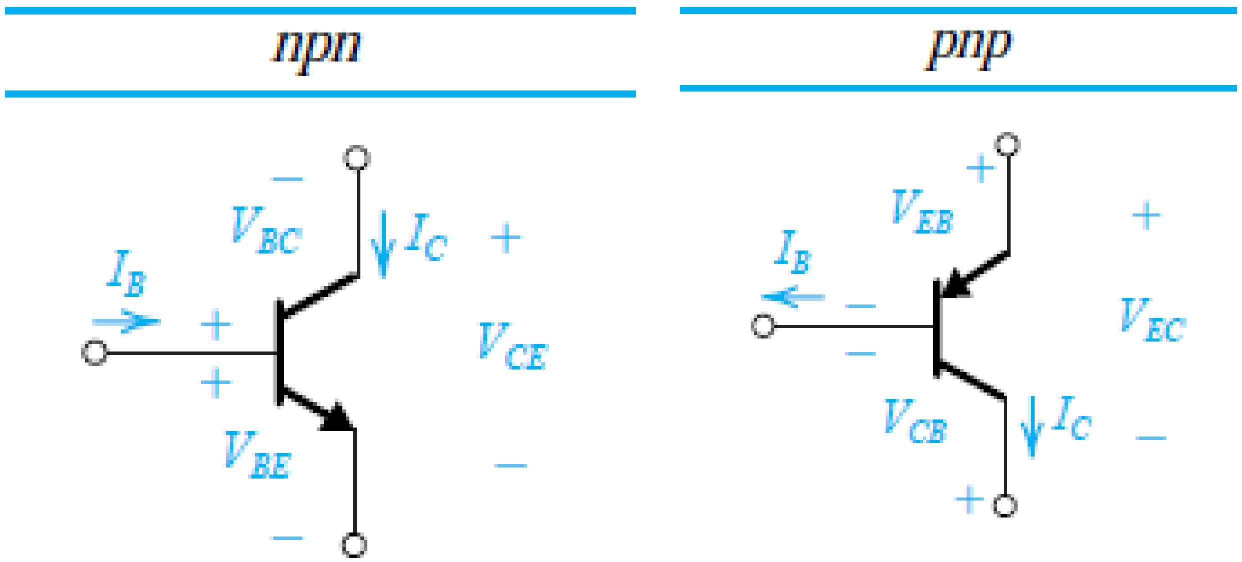

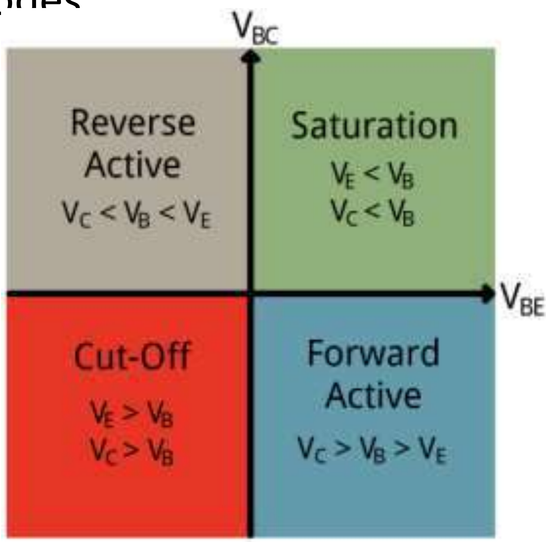

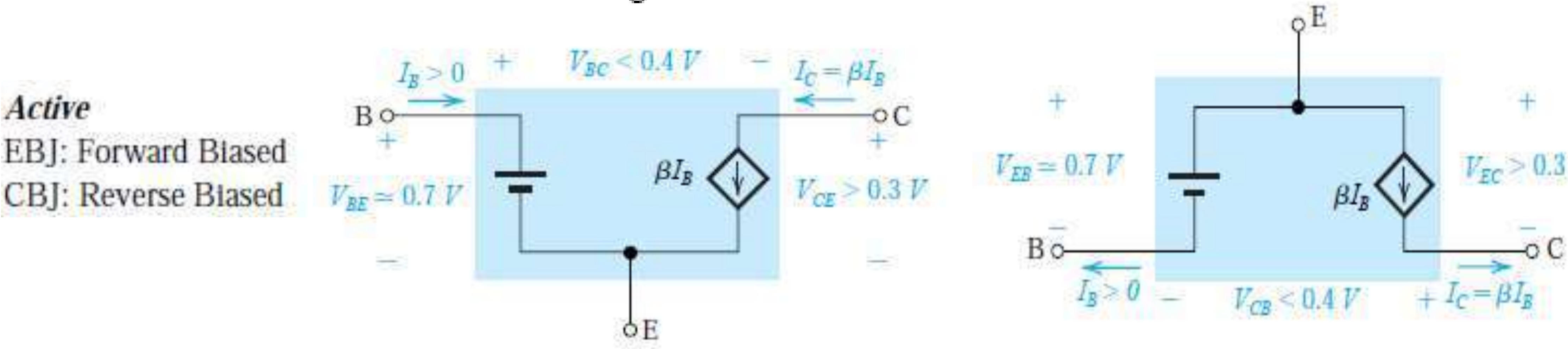

BJT Circuits at DC

Conditions and Models for the Operation of the BJT in Various Modes

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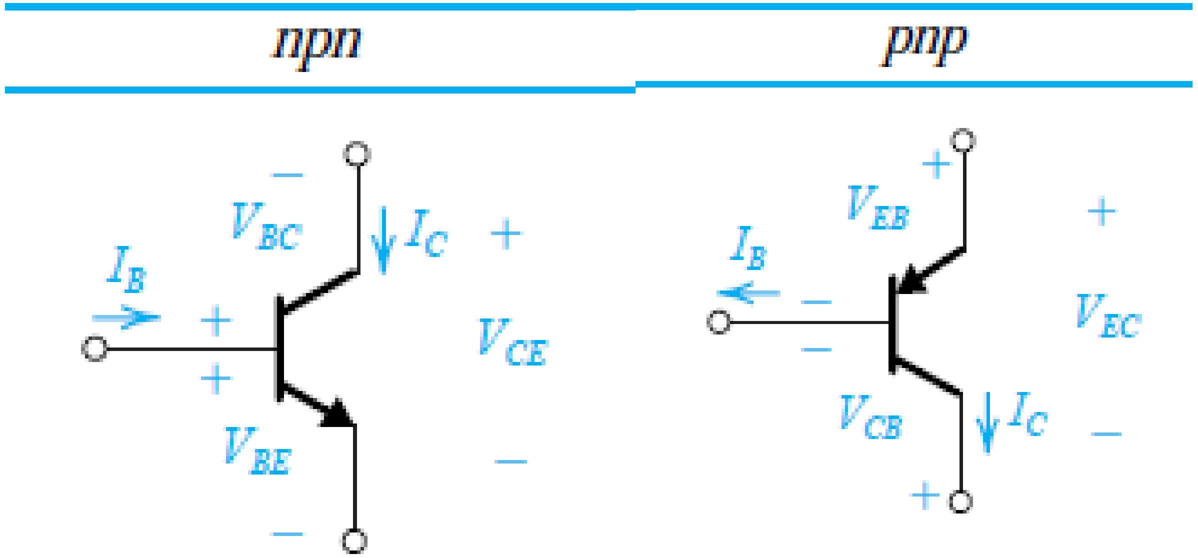
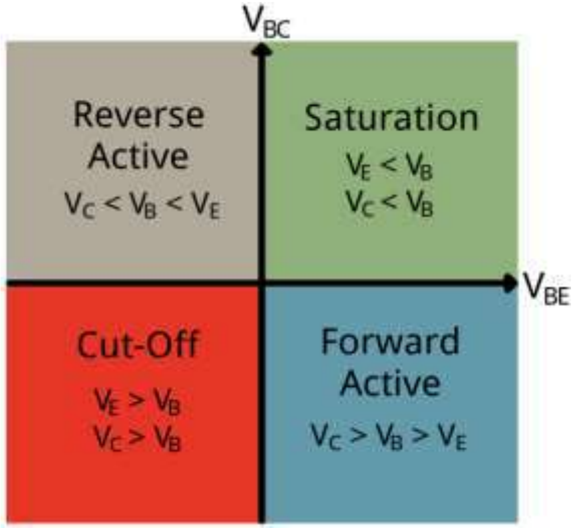
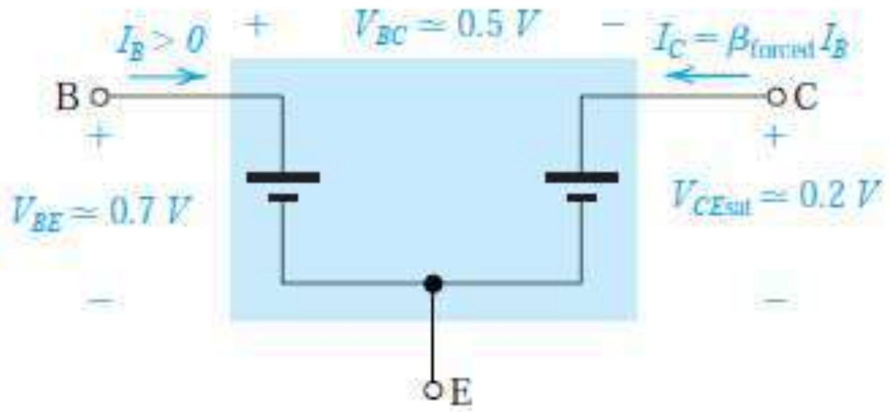
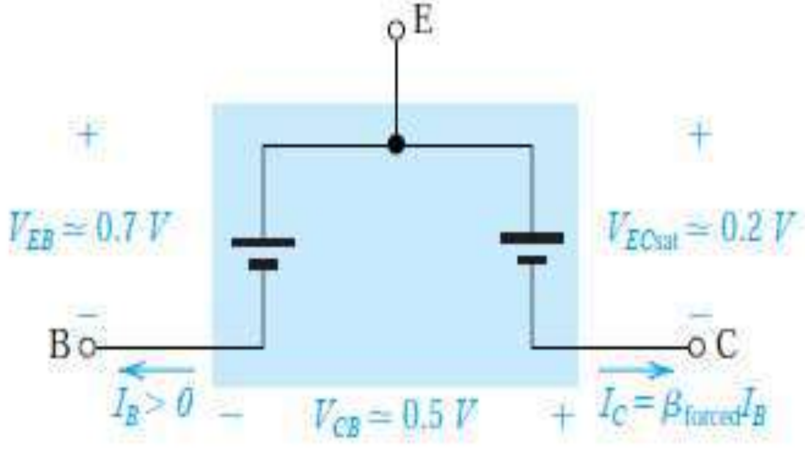




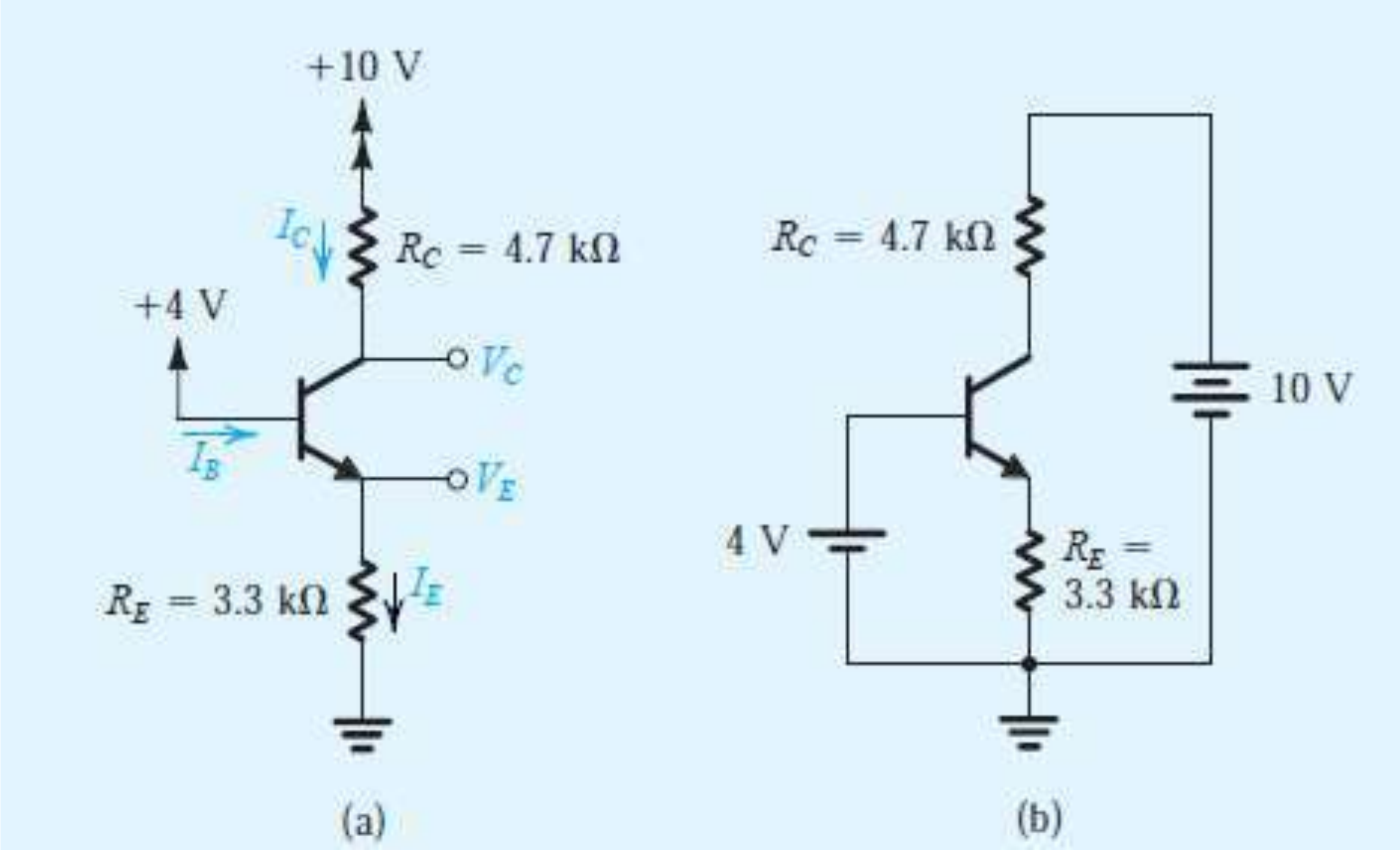
Saturation
EBJ: Forward Biased
CBJ: Forward Biased

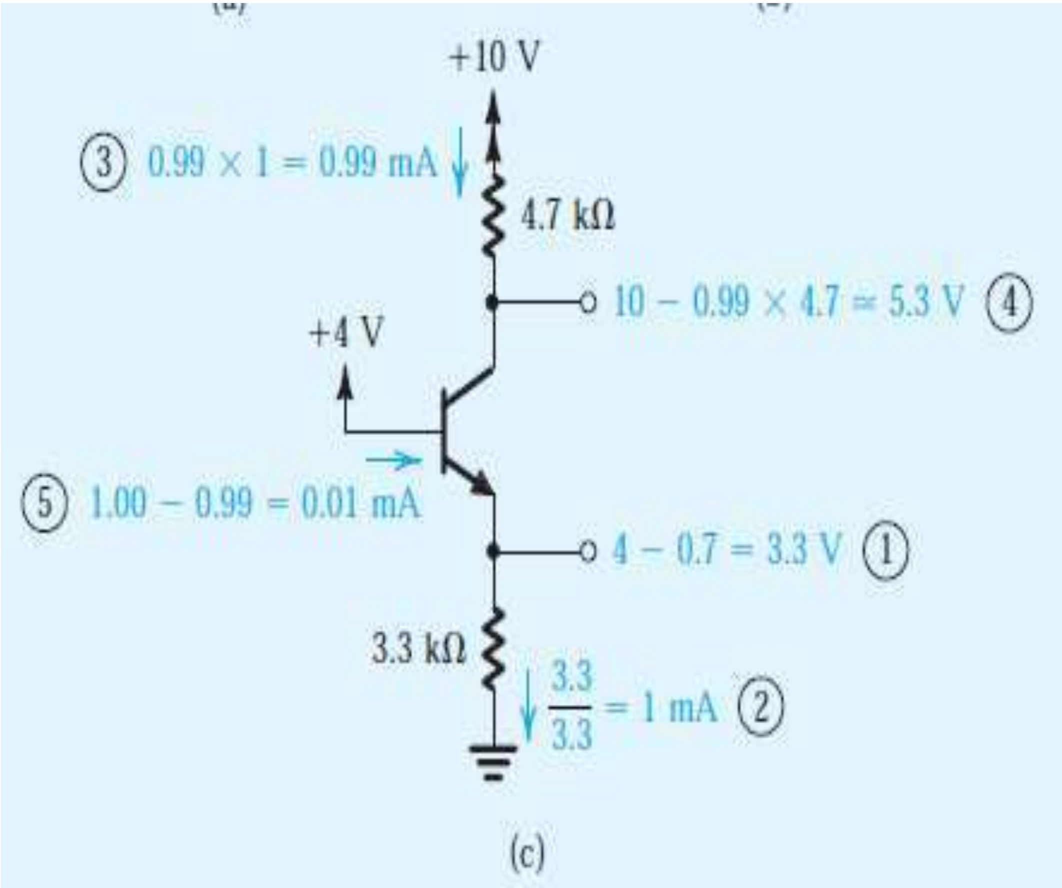




BJT Circuits at DC-Active Mode(Problems)

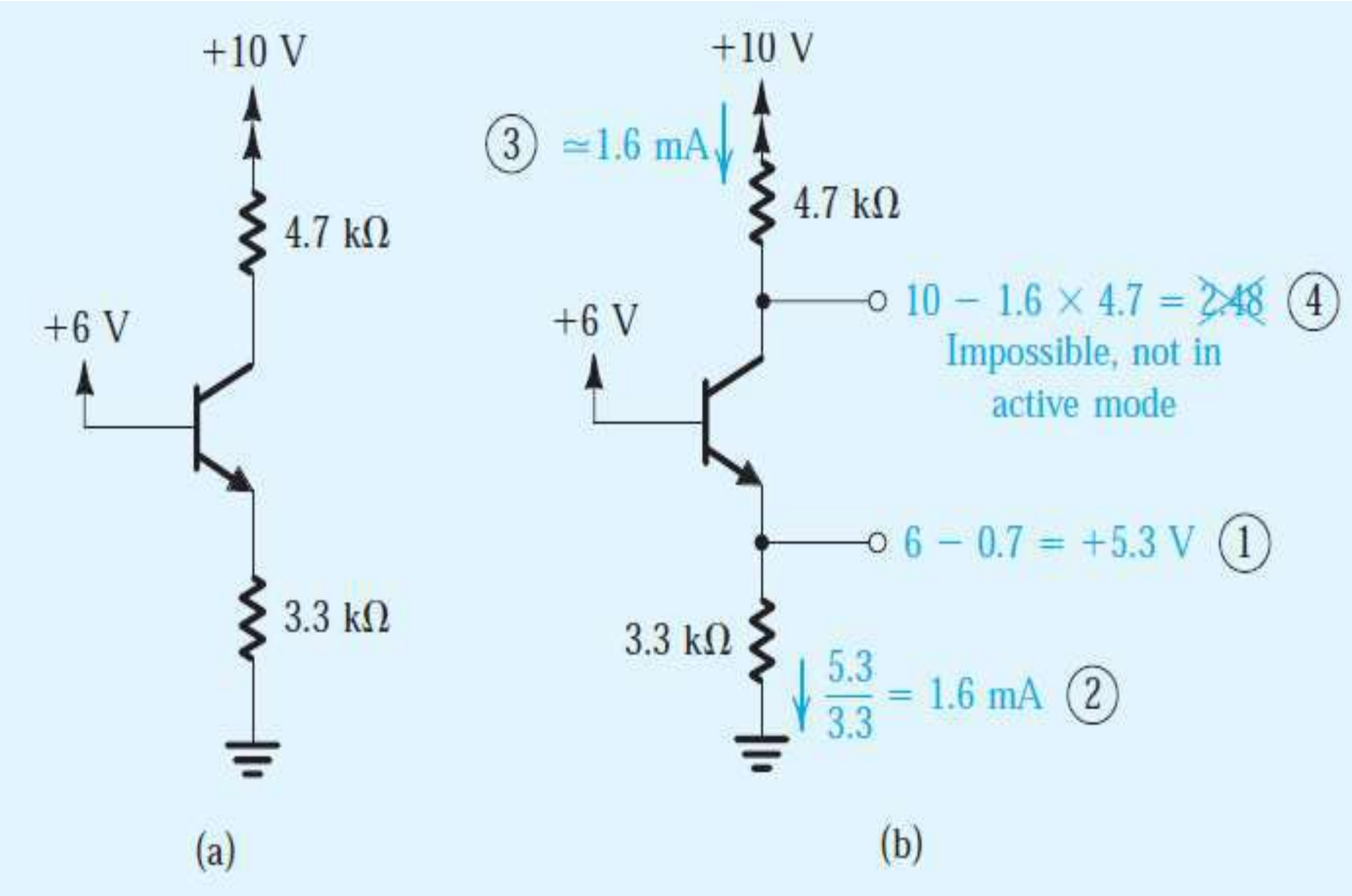
Example, β is specified to be 100.

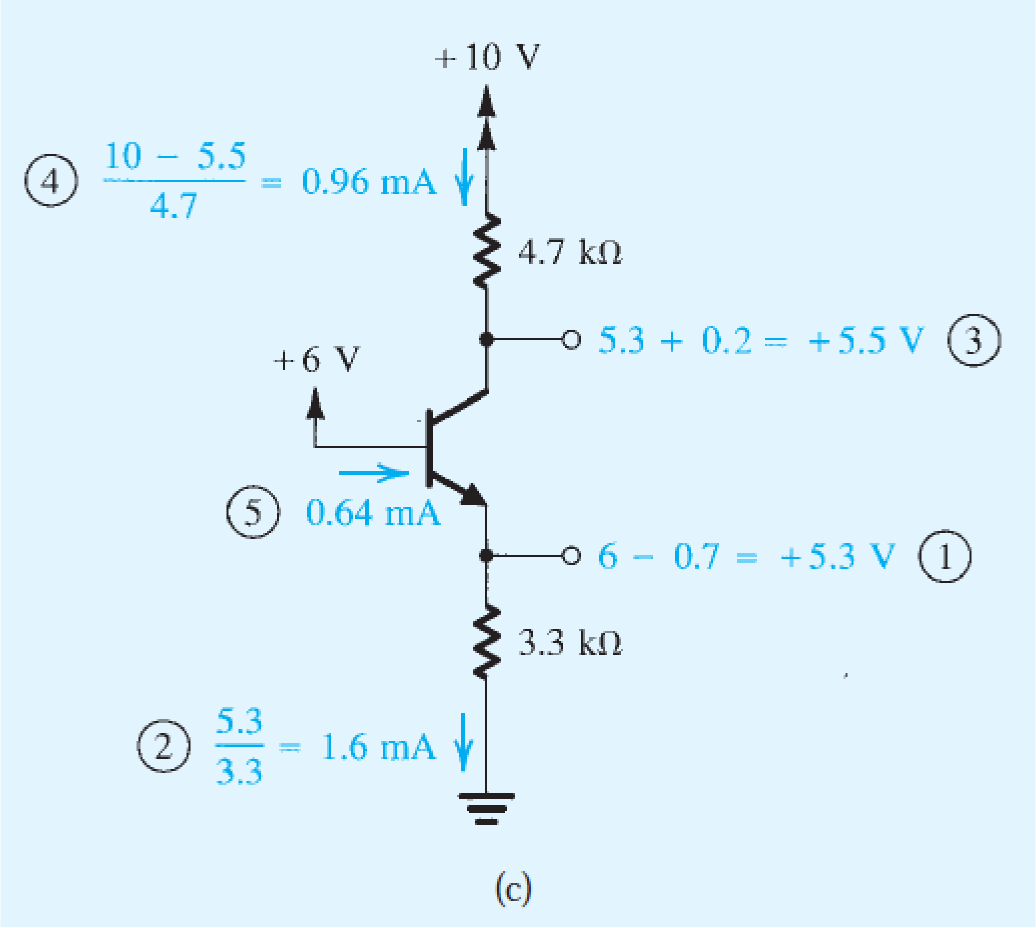




BJT Circuits at DC-Saturation Mode(Problems)

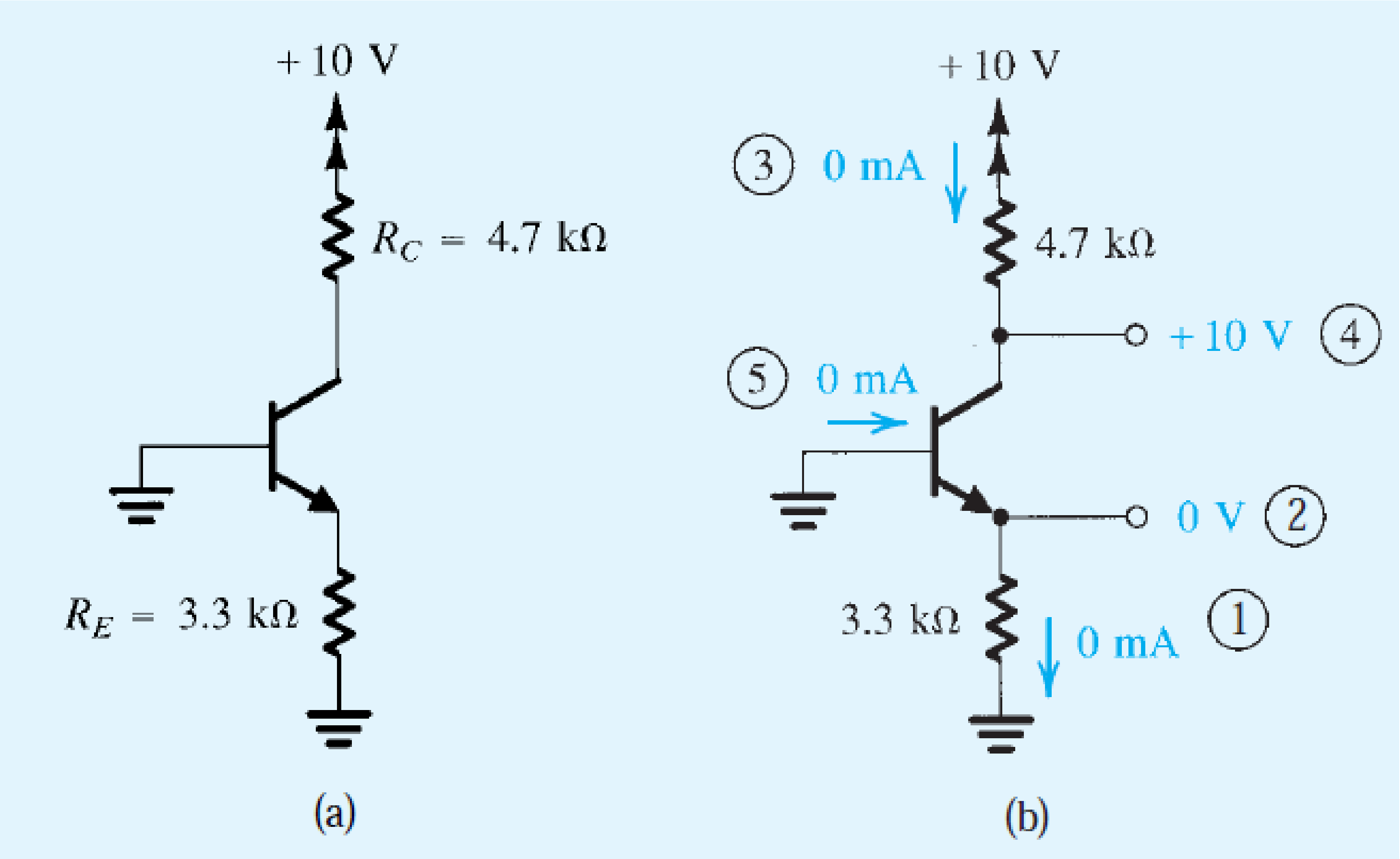
Example, β is specified to be ATLEAST OF 50.





BJT Circuits at DC-Cutoff Mode(Problems)

Example

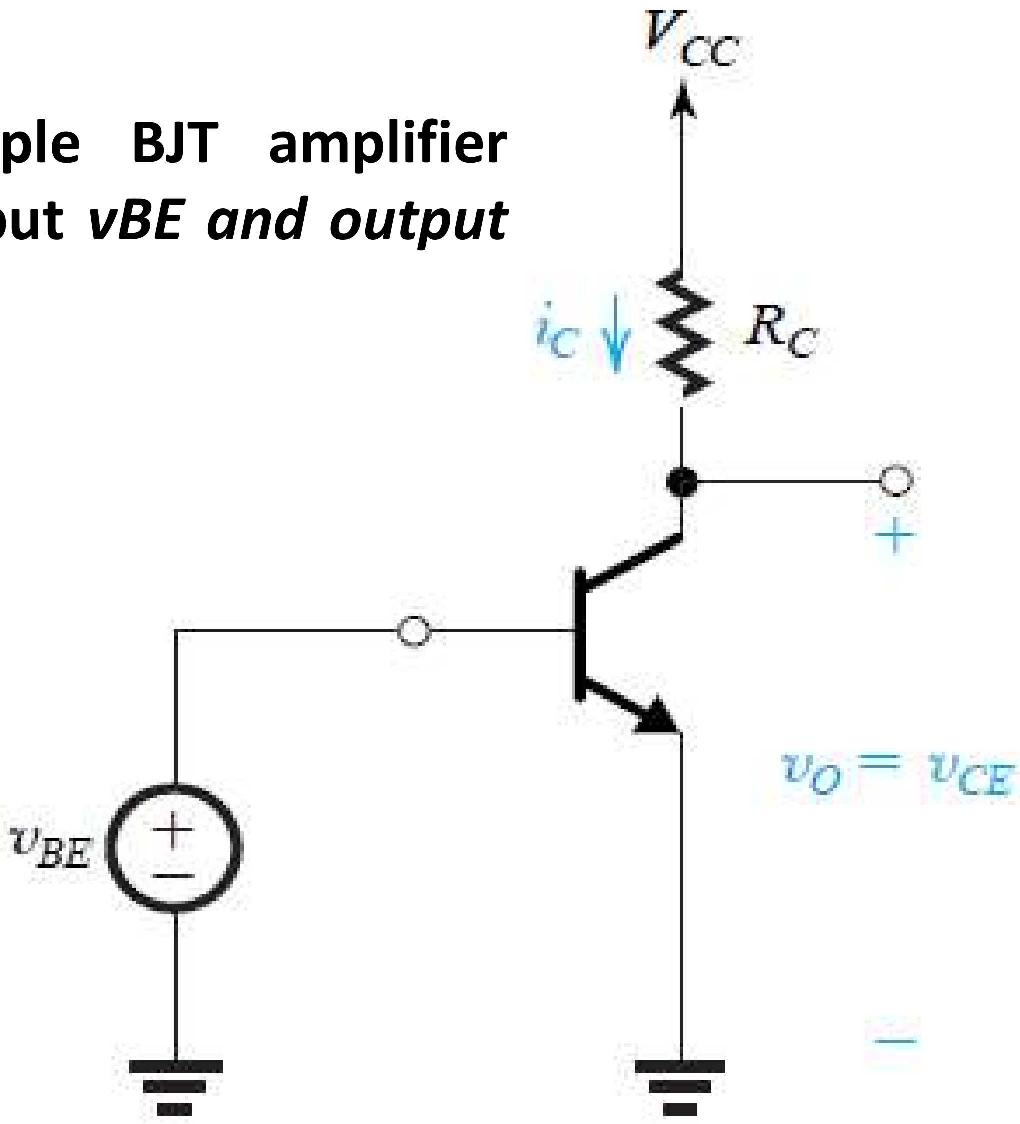


Applying the BJT in Amplifier Design

- The basis for this important application is that when operated in the **active mode**, the BJT functions as a **voltage-controlled current source**: the **base–emitter voltage(Vbe)** controls the **collector current(Ic)**
- Although the control relationship is **nonlinear (exponential)**
- we will shortly devise a method for obtaining **almost-linear amplification** from this fundamentally nonlinear device.
  - Voltage Amplifier
  - Voltage Transfer Characteristic (VTC)
  - **Biasing the BJT to Obtain Linear Amplification**
  - Small-Signal Voltage Gain
  - Determining the VTC by Graphical Analysis
  - Q-POINT

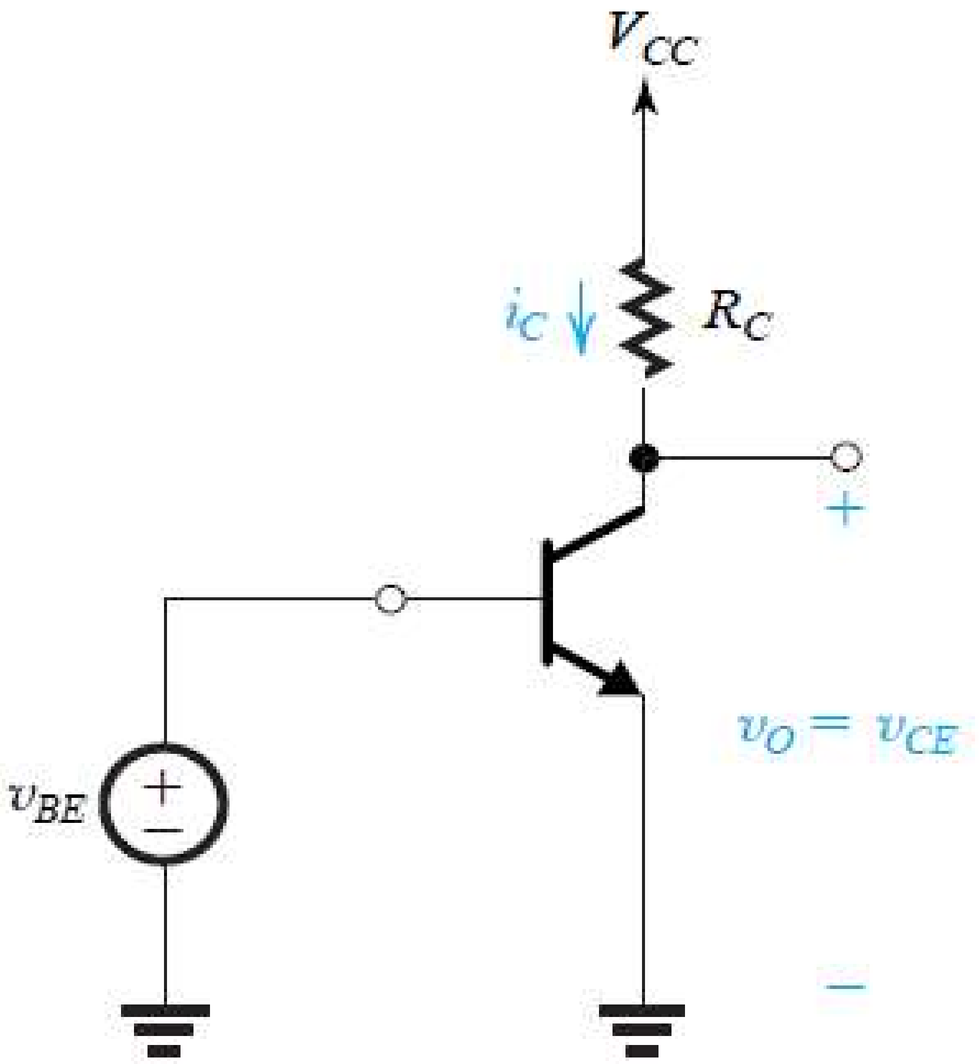
Applying the BJT in Amplifier Design-Voltage Amplifier

(a) Simple BJT amplifier with input *vBE and output vCE.*



- ❖**Voltage-controlled current source** can serve as a **transconductance amplifier**, that is, an amplifier whose input signal is a voltage and whose output signal is a current.
- ❖A simple way to convert a **transconductance amplifier** to a **voltage amplifier** is to pass the **output current** through a **resistor** and take the voltage across the resistor as the output.

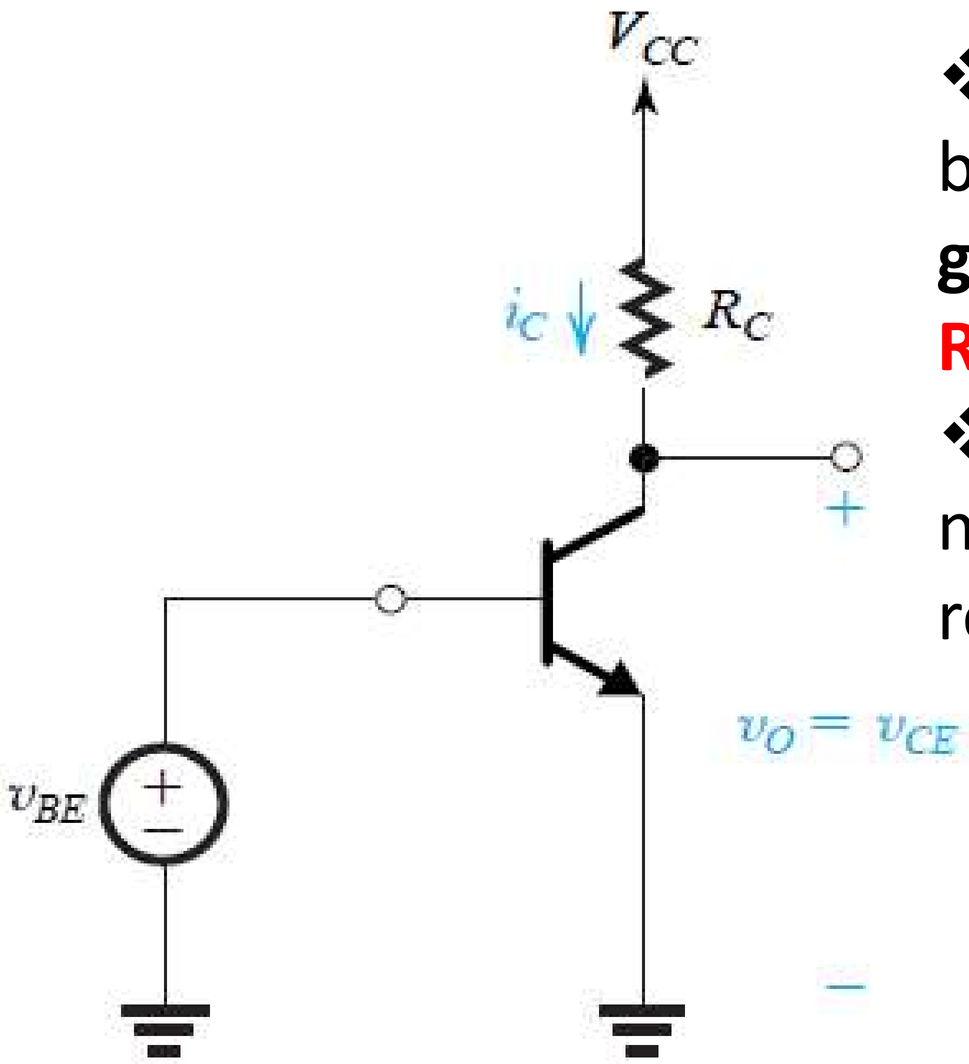
Applying the BJT in Amplifier Design-Voltage Amplifier



(a) Simple BJT amplifier with input *vBE and output vCE.*

Here **vBE** is the input voltage, **Rc** (known as a **load resistance) converts the collector current to** a voltage **(Ic Rc)**, and **Vcc** is the supply voltage that powers up the amplifier and, together with **Rc** , establishes operation in the active mode, as will be shown shortly.

Applying the BJT in Amplifier Design-Voltage Amplifier



(a) Simple BJT amplifier with input *vBE and output vCE.*

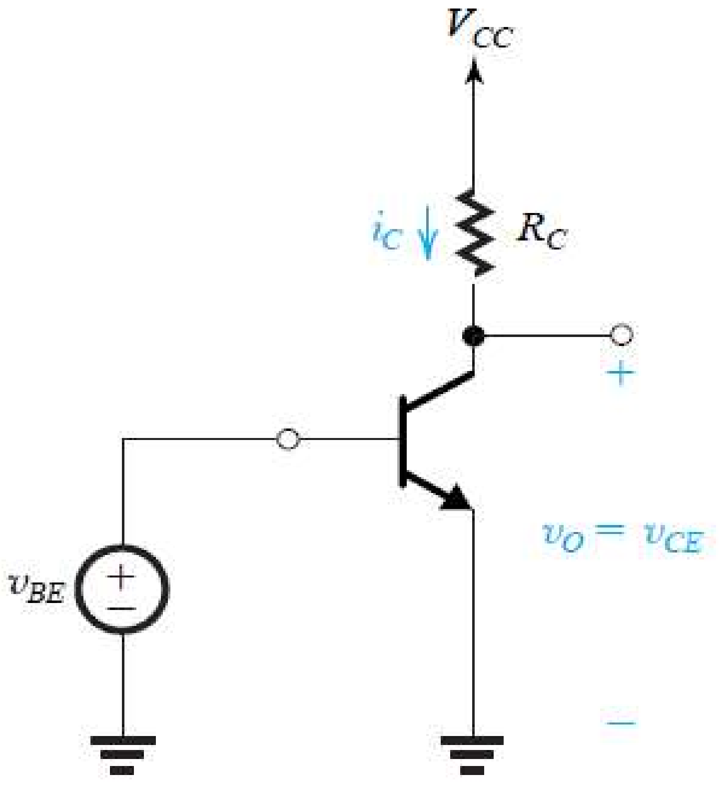
❖The output voltage is taken between the **collector** and **ground**, rather than simply across **Rc**.

❖This is done because of the need to maintain a ground reference throughout the circuit.

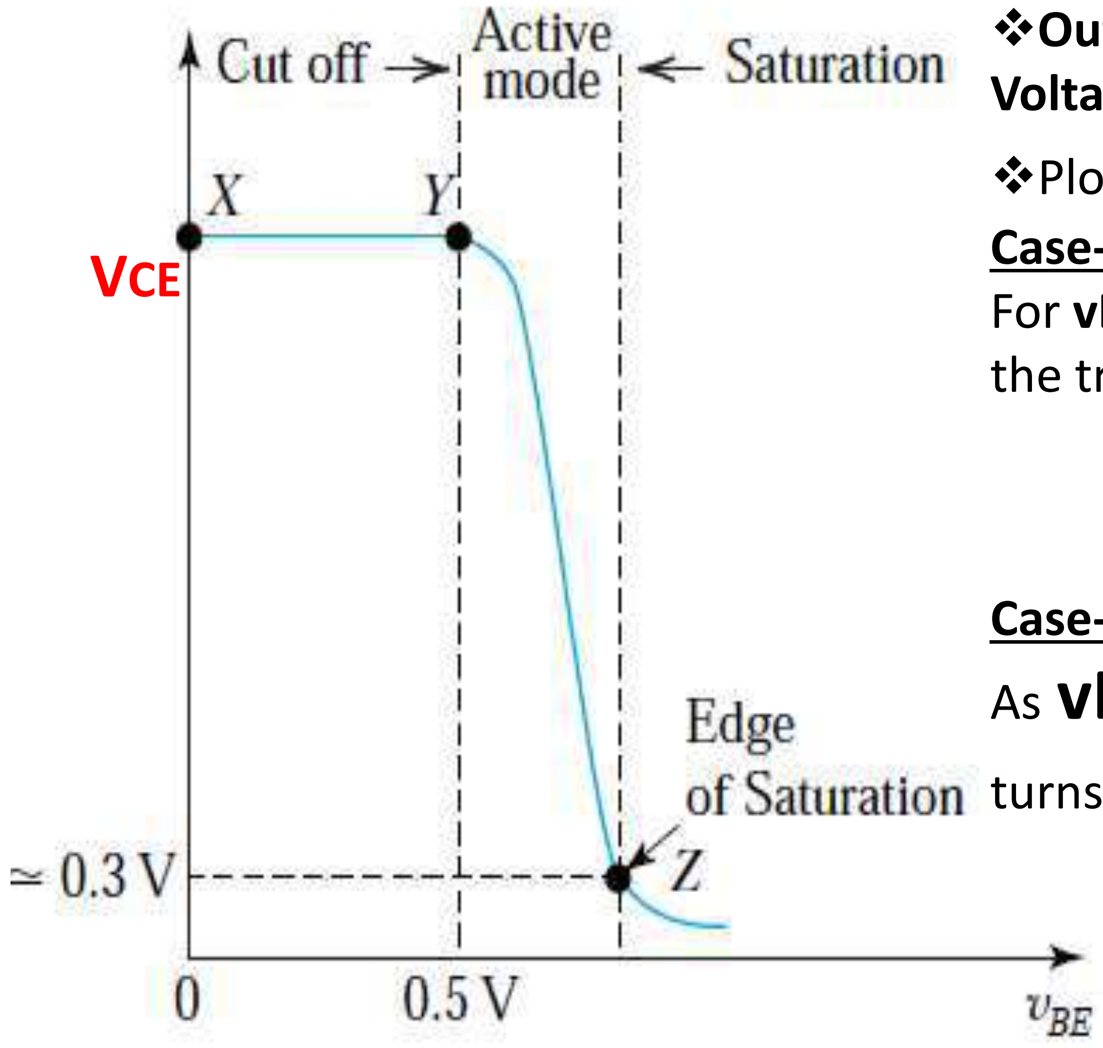
The output voltage is given by

$$\boxed{v_{CE} = V_{CC} - i_C R_C}$$

Applying the BJT in Amplifier Design-Voltage Transfer Characteristic (VTC)



(a) **Simple BJT amplifier with input *vBE and output vCE.***



(b) The voltage transfer characteristic(VTC) of the amplifier in **(a).**

❖**Output Voltage** Vs **Input Voltage**.

❖Plot of **vCE** Vs **vBE**

Case-1:

For **vBE** lower than about 0.5 V, the transistor is cut off, **Ic=0.**

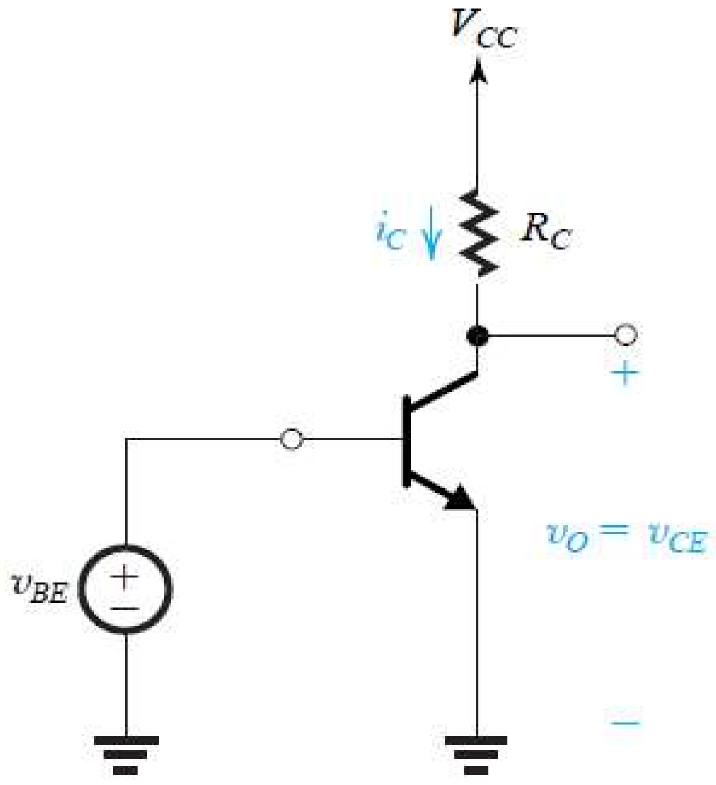
vCE=Vcc-Ic Rc

vCE=Vcc

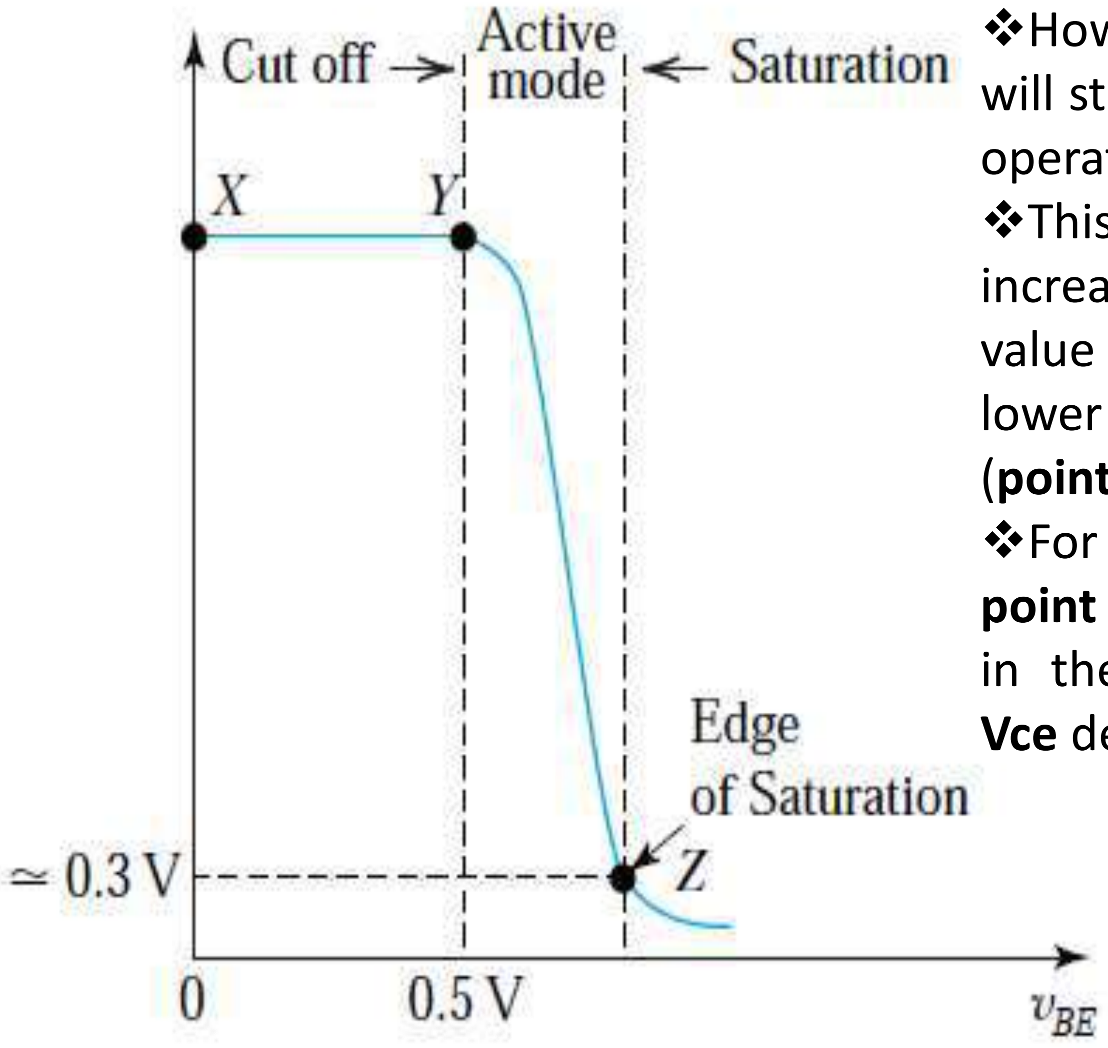
Case-2:

As **vBE** rises , the transistor is turns **ON** and **vCE** decreases.

Applying the BJT in Amplifier Design-Voltage Transfer Characteristic (VTC)



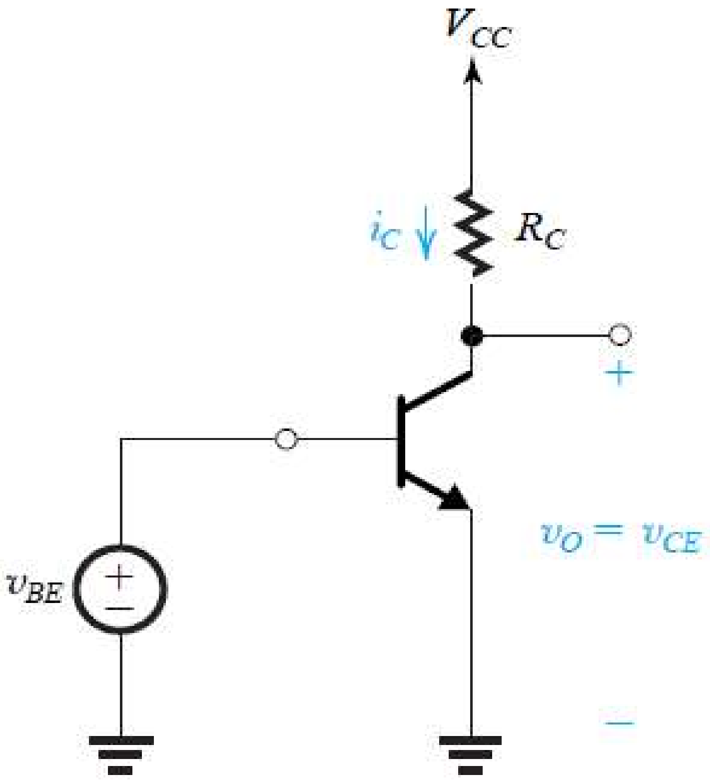
(a) Simple BJT amplifier with input *vBE and output vCE.*



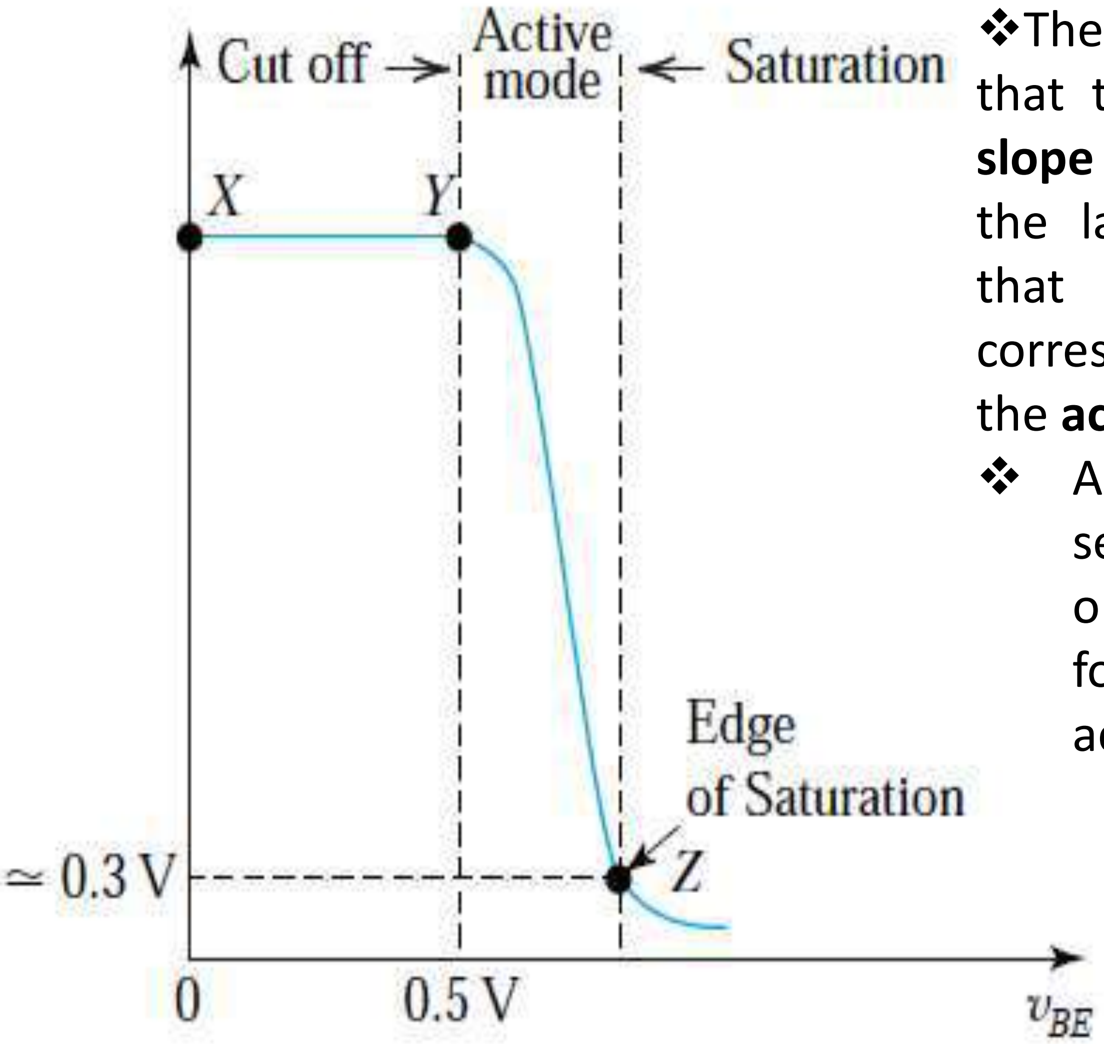
(b) The voltage transfer characteristic(VTC) of the amplifier in **(a).**

- ❖However, since initially **Vce** will still be high, the BJT will be operating in the active mode.
- ❖This continues as **Vbe** is increased until it reaches a value that results in becoming lower than by **0.4 volt** or so (**point Z** on the VTC in Fig. b).
- ❖For **greater than** that at **point Z**, the transistor operates in the **saturation region** and **Vce** decreases very slowly.

Applying the BJT in Amplifier Design-Voltage Transfer Characteristic (VTC)



(a) Simple BJT amplifier with input *vBE and output vCE.*

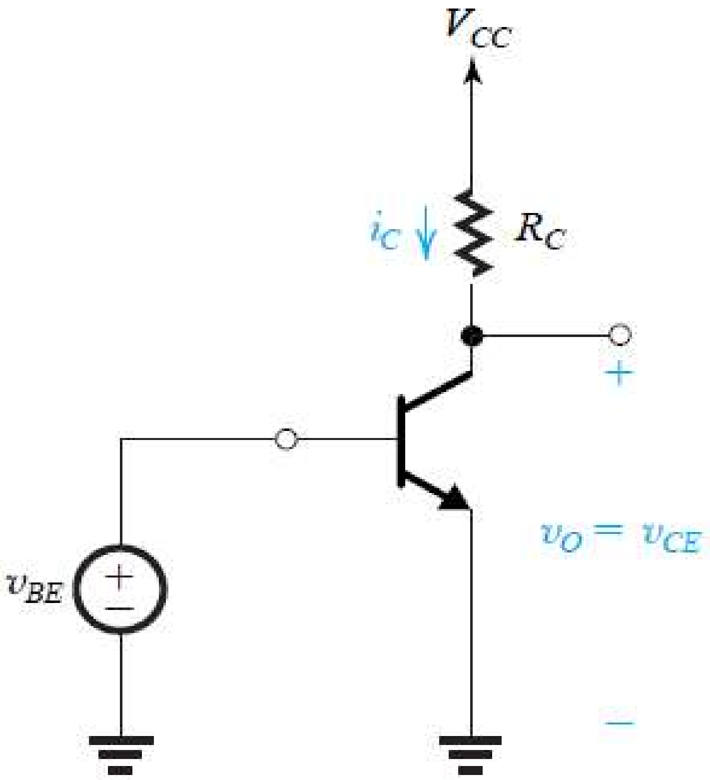


(b) The voltage transfer characteristic(VTC) of the amplifier in **(a).**

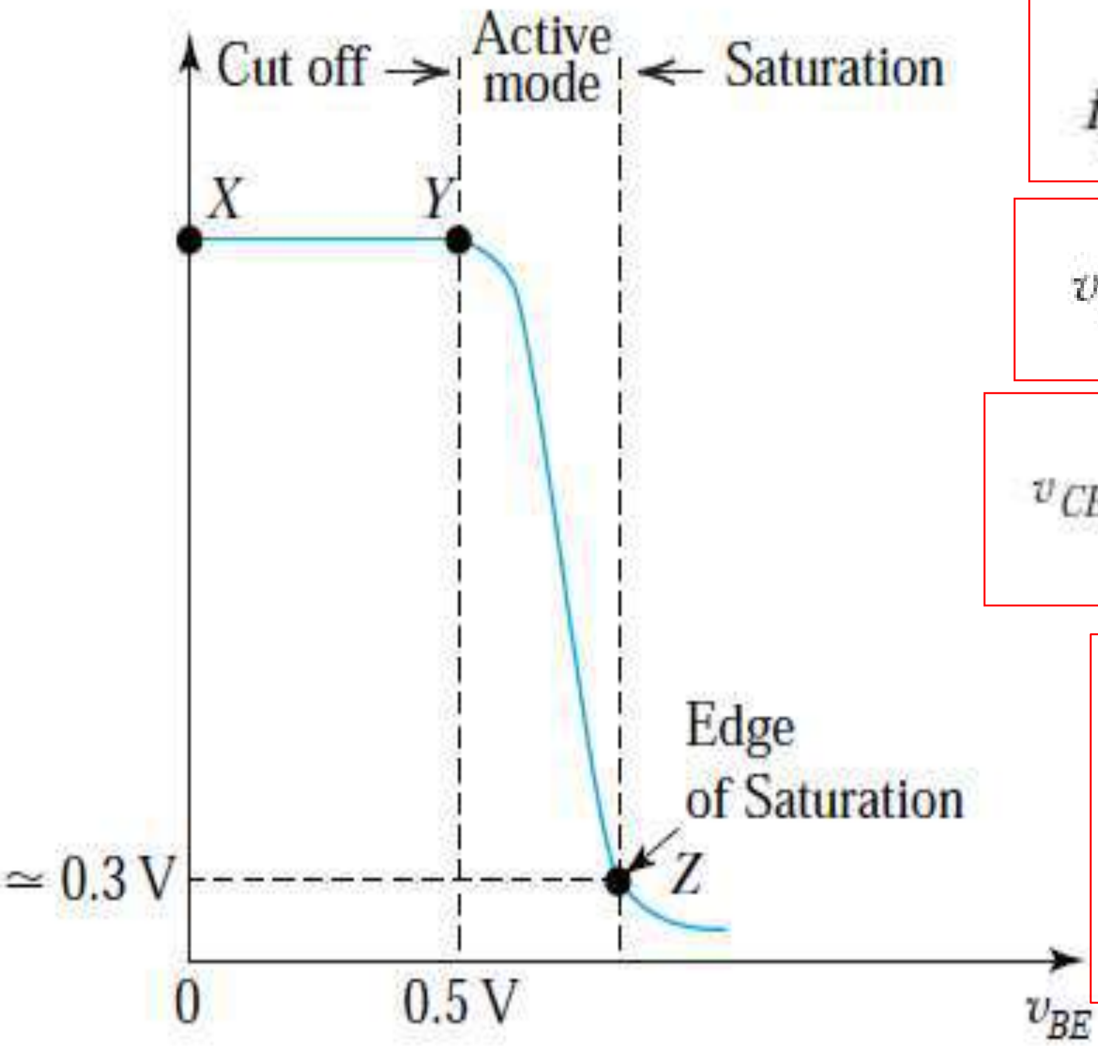
- ❖The VTC in Fig.(b) indicates that the **segment** of **greatest slope** (and hence potentially the largest amplifier gain) is that labeled YZ, which corresponds to operation in the **active mode**.
- ❖ An expression for the segment YZ can be obtained by substituting for **Ic** in Eq. (6.24) by its active-mode value.

$$\boxed{i_C = I_S\ e^{v_{BE}/V_T}}$$

Applying the BJT in Amplifier Design-Voltage Transfer Characteristic (VTC)



(a) Simple BJT amplifier with input *vBE and output vCE.*



(b) The voltage transfer characteristic(VTC) of the amplifier in **(a).**

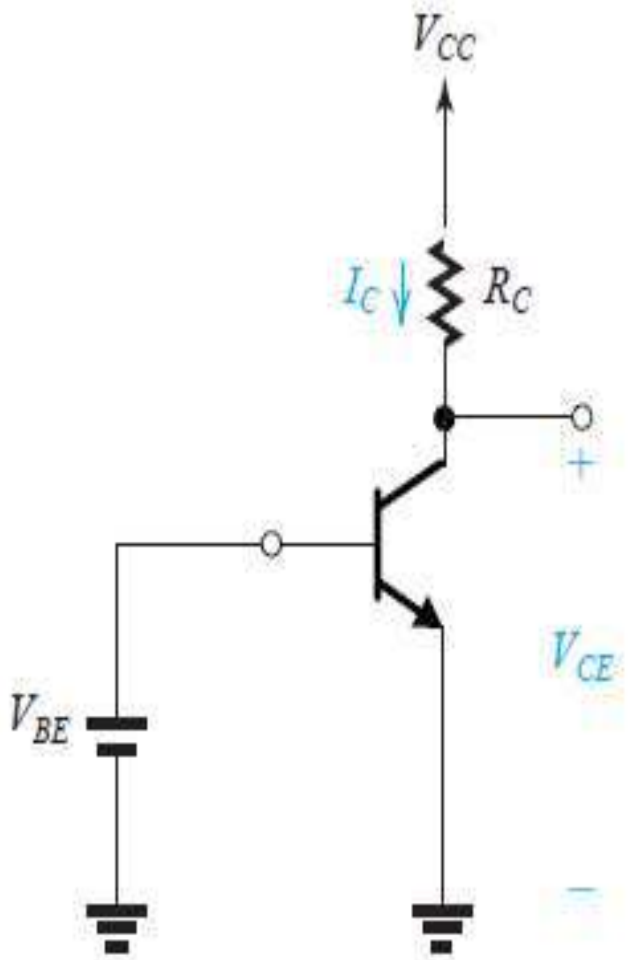
$$i_C = I_S\, e^{v_{BE}/V_T}$$

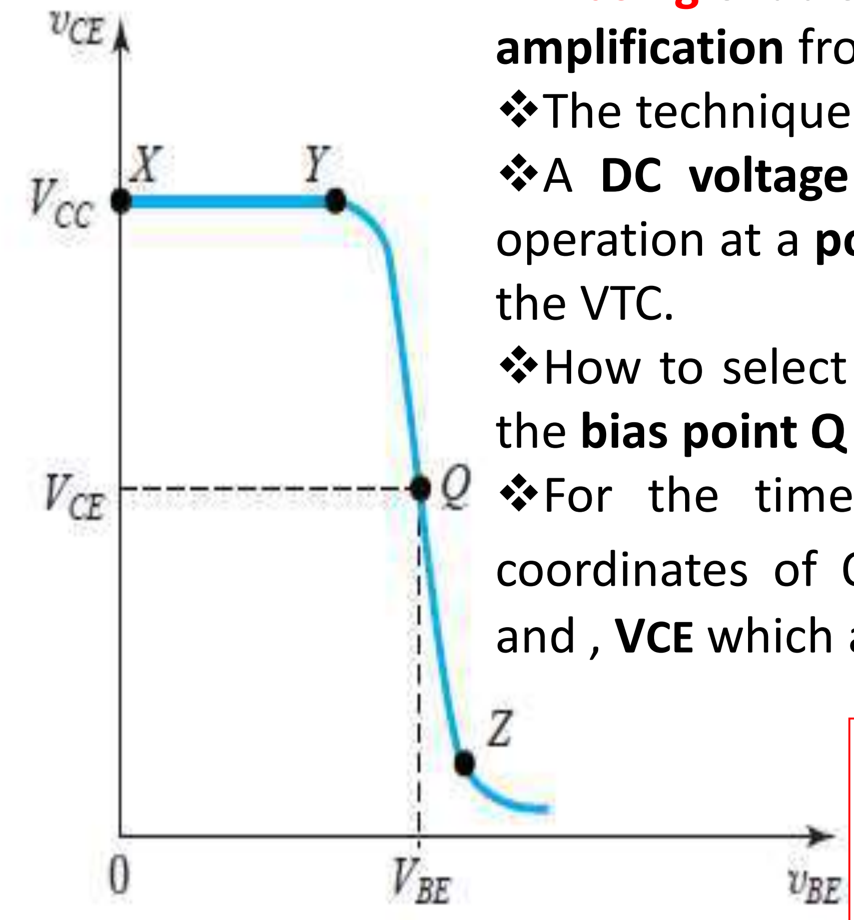
$$v_{CE} = V_{CC} - i_C R_C$$

$$v_{CE} = V_{CC} - R_C I_S\, e^{v_{BE}/V_T}$$

- ❖This is obviously a **nonlinear relationship**.
- ❖Nevertheless, **linear (or almost-linear) amplification** can be obtained by using the technique of biasing the BJT.

Applying the BJT in Amplifier Design- Biasing the BJT to Obtain Linear Amplification



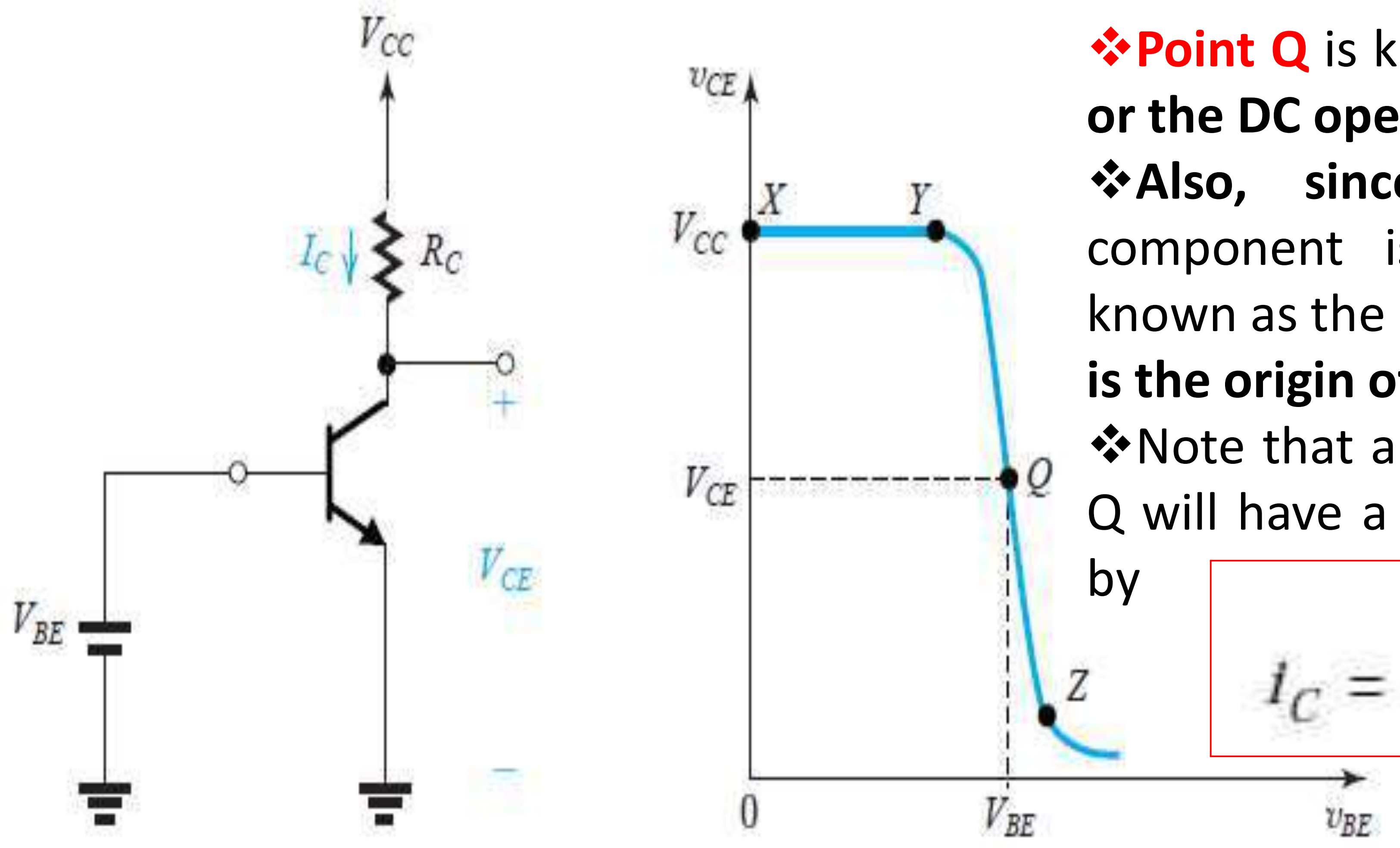


- ❖**Biasing** enables us to obtain **almost-linear amplification** from the BJT.
- ❖The technique is illustrated in Fig.(a).
- ❖A **DC voltage VBE** is selected to obtain operation at a **point Q** on the **segment YZ** of the VTC.
- ❖How to select an appropriate location for the **bias point Q** will be discussed shortly.
- ❖For the time being, observe that the coordinates of Q are the dc voltages **VBE** and , **VCE** which are related by

$$\boxed{v_{CE} = V_{CC} - R_C I_S \, e^{v_{BE}/V_T}}$$

(a) Biasing the BJT amplifier at a point Q located on the active-mode segment of the VTC.

Applying the BJT in Amplifier Design- Biasing the BJT to Obtain Linear Amplification



❖**Point Q** is known as the **bias point or the DC operating point.**

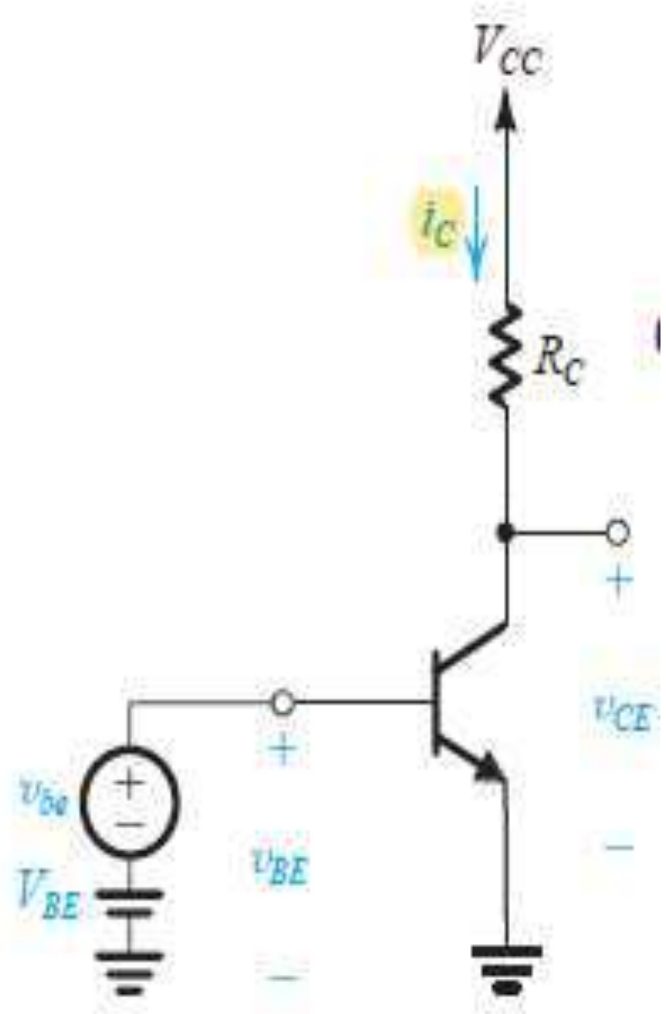
❖**Also, since at Q no signal** component is present, it is also known as the **quiescent point (which is the origin of the** symbol Q).

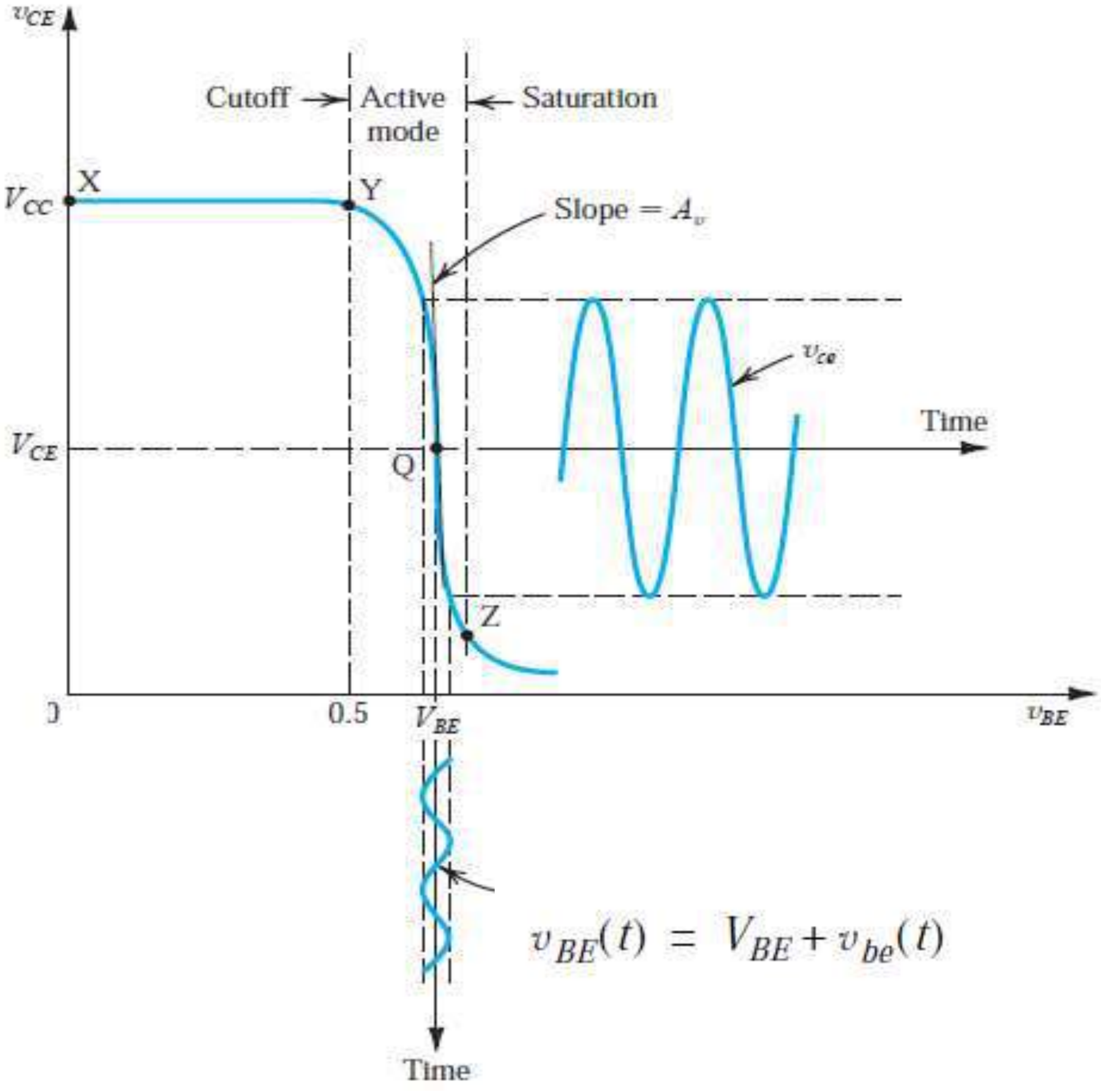
❖Note that a transistor operating at Q will have a collector current given by

$$\boxed{i_C = I_S\, e^{v_{BE}/V_T}}$$

(a) Biasing the BJT amplifier at a point Q located on the active-mode segment of the VTC.

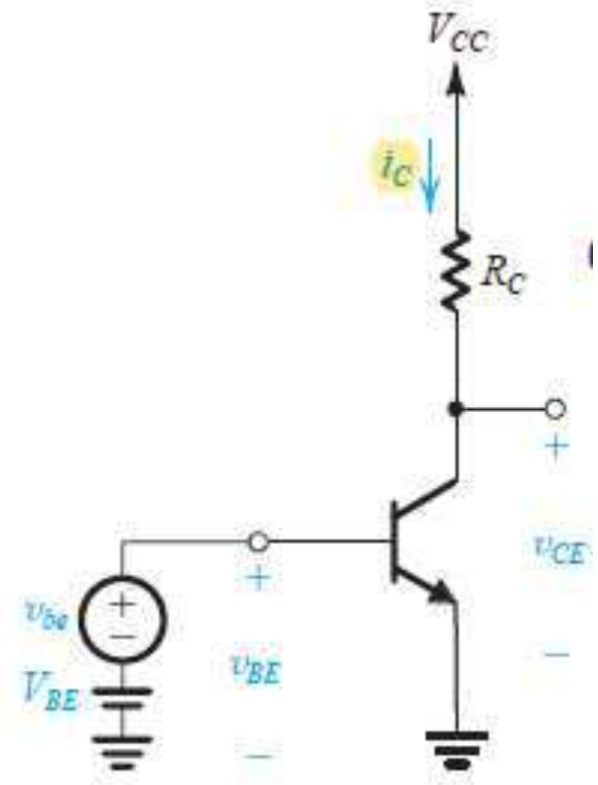
Applying the BJT in Amplifier Design- **Biasing the BJT to Obtain Linear Amplification**

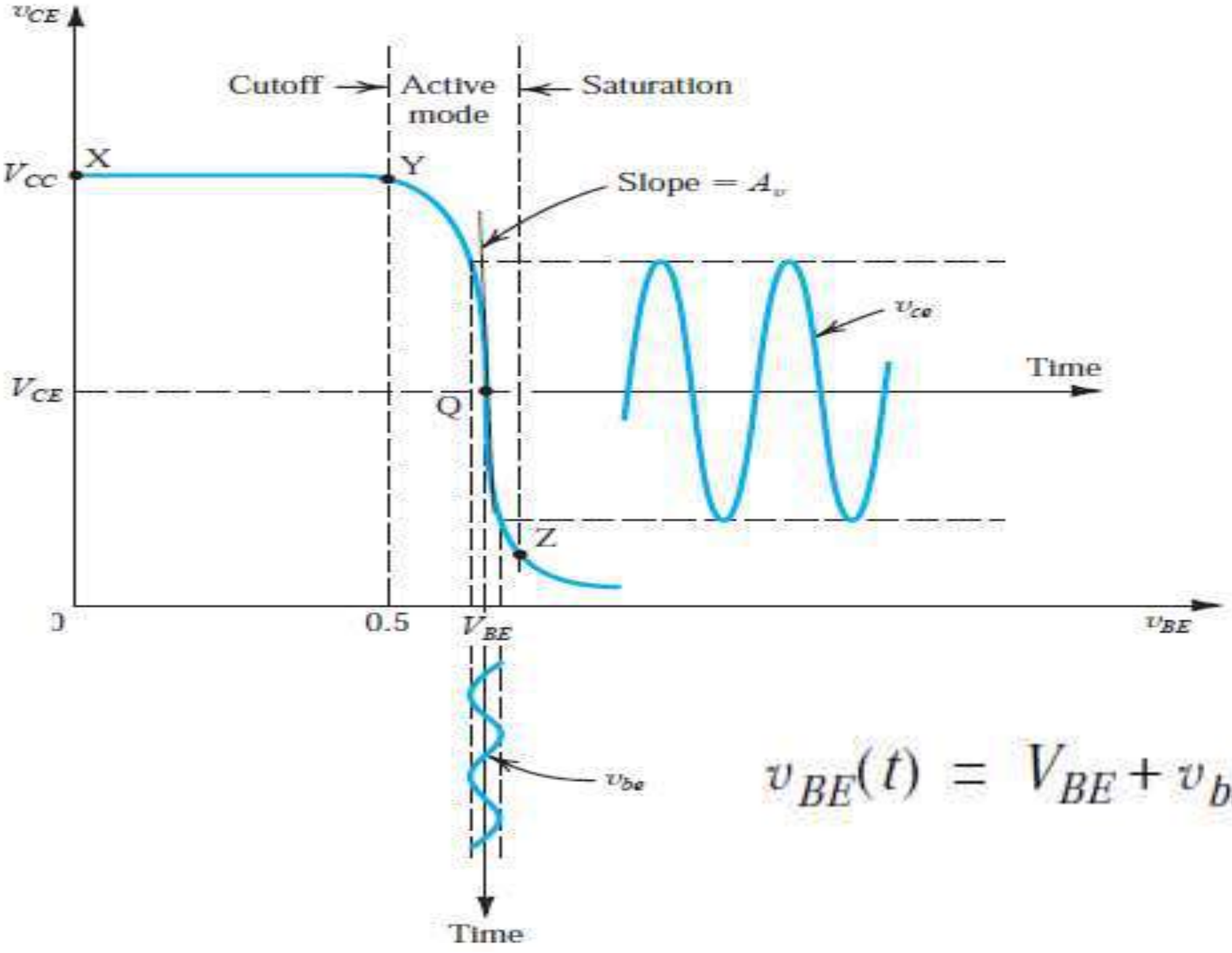




- ❖BJT amplifier biased at a point Q, with a **small voltage signal *vbe*** *superimposed on the **DC bias voltage VBE**.*
- ❖The resulting **Output Signal *vce*** *appears superimposed on the **DC collector voltage VCE**.*
- ❖*The **amplitude of vce** is larger than* that of ***vbe*** *by the voltage gain Av.*

Applying the BJT in Amplifier Design- Biasing the BJT to Obtain Linear Amplification





$$v_{BE}(t) = V_{BE} + v_{be}(t)$$

Applying the BJT in Amplifier Design- Small-Signal Voltage Gain

- If the input signal **Vbe** is kept small, the corresponding signal at the output **Vce** will be nearly proportional to with the constant of proportionality being the slope of the almost-linear segment of the VTC around Q.
- This is the voltage gain of the amplifier, and its value can be determined by evaluating the slope of the tangent to the VTC at the bias point Q,

$$A_v \equiv \left.\frac{dv_{CE}}{dv_{BE}}\right|_{v_{BE} = V_{BE}}$$

$$A_v = -\left(\frac{I_C}{V_T}\right)R_C$$

$$v_{CE} = V_{CC} - R_C I_S\, e^{v_{BE}/V_T}$$

1. The gain is negative, which signifies that the amplifier is inverting; that is, there is a 180 phase shift between the input and the output.

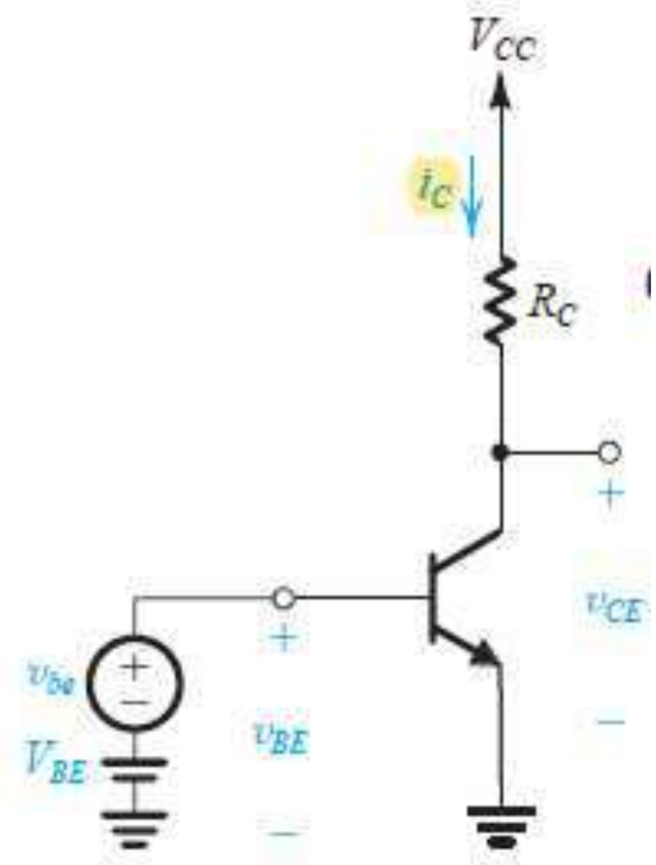
2. The gain is proportional to the collector bias current and to the load resistance.

Applying the BJT in Amplifier Design- Small-Signal Voltage Gain

$$A_v = -\left(\frac{I_C}{V_T}\right)R_C$$

$$A_v = -\frac{I_C R_C}{V_T} = -\frac{V_{RC}}{V_T}$$

$$V_{RC} = V_{CC} - V_{CE}$$



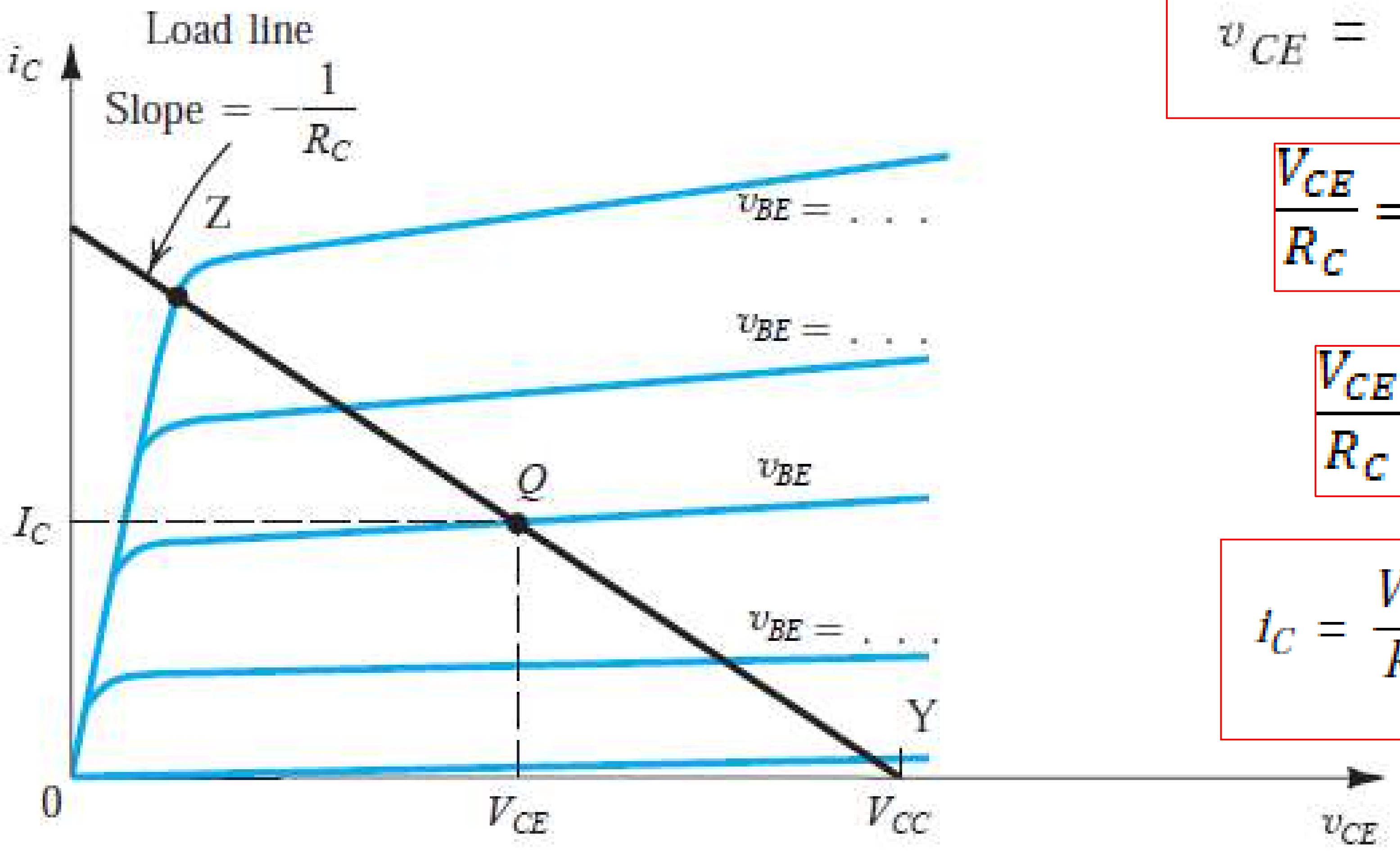
Where *VRC is the dc voltage drop across RC,*

$$A_v = -\frac{V_{CC} - V_{CEsat}}{V_T}$$

$$A_V = -\frac{V_{CC}}{V_T}$$

$$|A_{v\max}| \simeq \frac{V_{CC}}{V_T}$$

Applying the BJT in Amplifier Design- Determining the VTC by Graphical Analysis



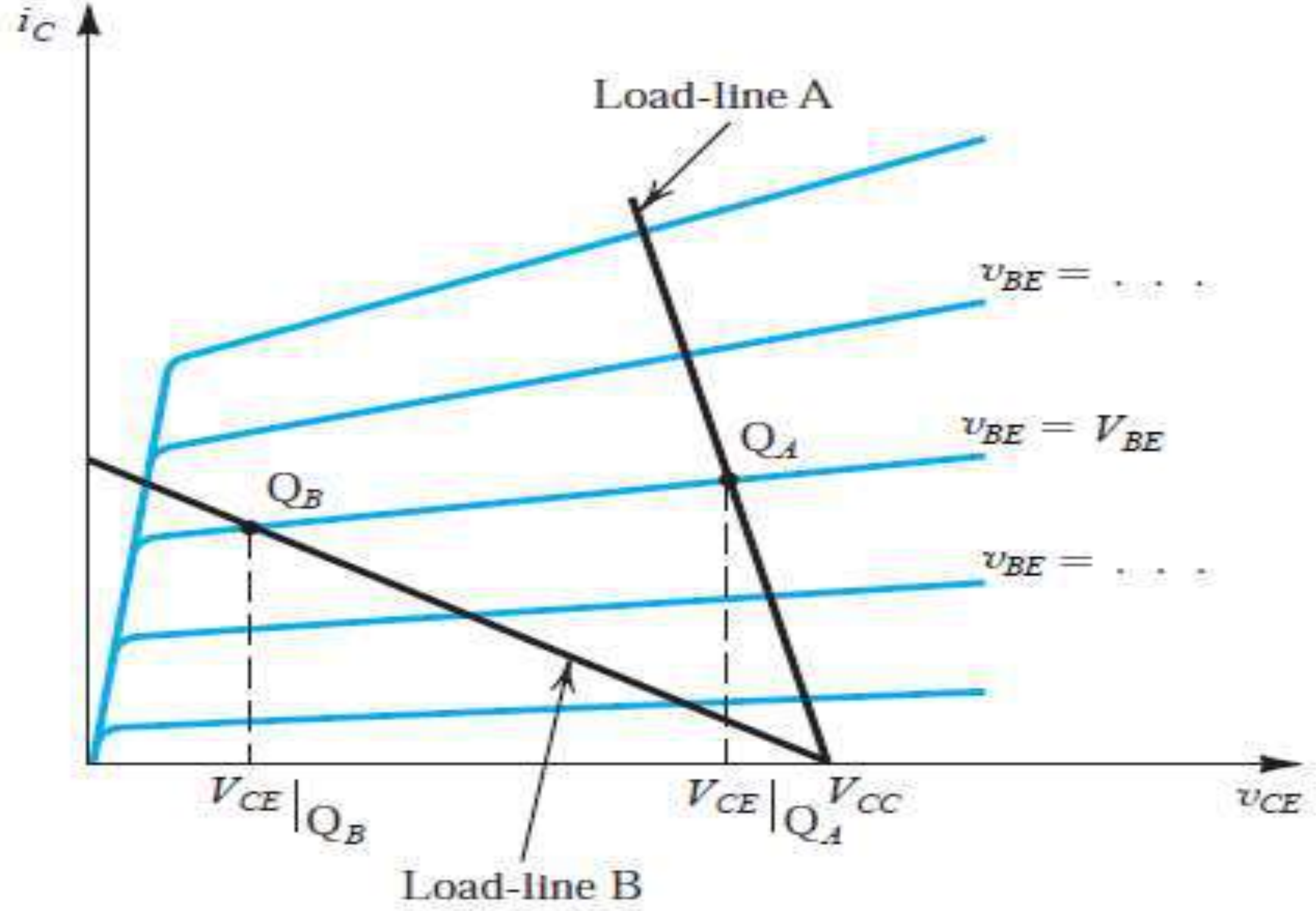
$$\boxed{v_{CE} = V_{CC} - i_C R_C}$$

$$\boxed{\frac{V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \frac{I_C R_C}{R_C}}$$

$$\boxed{\frac{V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - I_C}$$

$$\boxed{i_C = \frac{V_{CC}}{R_C} - \frac{1}{R_C} v_{CE}}$$

Applying the BJT in Amplifier Design- Q-Point

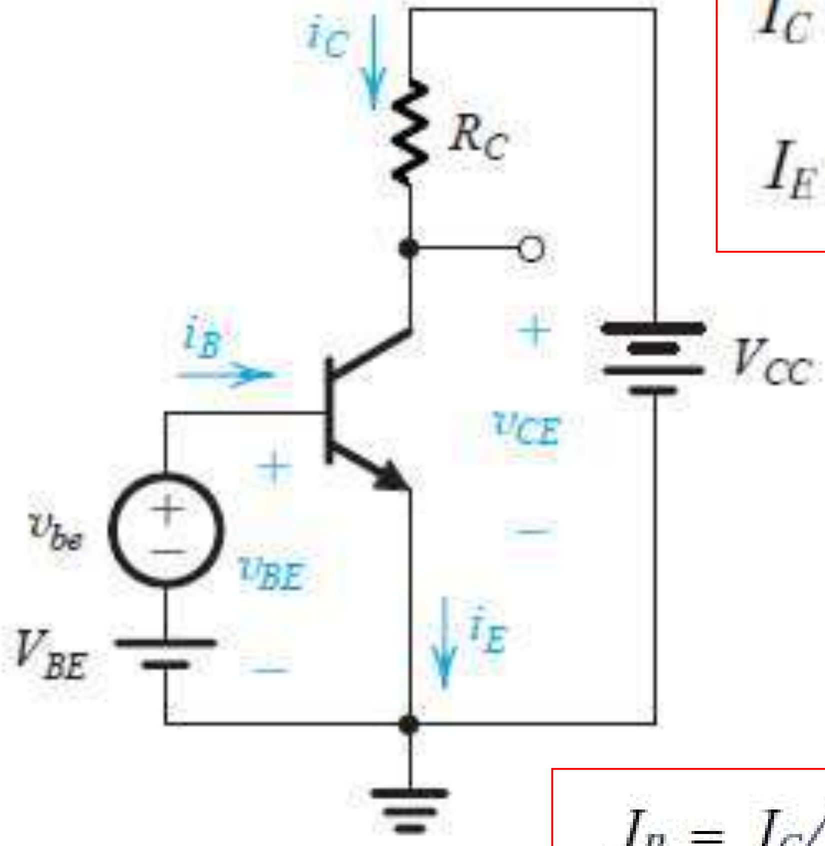


Small-Signal Operation and Models

- Trans-conductance
- Input Resistance at the Base
- Input Resistance at the Emitter
- Voltage Gain
- Separating the Signal and the DC Quantities

- Hybrid-π Model
- T Model

Small-Signal Operation and Models



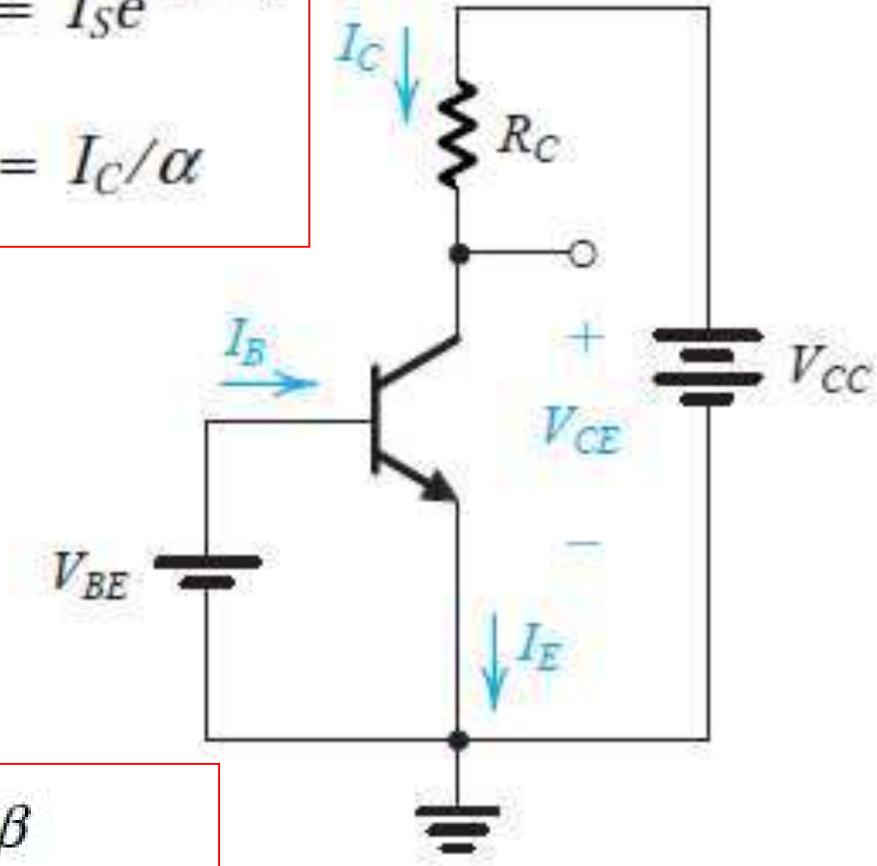
(a)

$$I_C = I_S e^{V_{BE}/V_T}$$

$$I_E = I_C/\alpha$$

$$I_B = I_C/\beta$$

$$V_{CE} = V_{CC} - I_C R_C$$



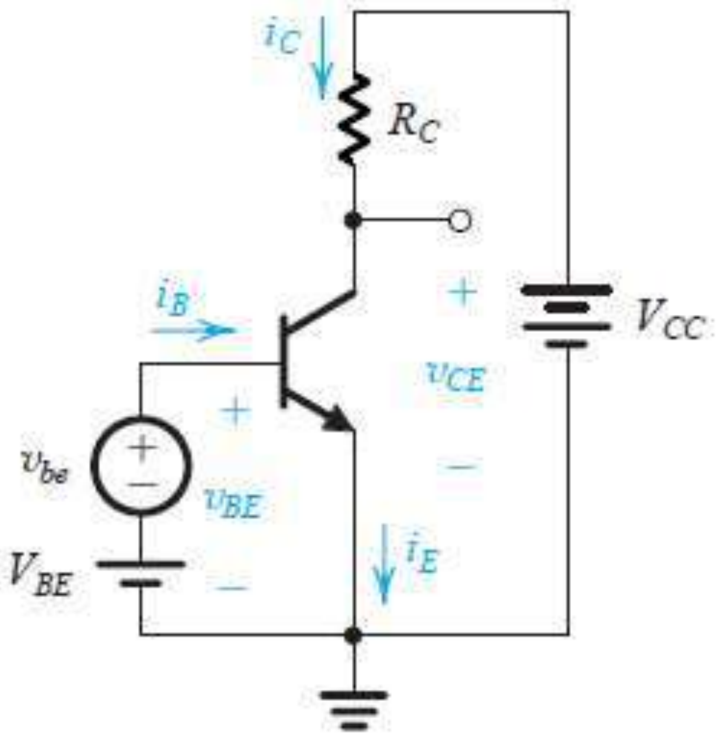
(b)

Transconductance

$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \cdots + \frac{x^n}{n!} + \cdots$$

vBE = VBE + vbe-----(1)

$$i_C = I_S e^{v_{BE}/V_T} = I_S e^{(V_{BE}+v_{be})/V_T}$$
$$= I_S e^{V_{BE}/V_T} e^{v_{be}/V_T}$$



(a)

$$i_C = I_C e^{v_{be}/V_T}$$ ***-----(2)***

If *vbe < VT,*

$$e^{\frac{v_{be}}{V_T}} = 1 + \left(\frac{v_{be}}{V_T}\right) + \frac{\left(\frac{v_{be}}{V_T}\right)}{2!} + \frac{\left(\frac{v_{be}}{V_T}\right)}{3!} + \cdots$$

$$i_C \simeq I_C\left(1 + \frac{v_{be}}{V_T}\right)$$ ***-----(3)***

Transconductance

$$e^{\frac{v_{be}}{V_T}} = 1 + \left(\frac{v_{be}}{V_T}\right) + \frac{\left(\frac{v_{be}}{V_T}\right)}{2!} + \frac{\left(\frac{v_{be}}{V_T}\right)}{3!} + \cdots$$ ***-----(3)***

This approximation, which is valid only for *vbe less than approximately 10 mV, is referred* to as the **small-signal approximation.**

$$\boxed{i_C \simeq I_C\left(1 + \frac{v_{be}}{V_T}\right)} \Rightarrow \boxed{i_C = I_C + \frac{I_C}{V_T} v_{be}}$$ ***-----(4)***

Thus the collector current is composed of the dc bias value *IC and a signal component ic ,*

$$\boxed{i_c = \frac{I_C}{V_T} v_{be}}$$

Transconductance

$$i_c = \frac{I_C}{V_T} v_{be}$$

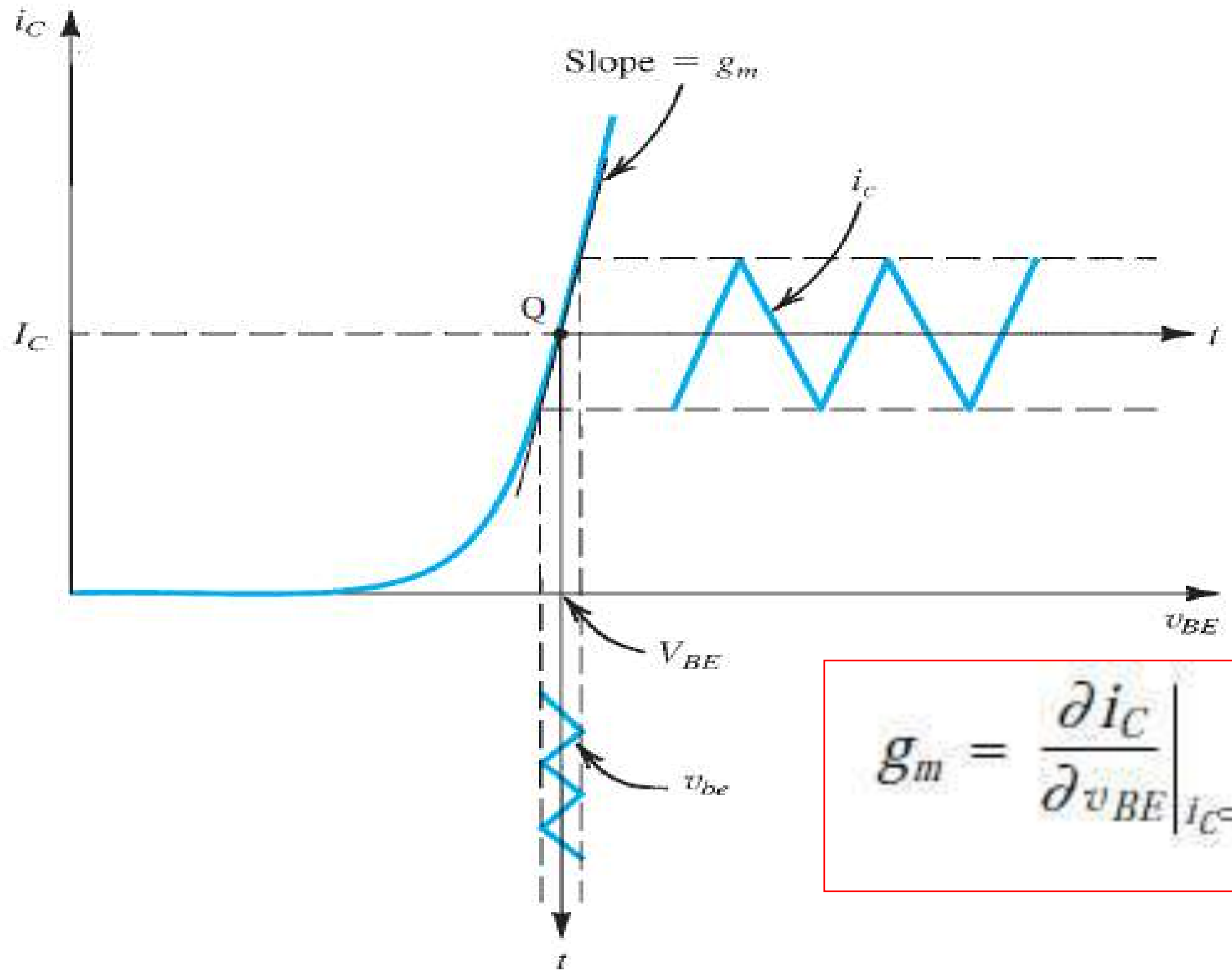
This equation relates the signal current in the collector to the corresponding base–emitter signal voltage. It can be rewritten as

$$i_c = g_m v_{be}$$

$$g_m = \frac{I_C}{V_T}$$

$$g_m = \left. \frac{\partial i_C}{\partial v_{BE}} \right|_{i_C = I_C}$$

Transconductance



$$g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{i_C = I_C}$$

Input Resistance at the Base

$$i_B = \frac{i_C}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta}\frac{I_C}{V_T}v_{be}$$

Thus,

$$i_B = I_B + i_b$$

where *IB is equal Ic/β to and the signal component ib is given by*

$$i_b = \frac{1}{\beta}\frac{I_C}{V_T}v_{be}$$

Substituting for IC/VT by *gm gives*

$$i_b = \frac{g_m}{\beta}v_{be}$$

The small-signal input resistance between base and emitter, *looking into the base, is denoted* by ***rπ*** *and is defined as*

$$r_\pi \equiv \frac{v_{be}}{i_b}$$

$$r_\pi = \frac{\beta}{g_m}$$

$$r_\pi = \frac{V_T}{I_B}$$

Substitute gm and Replace Ic/β by IB

Input Resistance at the Emitter

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha}$$

Thus,

$$i_E = I_E + i_e$$

where *IE is equal to IC /α and the signal current ie is given by*

$$i_e = \frac{i_c}{\alpha} = \frac{I_C}{\alpha V_T} v_{be} = \frac{I_E}{V_T} v_{be}$$

If we denote the **small-signal resistance** between **base** and **emitter** *looking into the emitter by* ***re****, it can be defined as*

$$r_e \equiv \frac{v_{be}}{i_e}$$

$$r_e = \frac{V_T}{I_E}$$

$$r_e = \frac{\alpha}{g_m} \simeq \frac{1}{g_m}$$

Input Resistance at the Emitter

The relationship between ***rπ*** *and* ***re*** *can be found by combining their respective definitions*

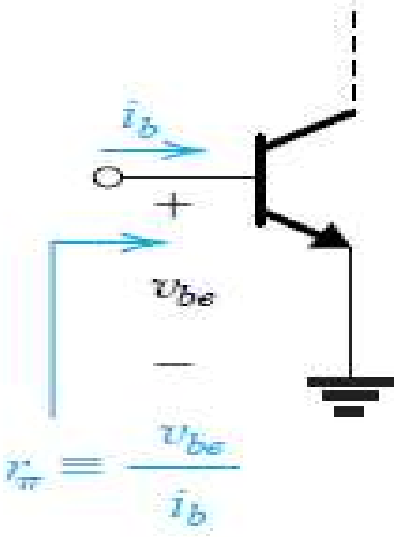
$$\boxed{v_{be} = i_b r_\pi = i_e r_e}$$

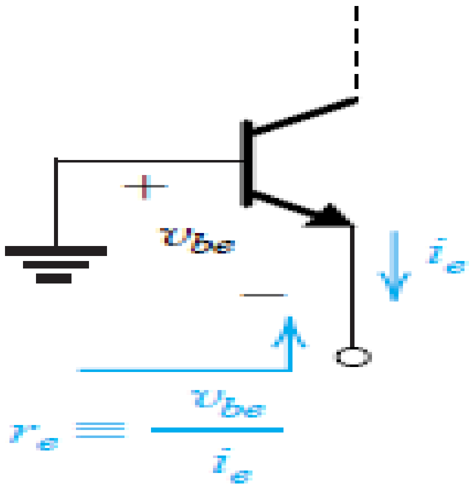
Thus,

$$\boxed{r_\pi = (i_e / i_b) r_e}$$

which yields

$$\boxed{r_\pi = (\beta + 1) r_e}$$





Voltage Gain

$$
\begin{aligned}
v_{CE} &= V_{CC} - i_C R_C \\
&= V_{CC} - (I_C + i_c) R_C \\
&= (V_{CC} - I_C R_C) - i_c R_C \\
&= V_{CE} - i_c R_C
\end{aligned}
$$

Here the quantity *VCE is the dc bias voltage at the collector, and the signal voltage is given by*

$$v_{ce} = -i_c R_C = -g_m v_{be} R_C$$

$$= (-g_m R_C) v_{be}$$

Thus the voltage gain of this amplifier *Av is*

$$A_v \equiv \frac{v_{ce}}{v_{be}} = -g_m R_C$$

$$A_v = -\frac{I_C R_C}{V_T}$$

Small Signal Operation

Transconductance

$$g_m = \frac{I_C}{V_T}$$

$$g_m = \frac{i_c}{V_{be}}$$

$$g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{i_C = I_C}$$

Input Resistance at the Base

$$i_B = I_B + i_b$$

$$r_\pi = \frac{V_T}{I_B}$$

$$r_\pi = \frac{\beta}{g_m}$$

Input Resistance at the Emitter

$$i_E = I_E + i_e$$

$$r_e = \frac{V_T}{I_E}$$

$$r_e = \frac{\alpha}{g_m} \simeq \frac{1}{g_m}$$

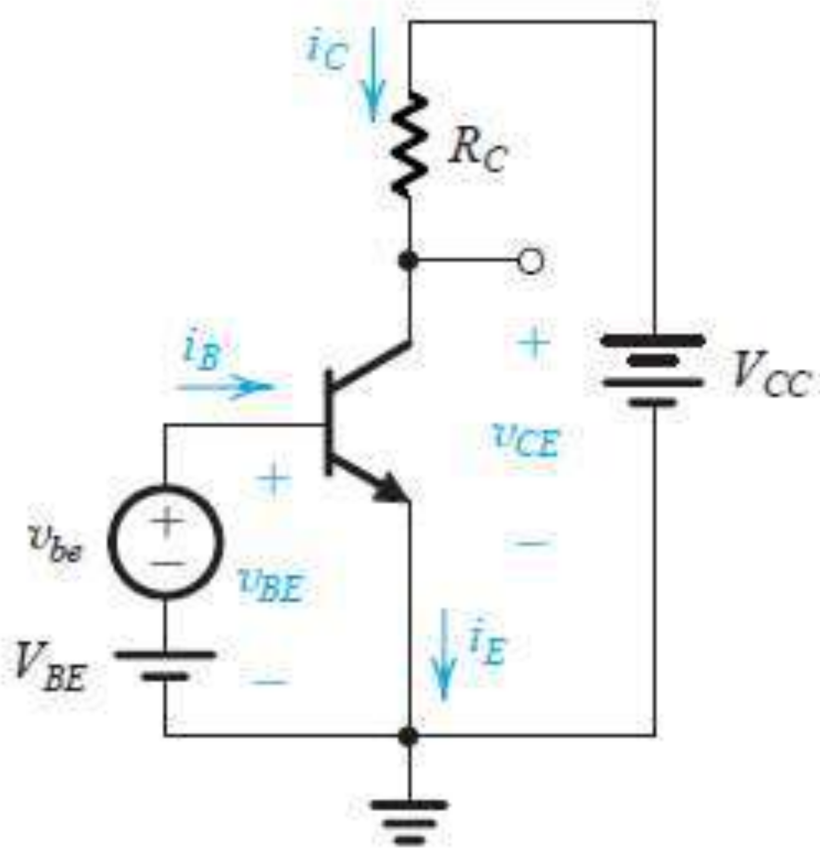
$$r_\pi = (\beta + 1) r_e$$

Voltage Gain

$$A_v \equiv \frac{v_{ce}}{v_{be}} = -g_m R_C$$

$$A_v = -\frac{I_C R_C}{V_T}$$

Separating the Signal and the DC Quantities

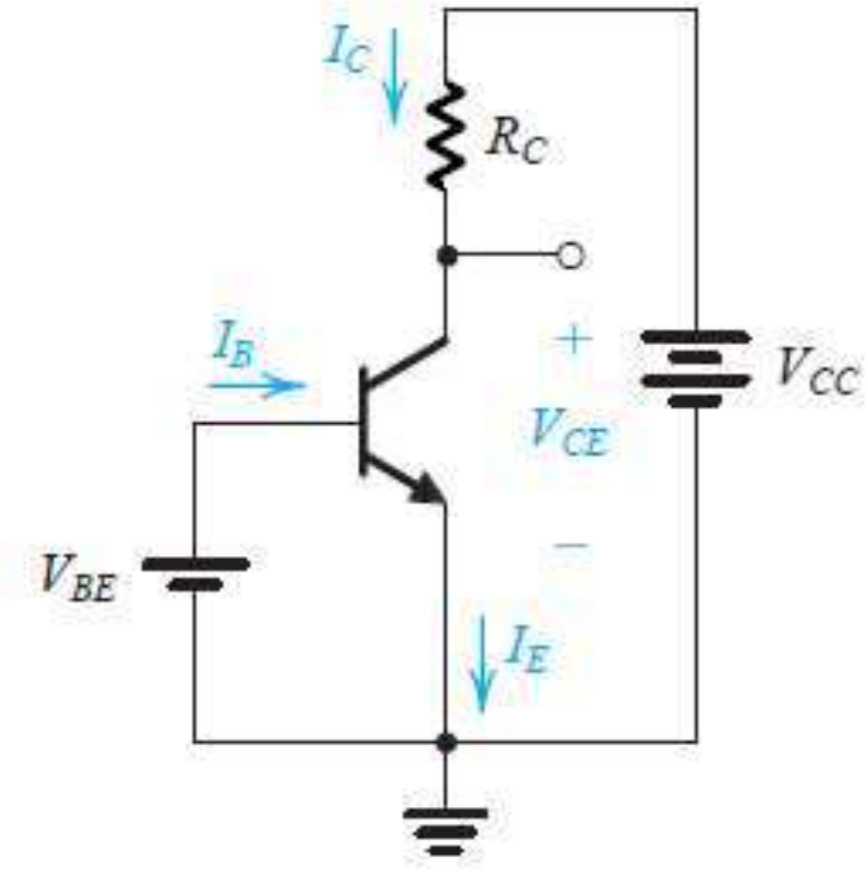


(a)

❖Every current and voltage in the amplifier circuit of Fig.(a) is composed of two components: a dc component and a signal component

❖For instance, *vBE = VBE + vbe, iC = IC + ic, and so on*

Separating the Signal and the DC Quantities



(b)

The dc components are determined from the dc circuit given in Fig. 6.36(b) and from the relationships imposed by the transistor.

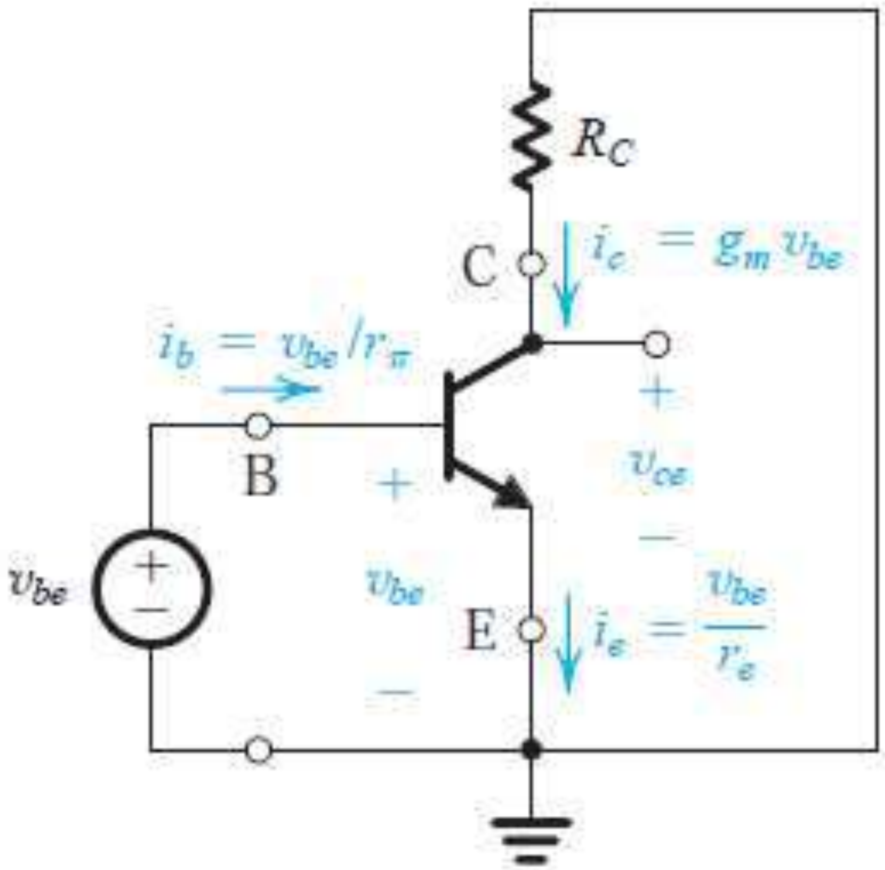
$$I_C = I_S e^{V_{BE}/V_T}$$

$$I_E = I_C/\alpha$$

$$I_B = I_C/\beta$$

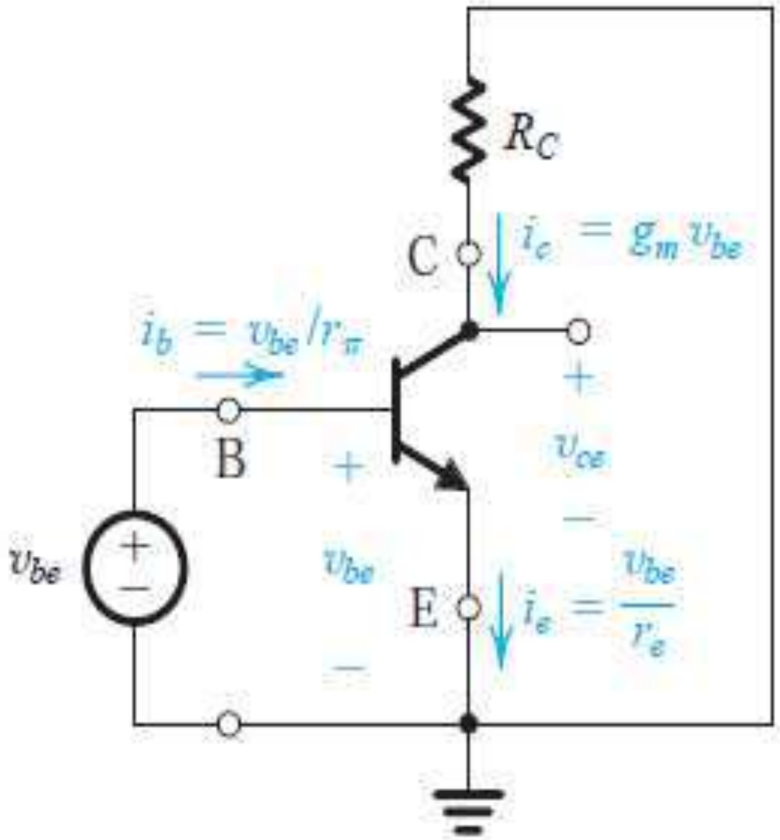
$$V_{CE} = V_{CC} - I_C R_C$$

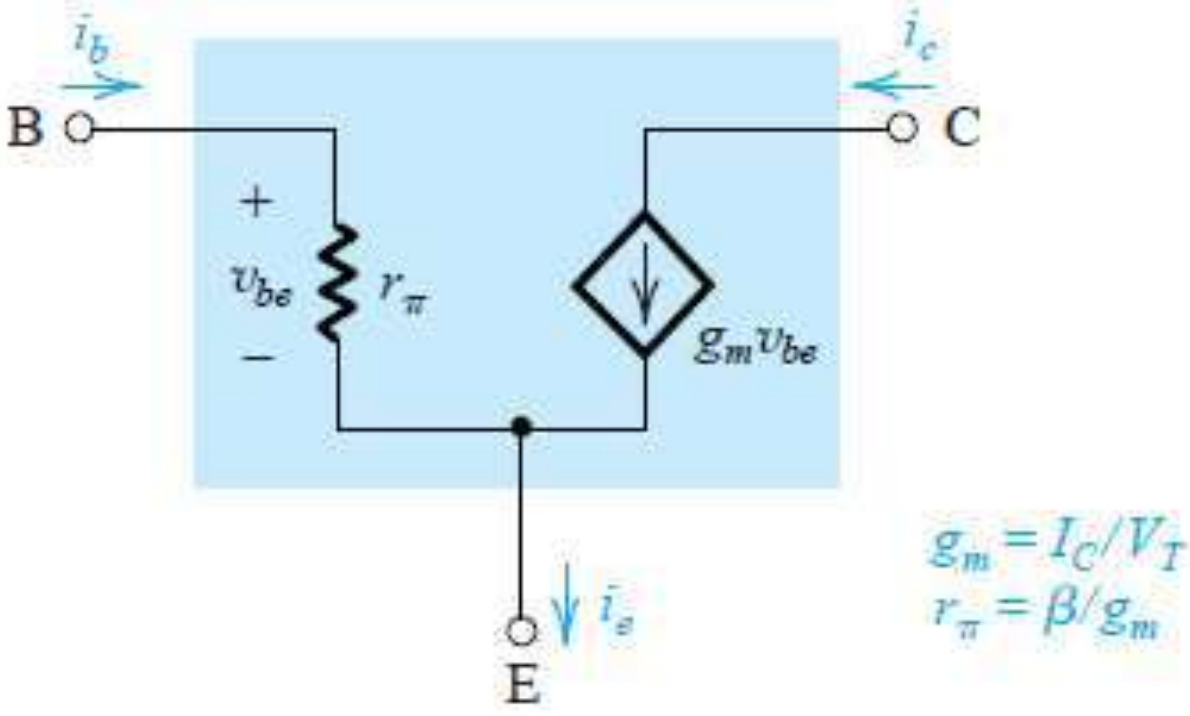
Separating the Signal and the DC Quantities



- ❖On the other hand, a representation of the signal operation of the BJT can be obtained by eliminating the dc sources, as shown in Fig.
- ❖Expressions for the current elements***(ic, ib, and ie)*** *obtained* when a **small signal *vbe*** *is applied.*
- ❖Small-Signal Circuit Model.

HYBRID π MODEL

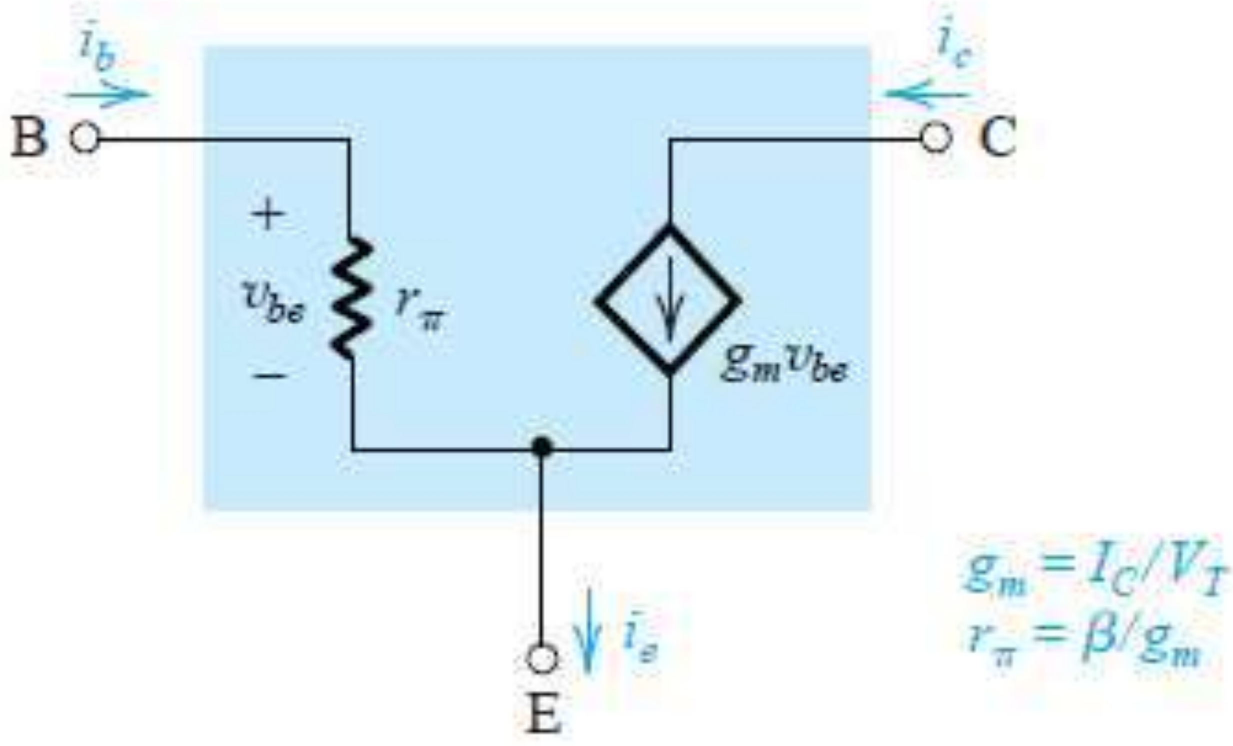




(a)

This model represents the BJT as a **voltage controlled current source** and explicitly includes the input resistance looking into the base , *rπ*

HYBRID π MODEL

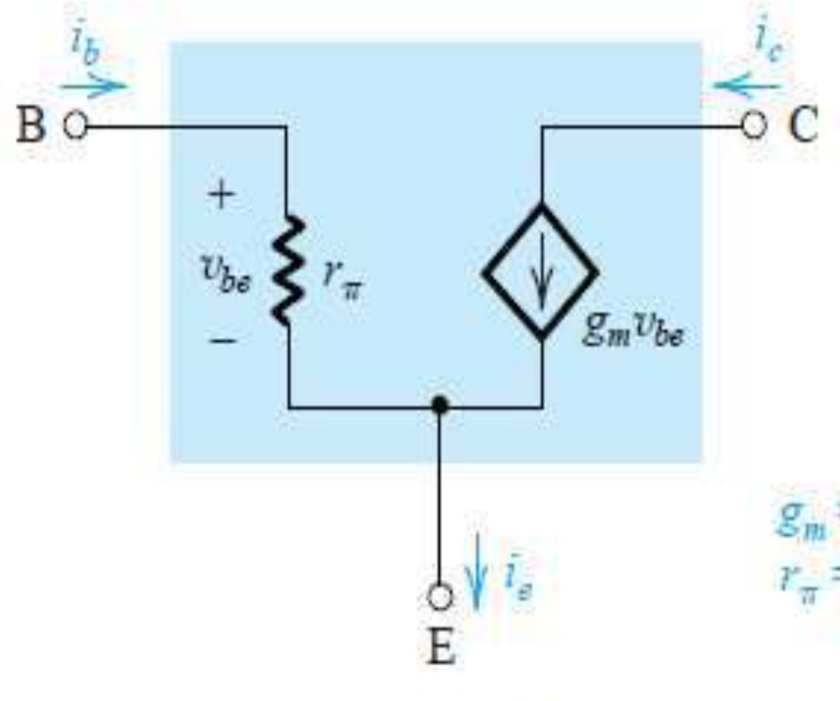


(a)

In this model

$$i_c = g_m v_{be}$$
$$i_b = \frac{v_{be}}{r_\pi}$$

HYBRID π MODEL



(a)

$g_m = I_C/V_T$

$r_\pi = \beta/g_m$

In this model

Ie=ic+ib

$$i_e = \frac{v_{be}}{r_\pi} + g_m v_{be} = \frac{v_{be}}{r_\pi}(1 + g_m r_\pi)$$

But $g_m r_\pi = \beta$

$$= \frac{v_{be}}{r_\pi}(1+\beta) = v_{be} \Big/ \left(\frac{r_\pi}{1+\beta}\right)$$

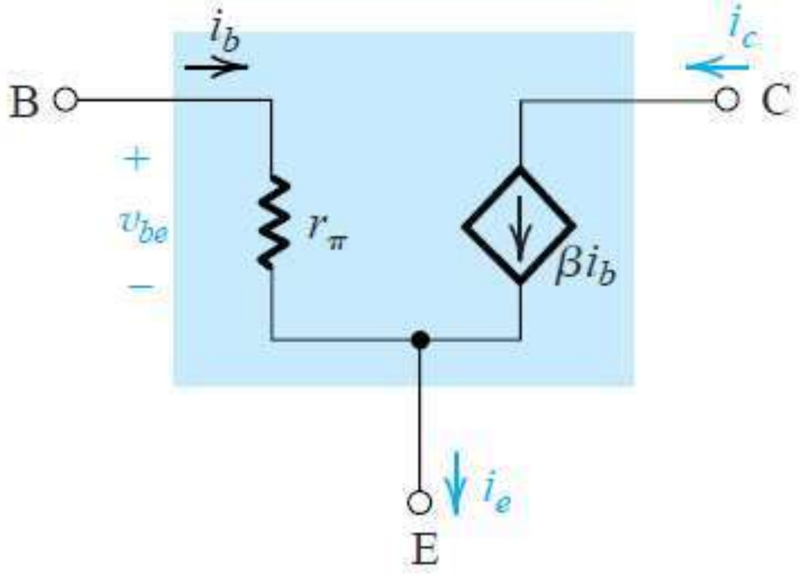
$$= v_{be}/r_e$$

HYBRID π MODEL

Slightly different model can be obtained by expressing the **current of the controlled source ($g_m v_{be}$)** *interms of base current* ***i_b***

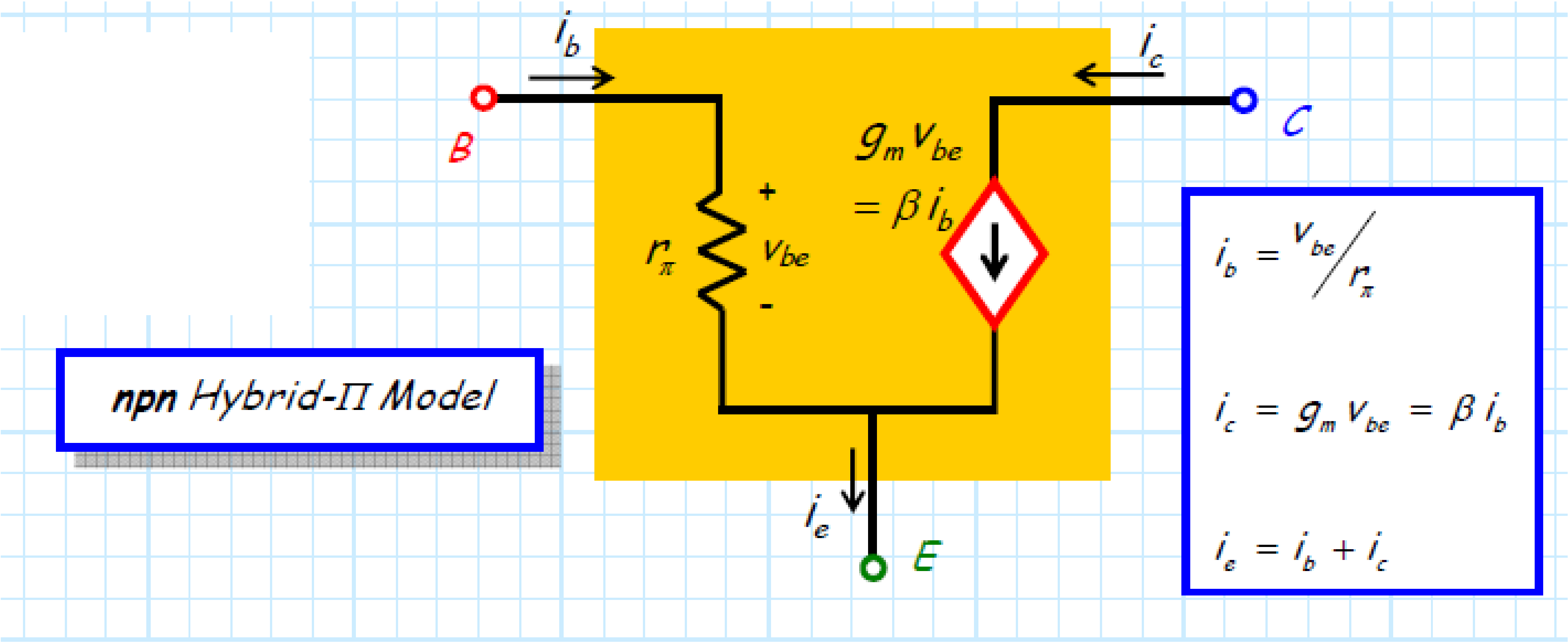
$$g_m v_{be} = g_m(i_b r_\pi) = (g_m r_\pi) i_b = \beta i_b$$

Equivalent circuit model is



Here the transistor is represented as a **current-controlled current source**, with the control current being ***ib***.

HYBRID π MODEL

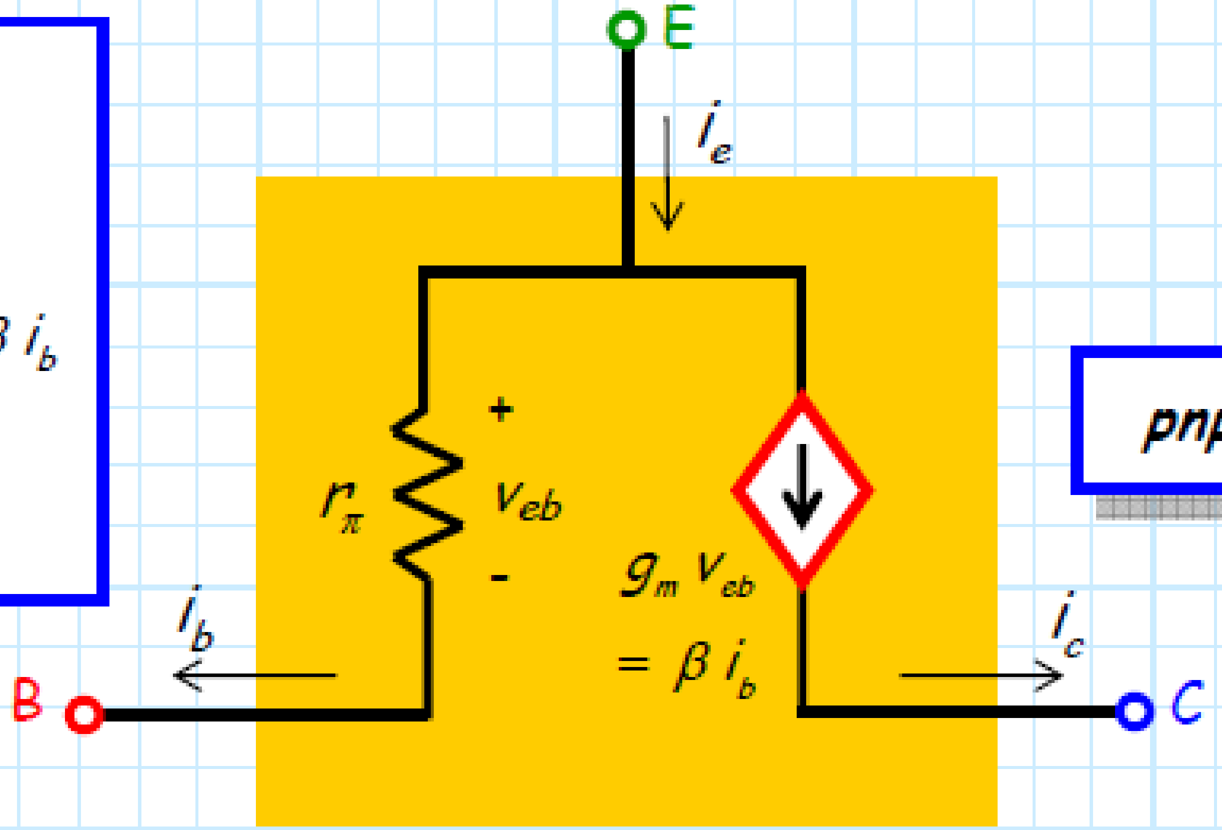


HYBRID π MODEL

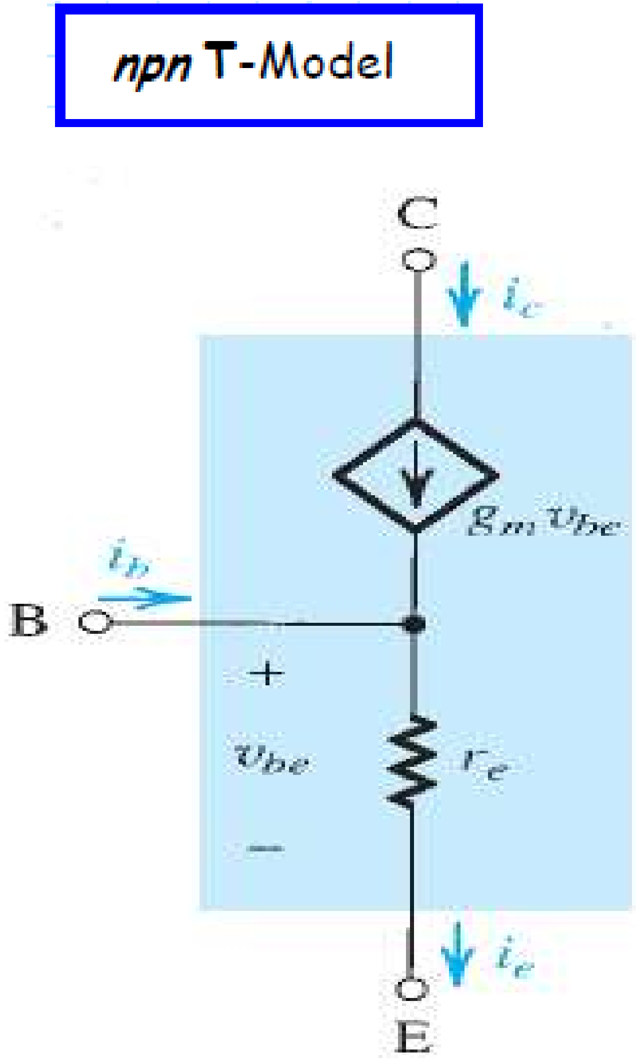
$$i_b = {}^{v_{eb}}\!/_{r_\pi}$$

$$i_c = g_m v_{eb} = \beta\, i_b$$

$$i_e = i_b + i_c$$



pnp **Hybrid-Π Model**



(a)

T Model

Ie=ic+ib

ib=ie-ic

$$i_b = \frac{v_{be}}{r_e} - g_m v_{be} = \frac{v_{be}}{r_e}(1 - g_m r_e)$$

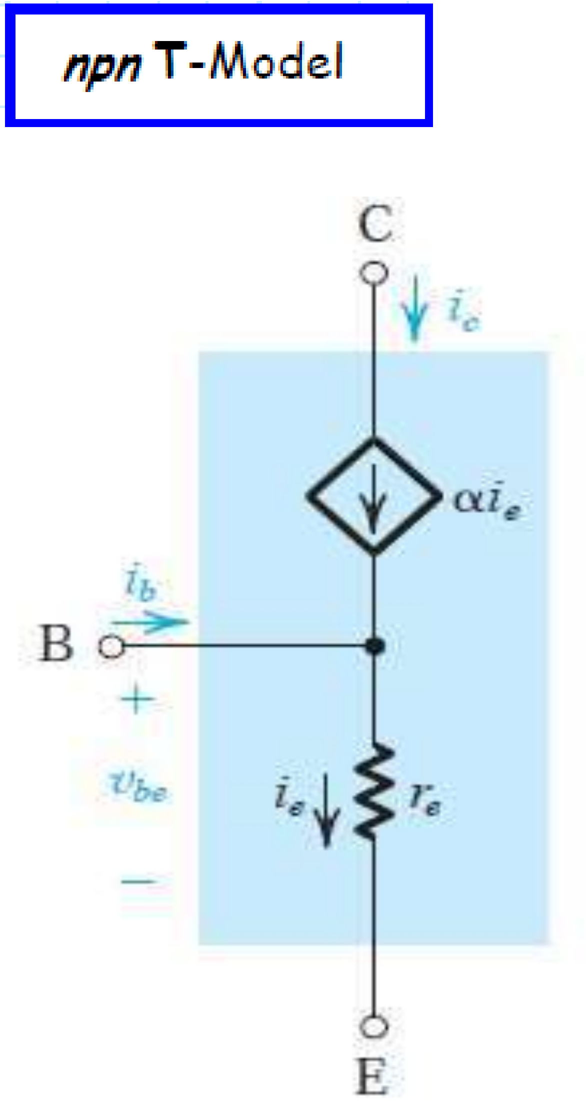
$$= \frac{v_{be}}{r_e}(1-\alpha) = \frac{v_{be}}{r_e}(1 - \frac{\beta}{\beta+1})$$

$$= \frac{v_{be}}{(\beta+1)r_e} = \frac{v_{be}}{r_\pi}$$

The current of the controlled source can be expressed in terms of the emitter current.

$$g_m v_{be} = g_m(i_e r_e)$$

$$= (g_m r_e) i_e = \alpha i_e$$



T Model

$$i_b = \frac{v_{be}}{r_e} - g_m v_{be} = \frac{v_{be}}{r_e}(1 - g_m r_e)$$

$$= \frac{v_{be}}{r_e}(1-\alpha) = \frac{v_{be}}{r_e}(1 - \frac{\beta}{\beta+1})$$

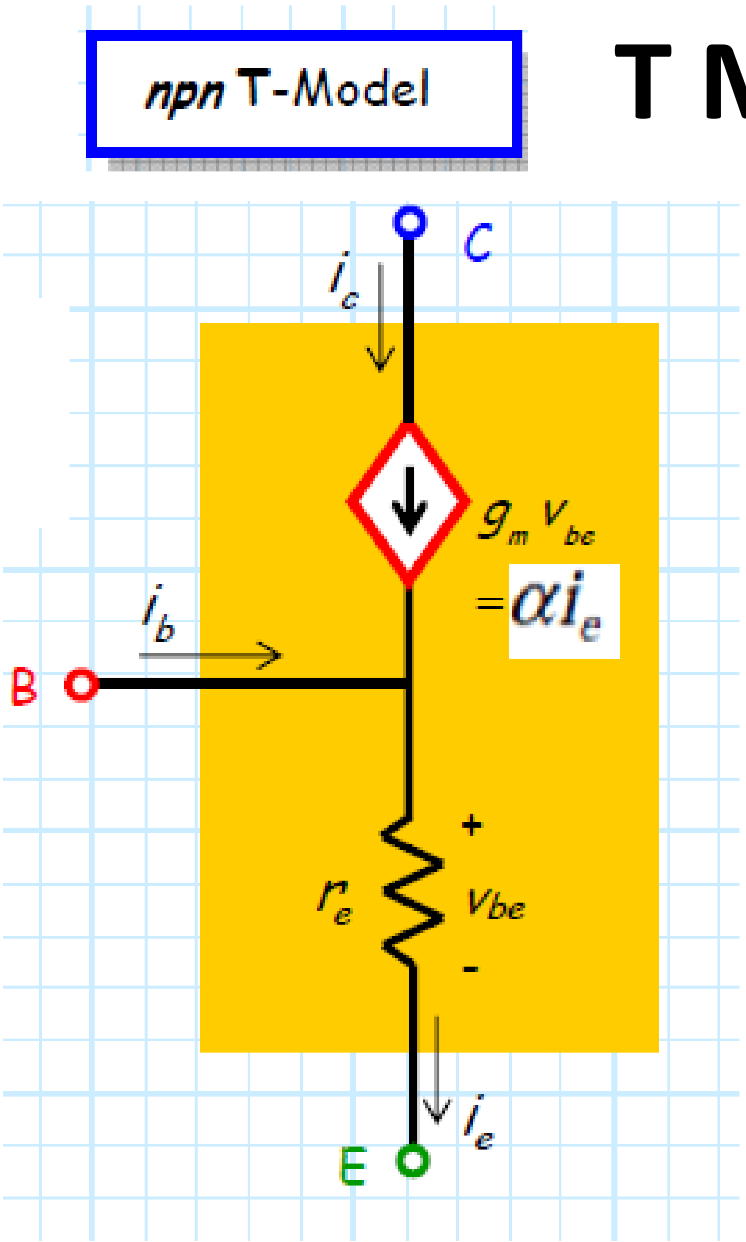
$$= \frac{v_{be}}{(\beta+1)r_e} = \frac{v_{be}}{r_\pi}$$

The current of the controlled source can be expressed in terms of the emitter current.

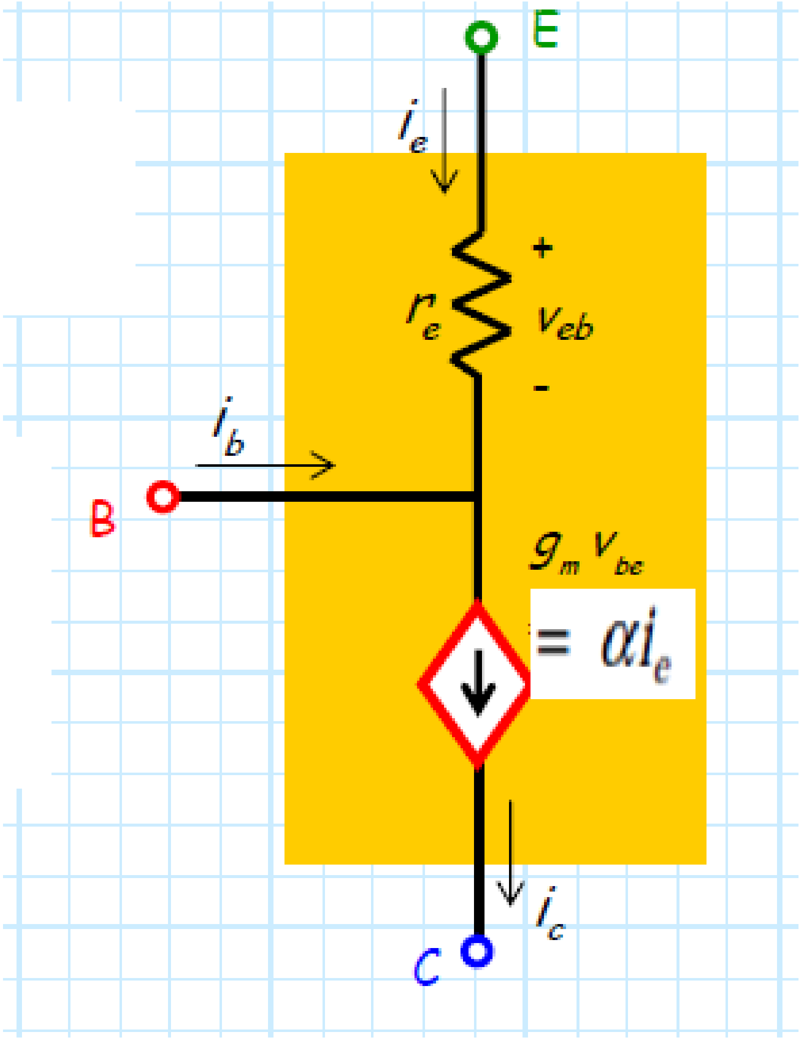
$$g_m v_{be} = g_m(i_e r_e)$$

$$= (g_m r_e) i_e = \alpha i_e$$

T Model



npn T-Model
C
i_c
$g_m v_{be}$
$= \alpha i_e$
i_b
B
+
r_e
v_{be}
-
i_e
E



E
i_e
+
r_e
v_{eb}
-
i_b
B
$g_m v_{be}$
$= \alpha i_e$
i_c
C

APPLICATION OF THE SMALL SIGNAL EQUIVALENT CIRCUIT

1. **Eliminate the signal source and determine the dc operating point of the BJT and in particular** the dc collector current *IC.*

$$\boxed{I_C, I_B, I_E \; and \; V_C}$$

2. **Calculate the values of the small-signal model parameters:**

$$\boxed{g_m = \frac{I_C}{V_T}} \qquad r_\pi = \frac{V_T}{I_B} \qquad r_\pi = \frac{\beta}{g_m} \qquad r_e = \frac{\alpha}{g_m} \simeq \frac{1}{g_m} \qquad r_e = \frac{V_T}{I_E}$$

3. **Eliminate the dc sources by replacing each dc voltage source with a short circuit and each** dc current source with an open circuit.

APPLICATION OF THE SMALL SIGNAL EQUIVALENT CIRCUIT

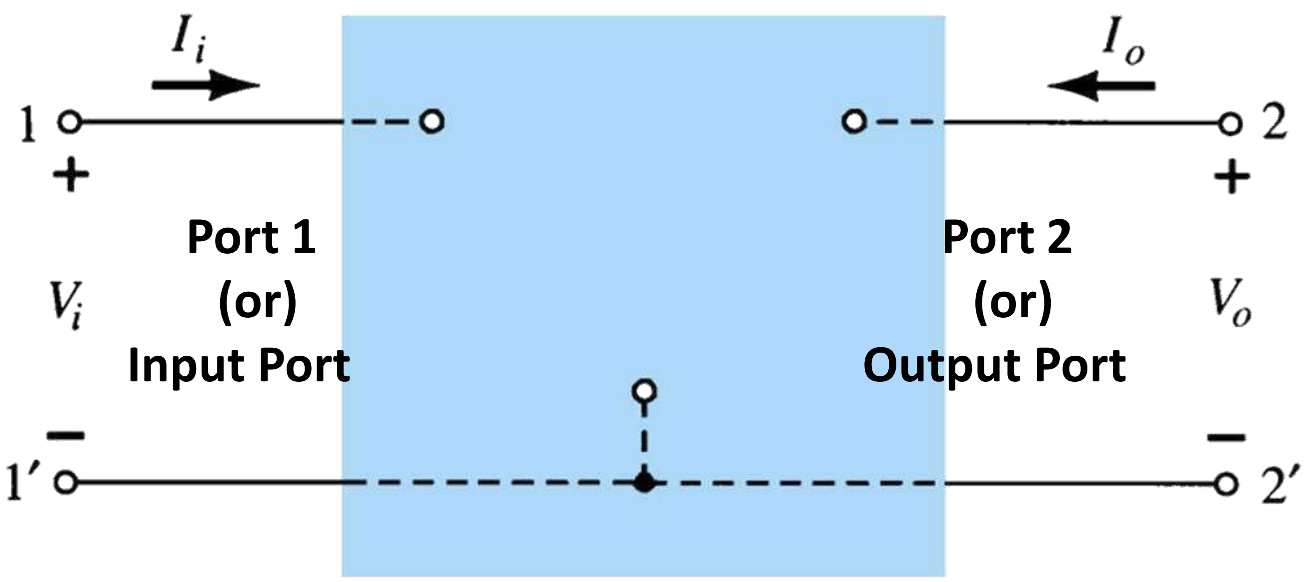
4. **Replace the BJT with one of its small-signal equivalent circuit models. Although any** one of the models can be used, one might be more convenient than the others for the particular circuit being analyzed.
   - **Hybrid-π Model**
   - **T Model**
   - **Hybrid Model**
5. **Analyze the resulting circuit to determine the required quantities (e.g., voltage gain, input and output** resistance).

$$\boxed{A_v = \frac{v_0}{v_i}} \qquad \boxed{R_o \, and \, R_i}$$

Basic BJT Amplifier Configurations

- Common-Emitter (CE) amplifier without and with emitter resistance
- Common-Base (CB) amplifier
- Common-Collector (CC) amplifier or Emitter Follower

Hybrid Equivalent Model



Two -Port Network

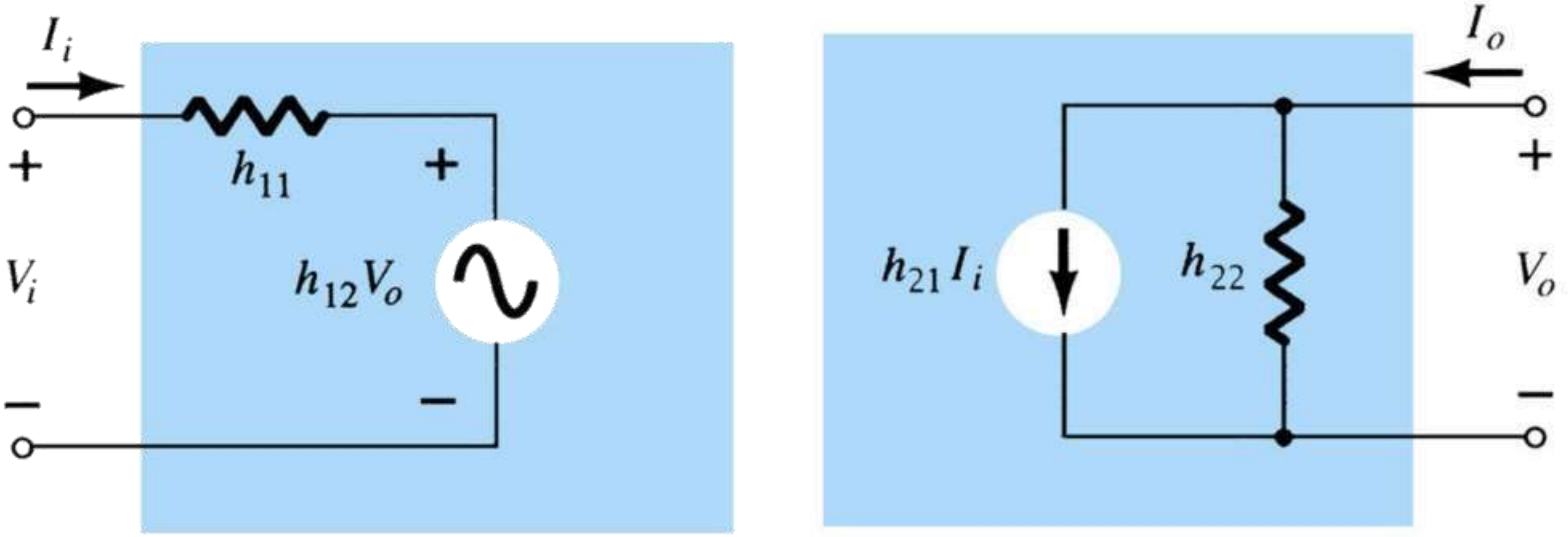
$V_i = Input \quad Voltage$

$V_o = Output \quad Voltage$

$I_i = Input \quad Current$

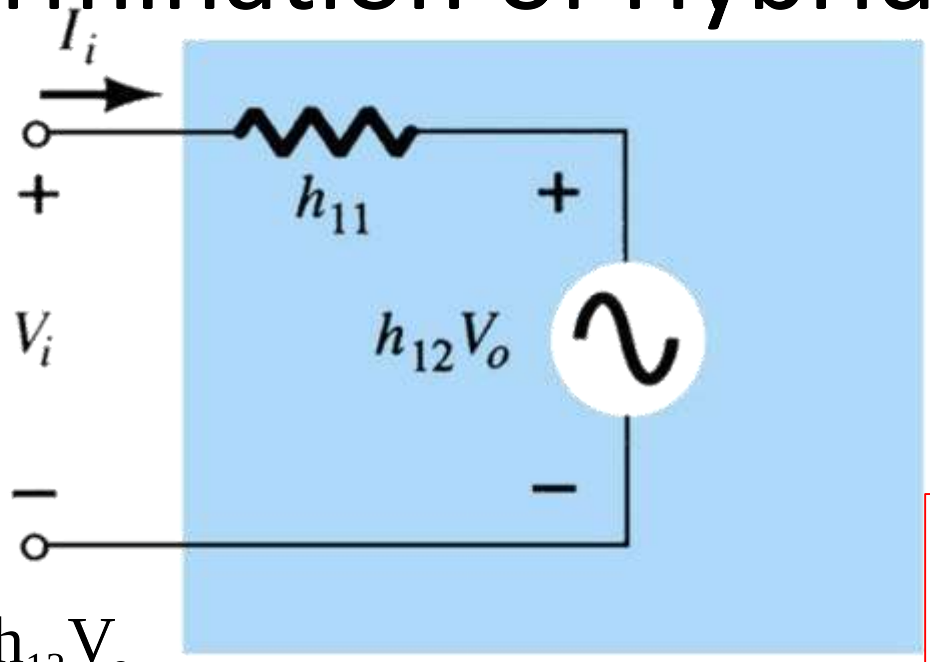
$I_o = Output \quad Current$

Determination of Hybrid Parameters



$$V_i = h_{11}I_i + h_{12}V_o \quad I_O = h_{21}I_i + h_{22}V_o$$

Determination of Hybrid Parameters



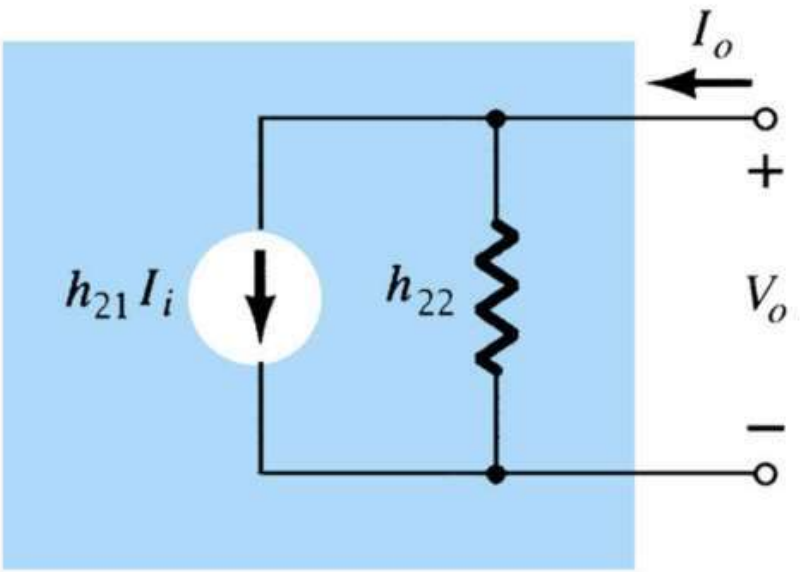
h_{11} - Ω and h_{22} – mhos
h12, h21 – Dimension Less.

$$V_i = h_{11}I_i + h_{12}V_o$$

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0V} = \textbf{Input Impedance} \text{ with output part short circuited}(\Omega)$$

$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0V} = \textbf{Reverse Voltage Transfer Ratio} \text{ with input part open circuited}$$

Determination of Hybrid Parameters



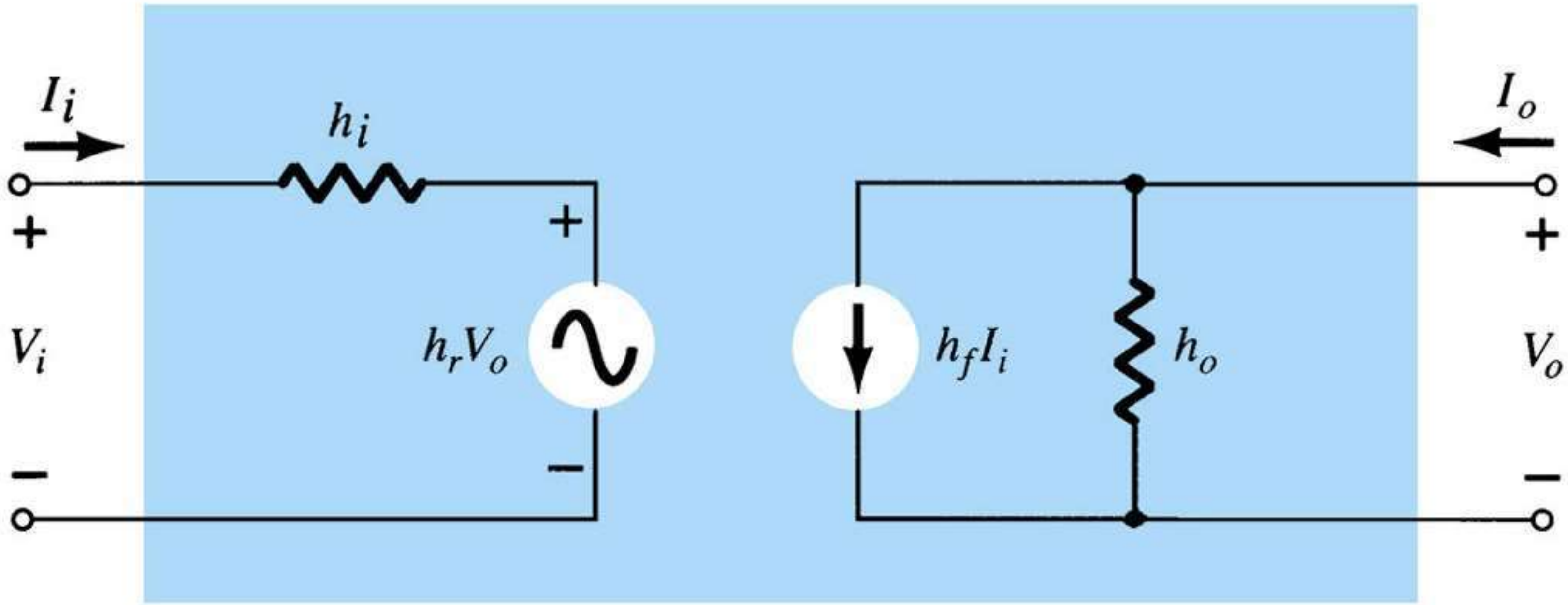
h_{11} - Ω and h_{22} – mhos
h12, h21 – Dimension Less.

$$I_O = h_{21} I_i + h_{22} V_o$$

$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o = 0V} = \textbf{Forward Current Gain} \text{ with output part short circuited}$$

$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i = 0A} = \textbf{Output Admittance} \text{ with input part open circuited(mhos)}$$

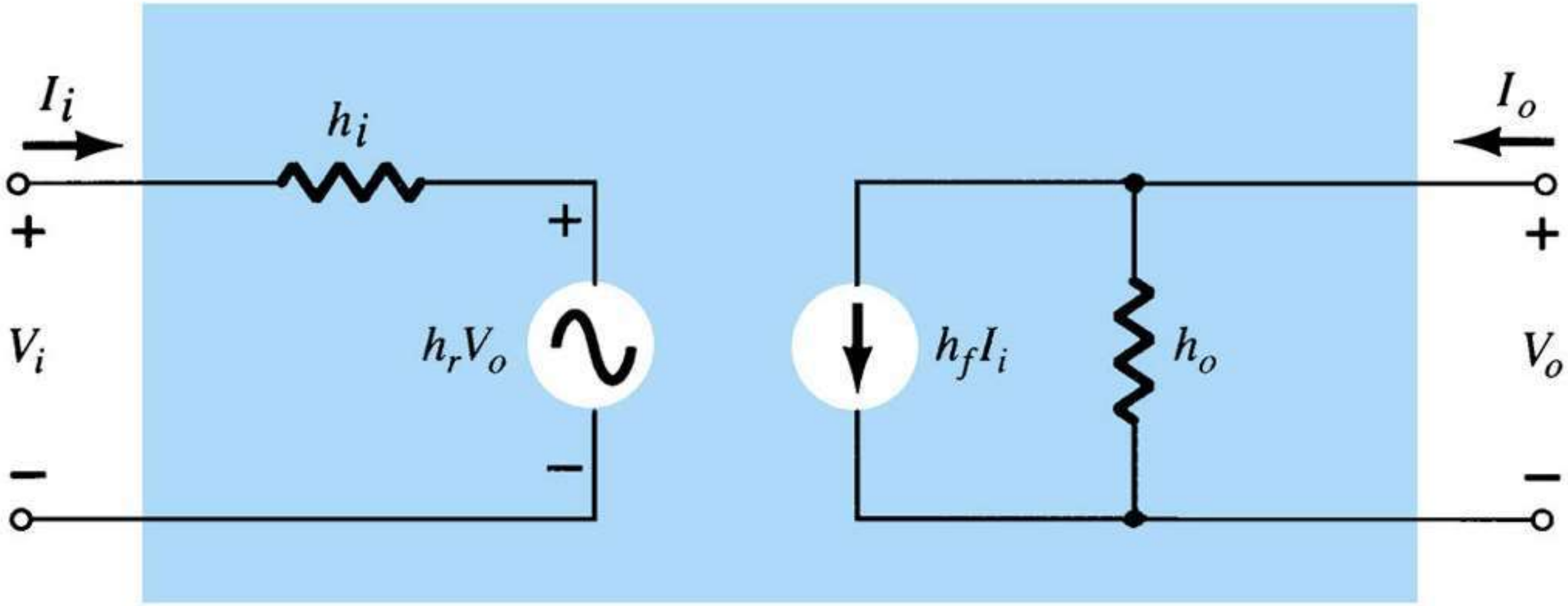
General h-Parameters for any Transistor Configuration



$$V_i = h_i\,I_i + h_r\,V_o$$
$$I_2 = h_f\,I_i + h_0\,V_o$$

hi = Input Resistance(Vi/Ii)
hr = Reverse Transfer Voltage Ratio (Vi/Vo)
hf = Forward Transfer Current Ratio (Io/Ii)
ho = Output Conductance(Io/Vo)

General h-Parameters for any Transistor Configuration

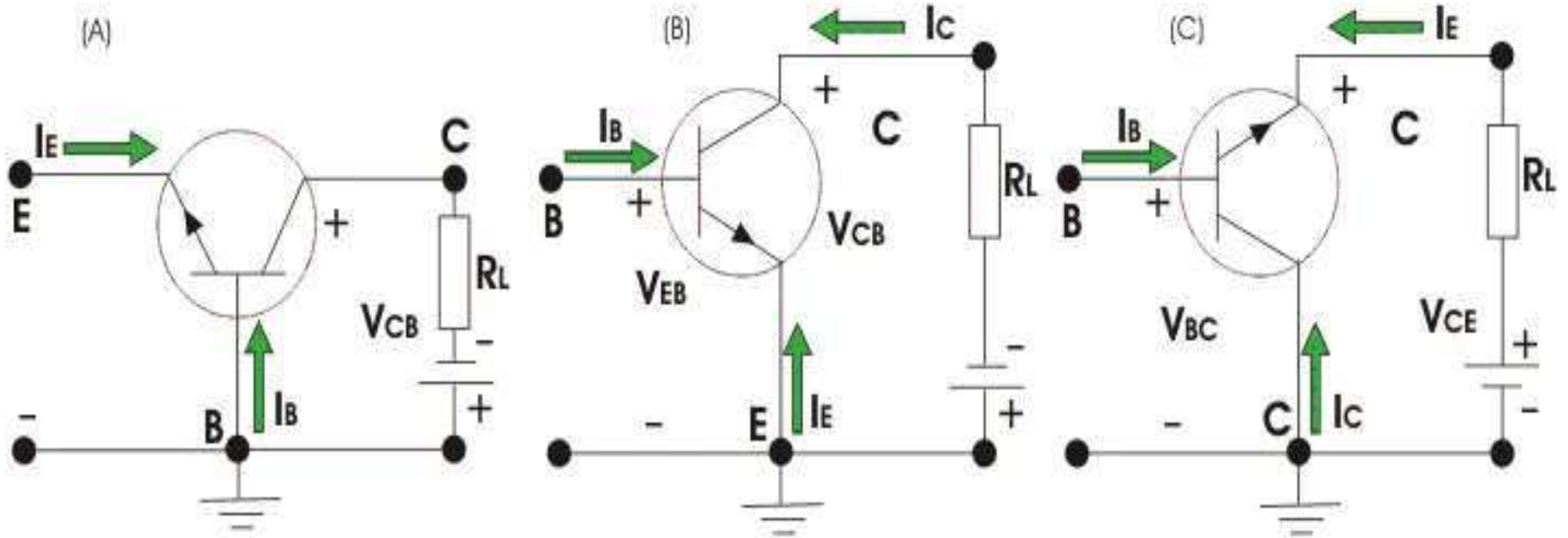


$$h_f = \left.\frac{I_o}{I_i}\right|_{V_o = 0\,V}$$

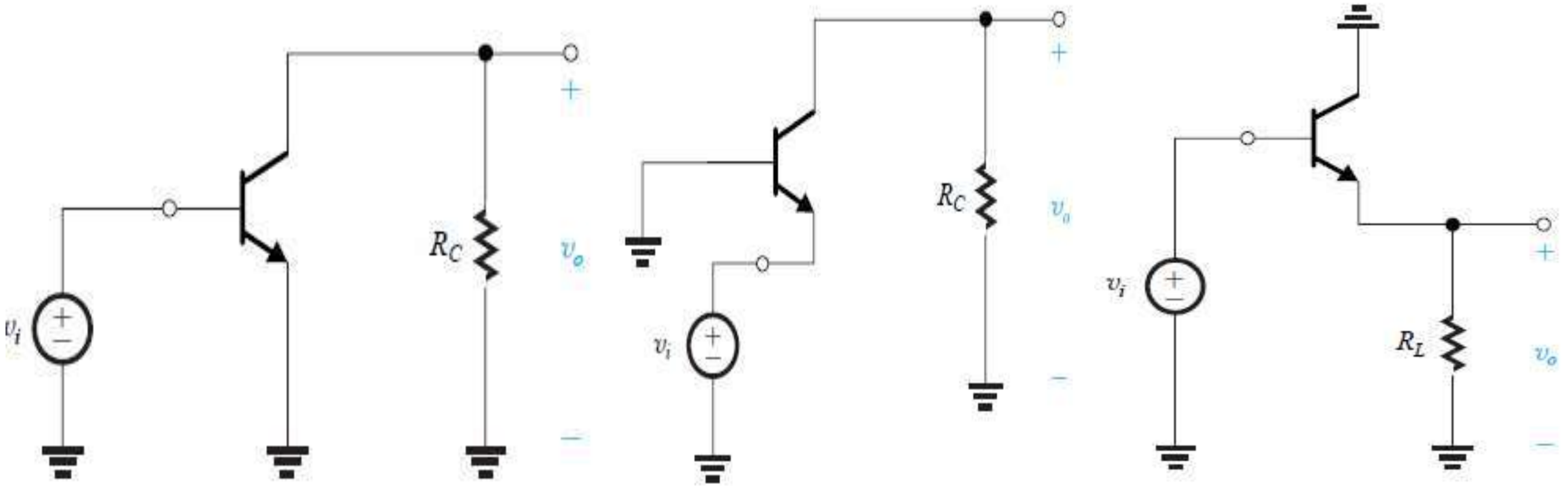
$$V_i = h_i\, I_i + h_r\, V_o$$
$$I_o = h_f\, I_i + h_0\, V_o$$

$$h_i = \left.\frac{V_i}{I_i}\right|_{V_o = 0\,V} \qquad h_r = \left.\frac{V_i}{V_o}\right|_{I_i = 0\,A} \qquad h_o = \left.\frac{I_o}{V_o}\right|_{I_i = 0\,A}$$

Three Basic Configurations of BJT Amplifier



Three Basic Configurations of BJT Amplifier

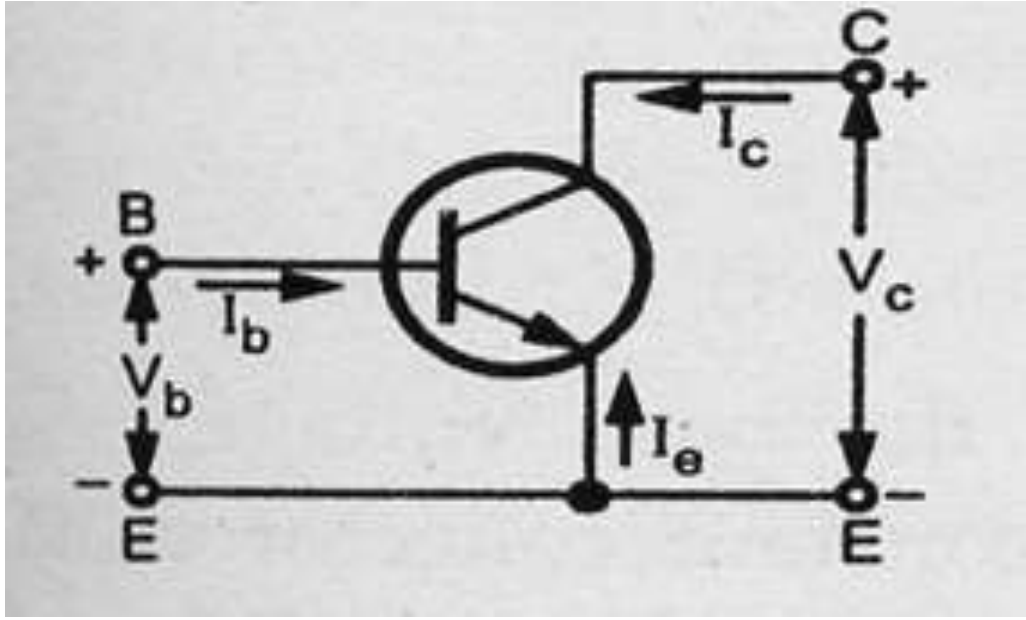


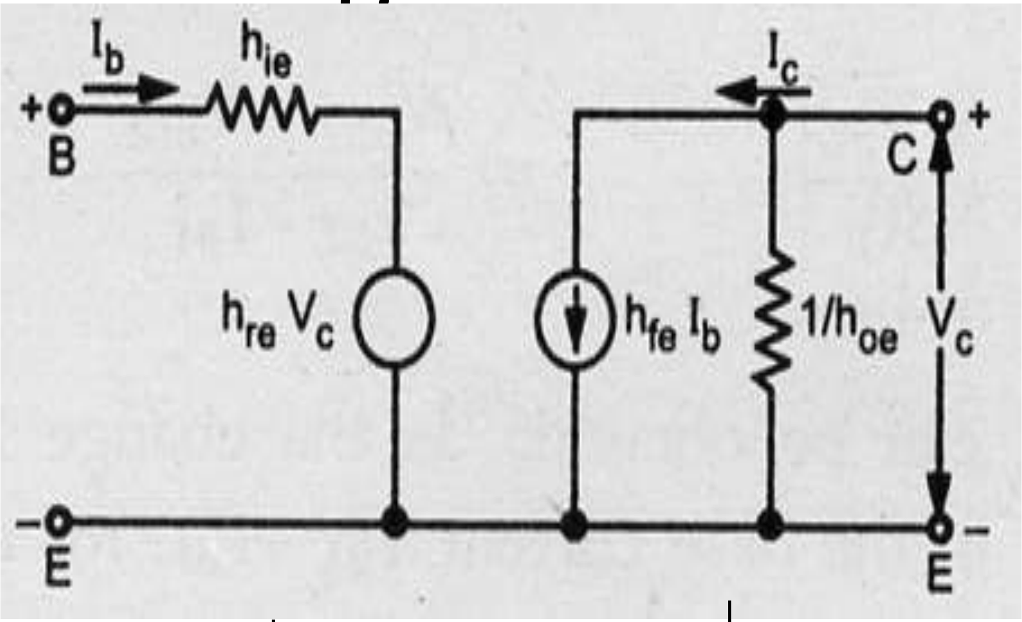
(a) Common-Emitter (CE)

(b) Common-Base (CB)

(c) Common-Collector (CC)
or Emitter Follower

Hybrid Model for BJT Configurations-CE



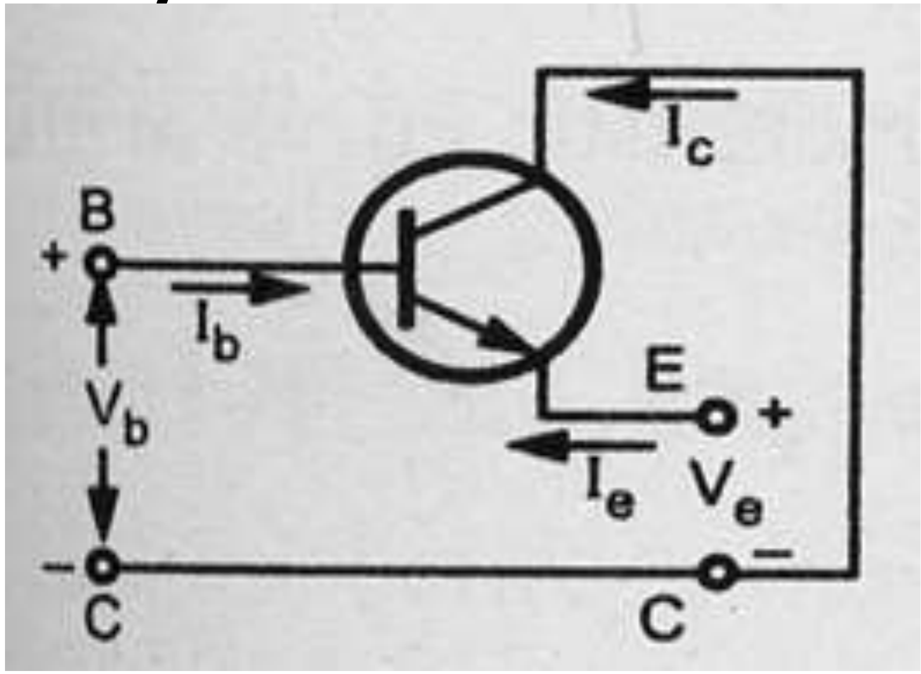


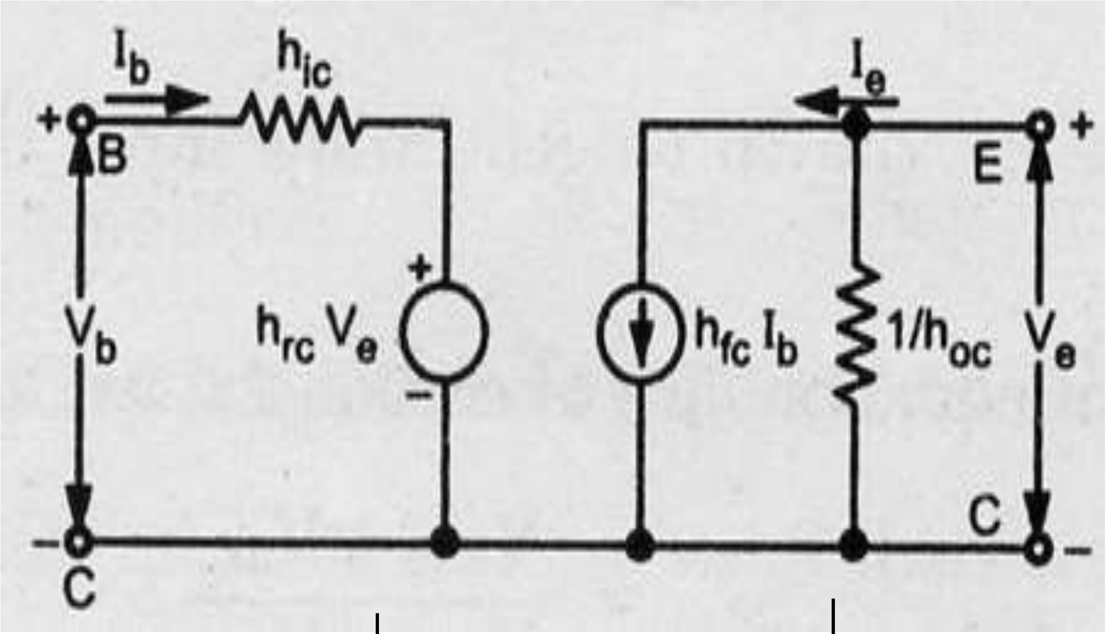
$$\boxed{\begin{aligned} v_b &= h_{ie} i_b + h_{re} v_c \\ i_c &= h_{fe} i_b + h_{oe} v_c \end{aligned}}$$

$$h_{ie} = \left.\frac{v_b}{i_b}\right|_{V_c = 0V} \qquad h_{re} = \left.\frac{v_b}{v_c}\right|_{i_b = 0\,A}$$

$$h_{fe} = \left.\frac{i_c}{i_b}\right|_{V_c = 0V} \qquad h_{oe} = \left.\frac{i_c}{v_c}\right|_{i_b = 0\,A}$$

Hybrid Model for BJT Configurations-CC



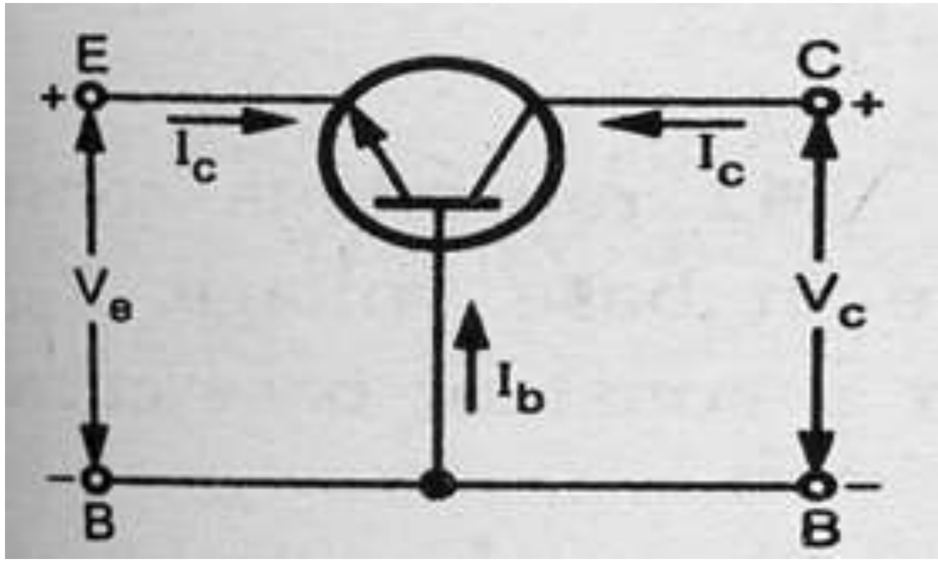


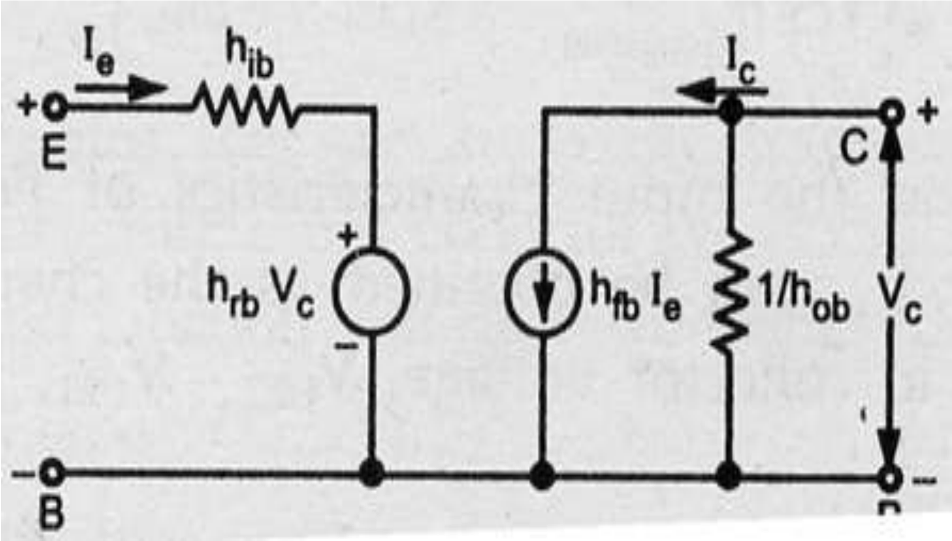
$$\boxed{\begin{aligned} v_b &= h_{ic}i_b + h_{rc}v_e \\ i_e &= h_{fc}i_b + h_{oc}v_e \end{aligned}}$$

$$h_{ic} = \left.\frac{v_b}{i_b}\right|_{V_e=0V} \qquad h_{rc} = \left.\frac{v_b}{v_e}\right|_{i_b=0\,A}$$

$$h_{fc} = \left.\frac{i_e}{i_b}\right|_{V_e=0V} \qquad h_{oe} = \left.\frac{i_e}{v_e}\right|_{i_b=0\,A}$$

Hybrid Model for BJT Configurations-CB



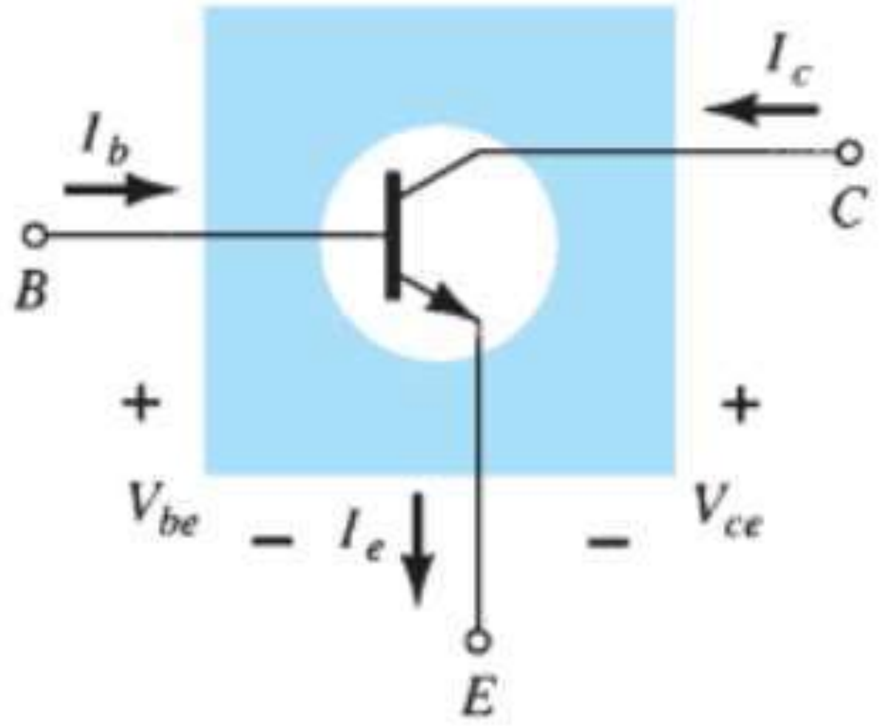


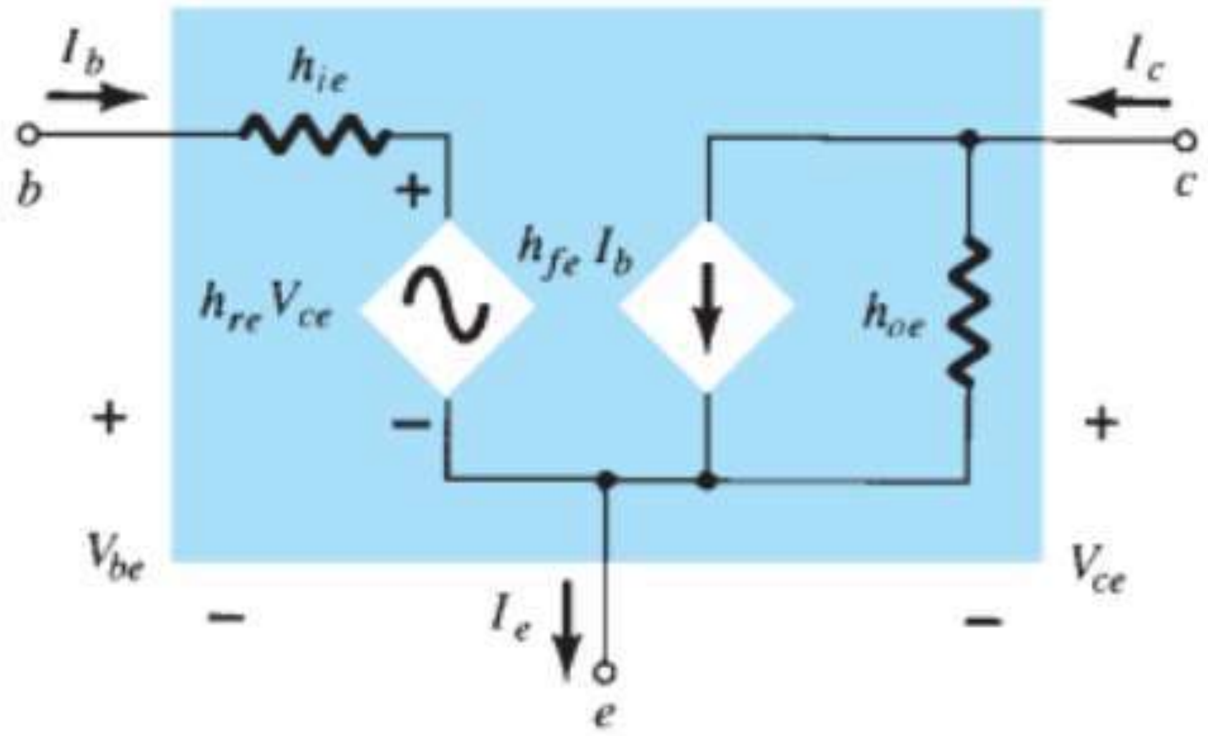
$$\boxed{\begin{aligned} v_e &= h_{ib} i_e + h_{rb} v_c \\ i_c &= h_{fb} i_e + h_{ob} v_c \end{aligned}}$$

$$h_{ib} = \left.\frac{v_e}{i_c}\right|_{V_c = 0V} \qquad h_{rb} = \left.\frac{v_e}{v_c}\right|_{i_e = 0\ A}$$

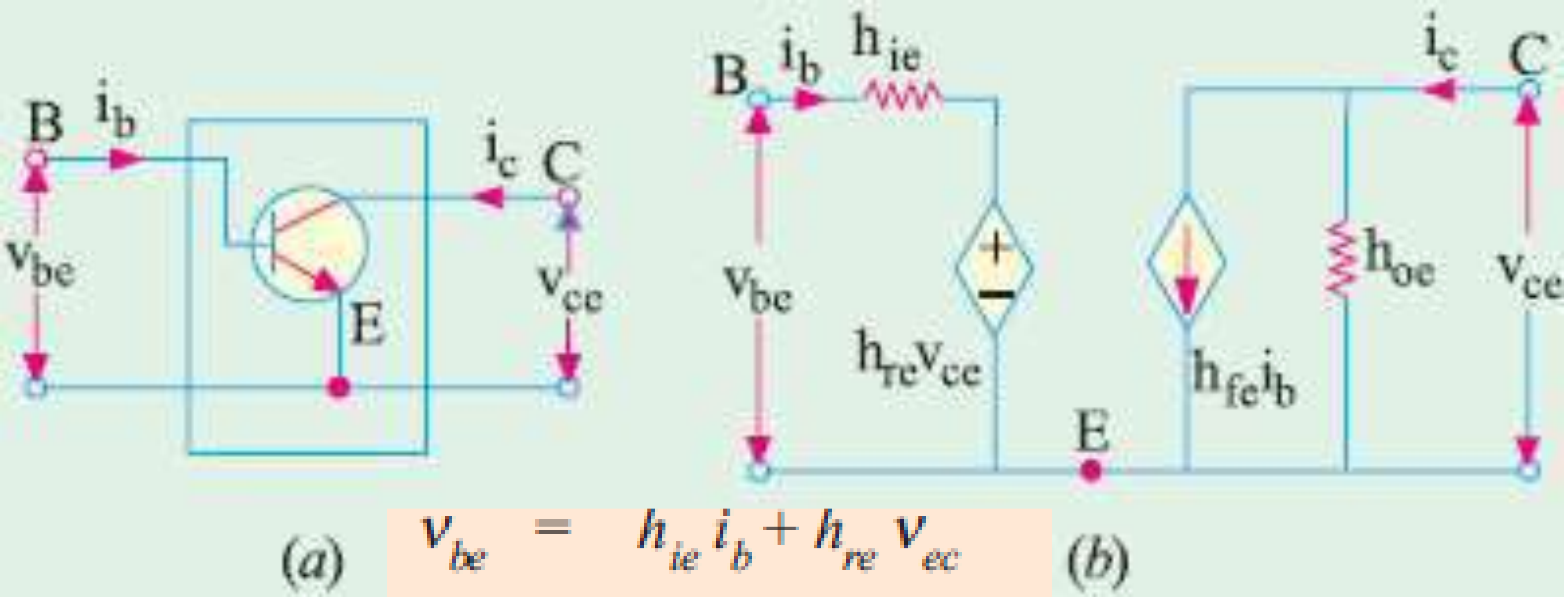
$$h_{fb} = \left.\frac{i_c}{i_e}\right|_{V_c = 0V} \qquad h_{ob} = \left.\frac{i_c}{v_c}\right|_{i_e = 0\ A}$$

Hybrid Model for BJT Configurations-CE





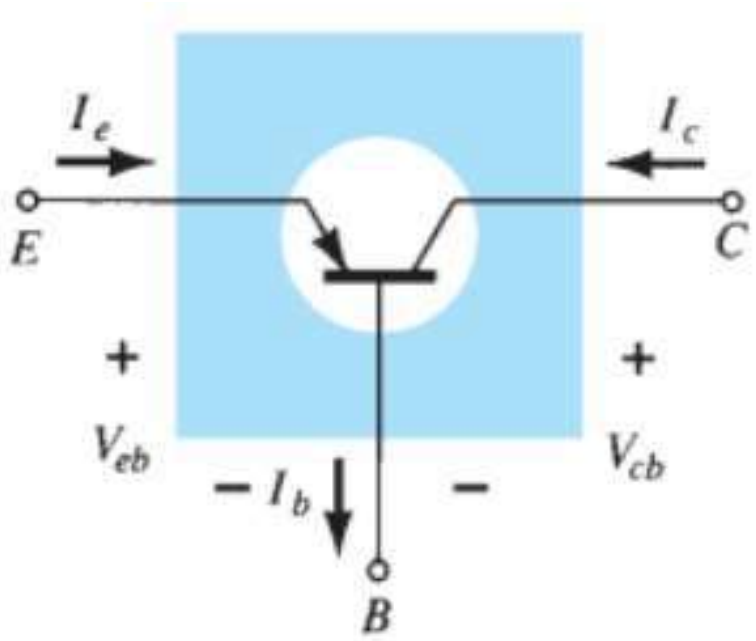
Hybrid Model for BJT Configurations-CE

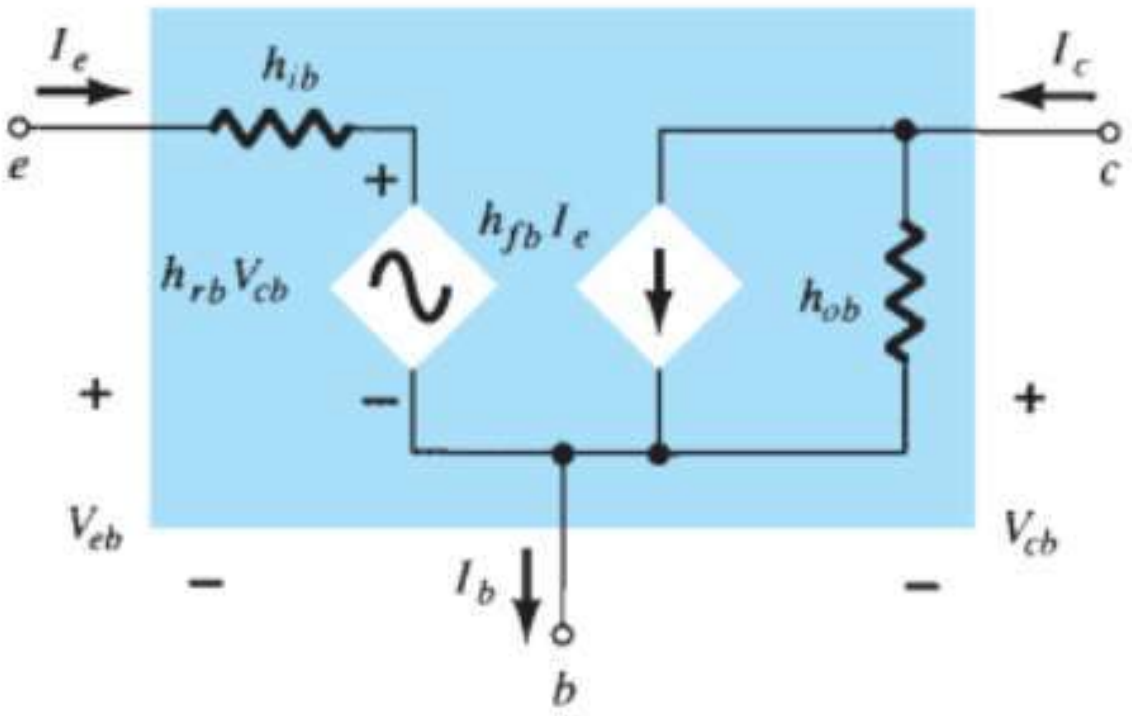


$$v_{be} = h_{ie}\, i_b + h_{re}\, v_{ec}$$

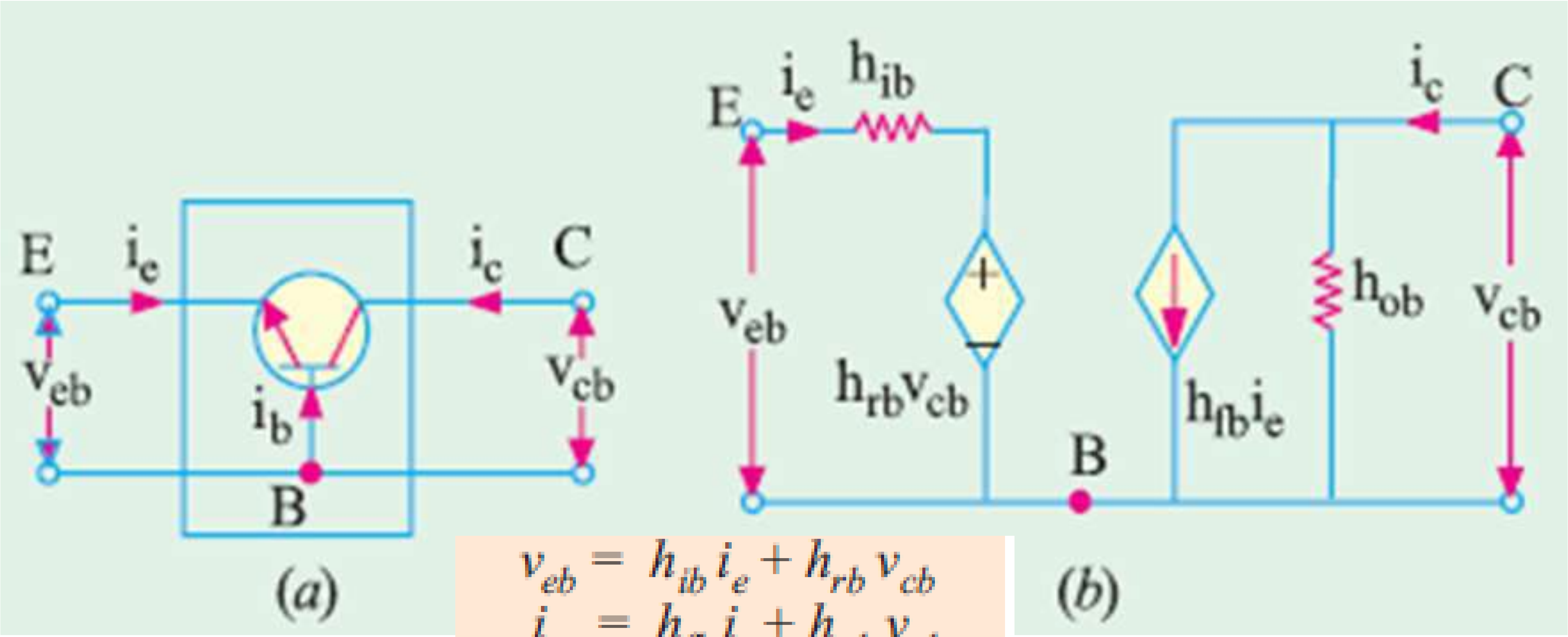
$$i_e = h_{fb}\, i_b + h_{oe}\, v_{ec}$$

Hybrid Model for BJT Configurations-CB



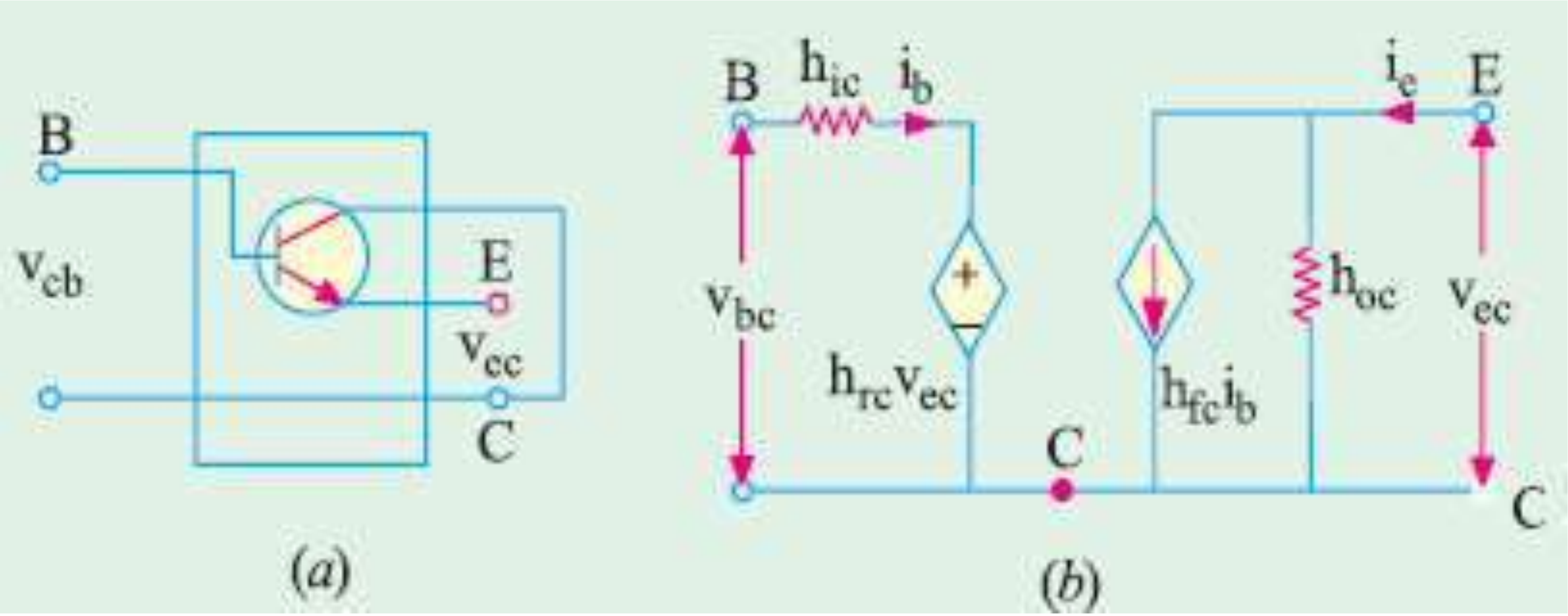


Hybrid Model for BJT Configurations-CB



$$v_{eb} = h_{ib}\, i_e + h_{rb}\, v_{cb}$$
$$i_e = h_{fb}\, i_e + h_{ob}\, v_{eb}$$

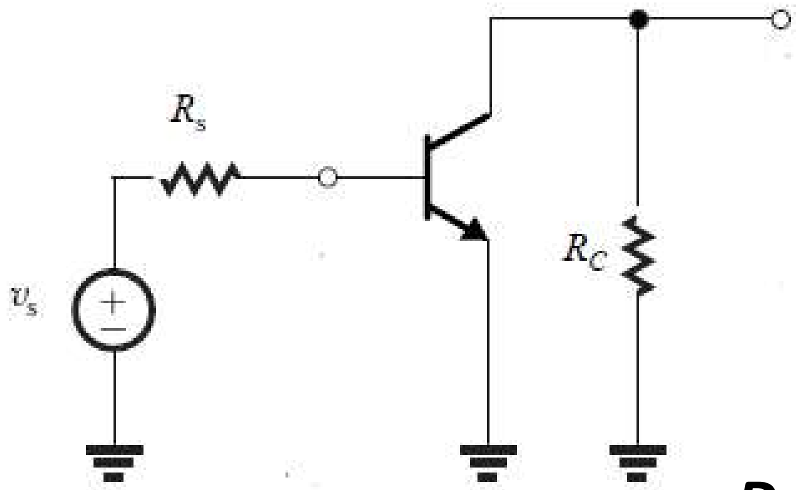
Hybrid Model for BJT Configurations-CC

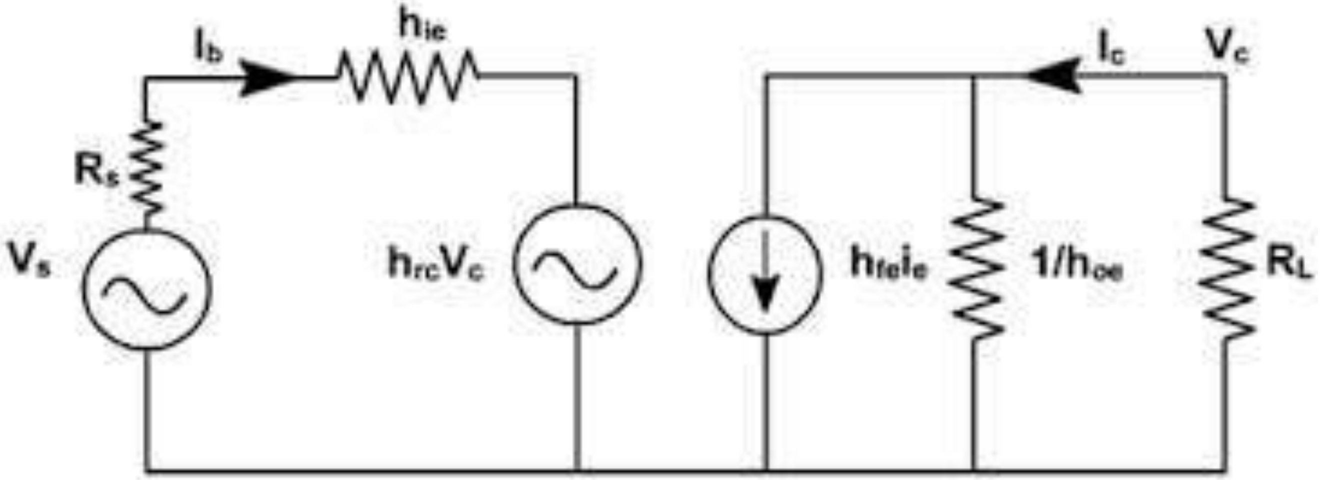


$$
\begin{aligned}
v_{be} &= h_{ie}\, i_b + h_{re}\, v_{ec} \\
i_e &= h_{fe}\, i_b + h_{oc}\, v_{ce}
\end{aligned}
$$

CE Amplifier Without Emitter Resistance

(Using Hybrid Model)





Determine :

1.Current Gain or Current Amplification A_i

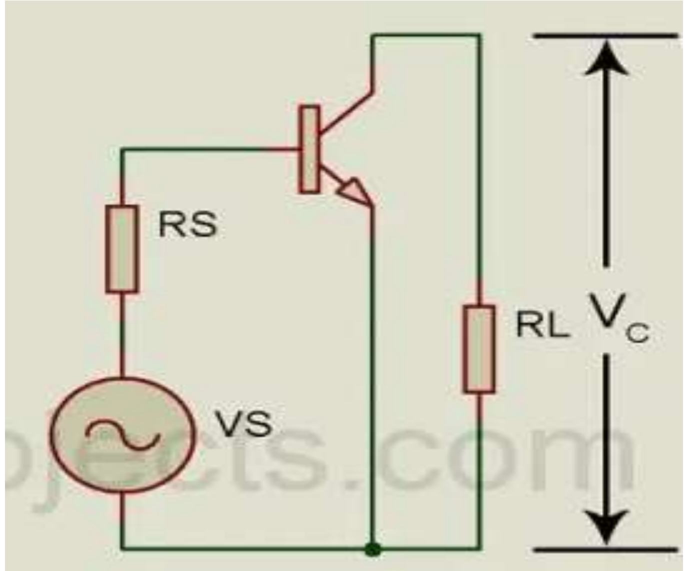
2. Input Resistance R_i

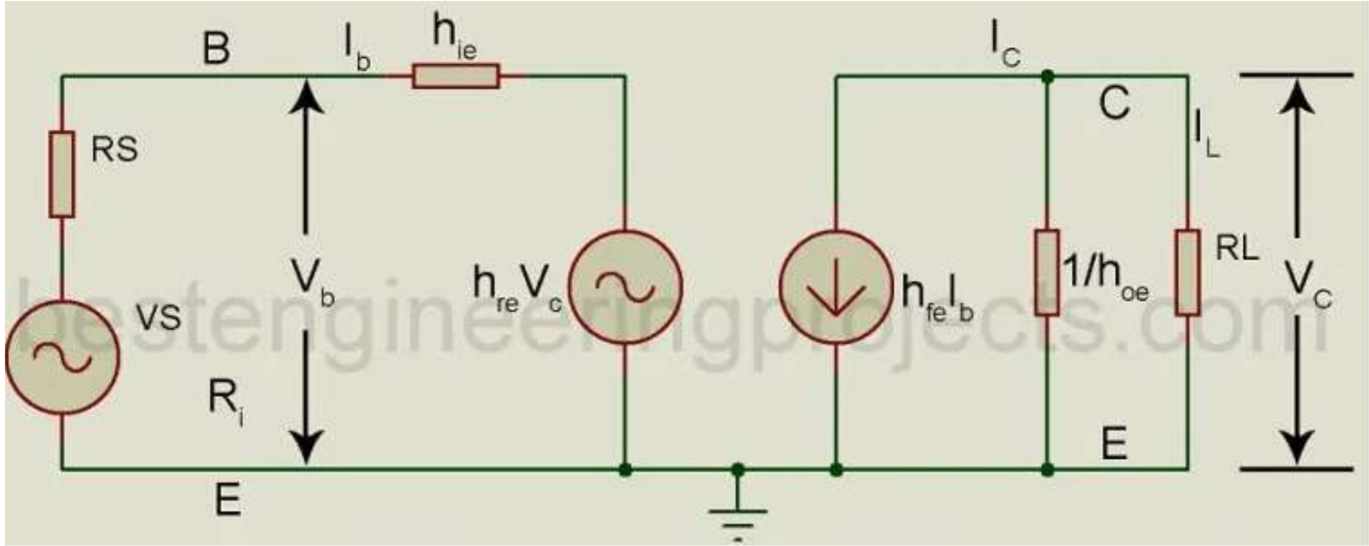
3. ***Voltage Gain or Voltage Amplification A_v***

4. ***Output Admittance Y_0***

5. ***Output Resistance R_o***

CE Amplifier Without Emitter Resistance
(Using Hybrid Model)





Determine :

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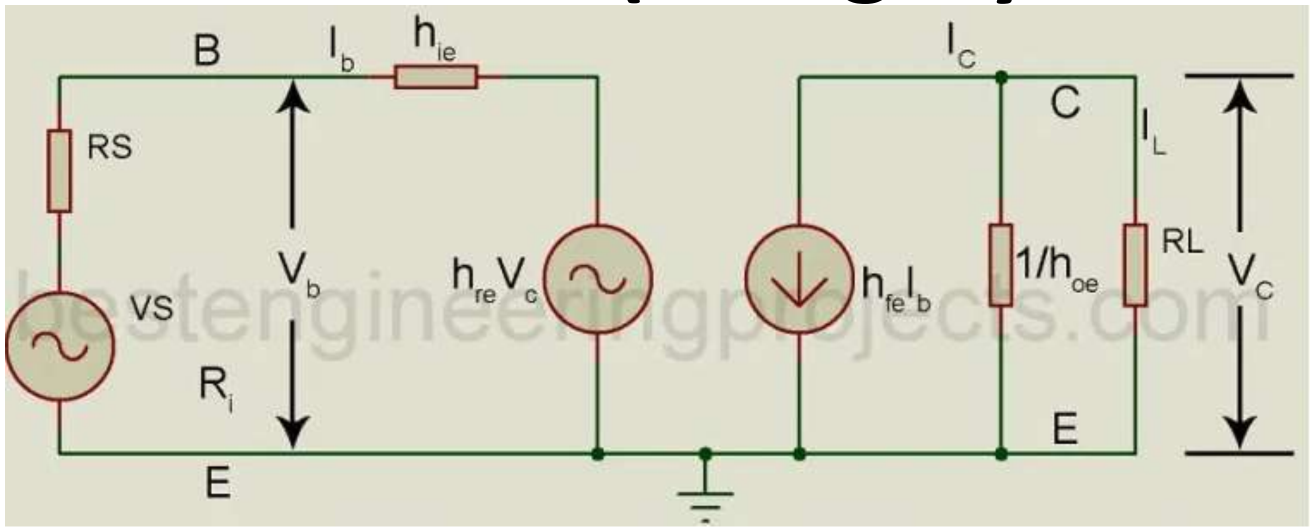
3. ***Voltage Gain or Voltage Amplification A_v***

4. ***Output Admittance Y_0***

5. ***Output Resistance R_o***

CE Amplifier Without Emitter Resistance
(Using Hybrid Model)



$$A_i = \frac{i_L}{i_b} = -\frac{i_c}{i_b}$$

$$i_c = h_{fe} i_b + h_{oe} v_c$$

$$v_c = i_L R_L = -i_c R_L$$

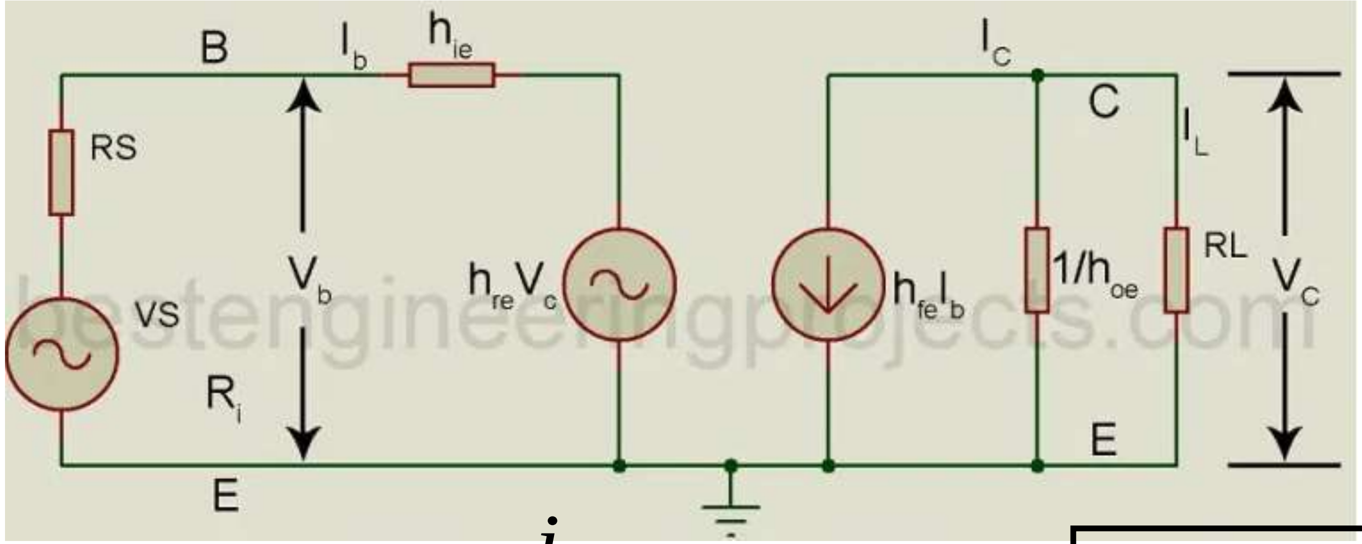
$$i_c = h_{fe} i_b + h_{oe}\left(-i_c R_L\right)$$

$$i_c\left(1 + h_{oe} R_L\right) = h_{fe} i_b$$

$$\boxed{A_i = \frac{i_c}{i_b} = -\frac{h_{fe}}{1 + h_{oe} R_L}}$$

- ***Current Gain or Current Amplification:***
- Current gain is defined as the ratio of the load current I_L to the input current I_b.

CE Amplifier Without Emitter Resistance
(Using Hybrid Model)



Input Resistance R_i

$$\boxed{R_i = \frac{v_b}{i_b}}$$

$$\boxed{v_b = h_{ie} i_b + h_{re} v_c}$$

$$\boxed{v_c = i_L R_L = -i_c R_L = A_i i_b R_L}$$

But, $A_i = -\frac{i_c}{i_b} \Rightarrow i_c = -A_i i_b$

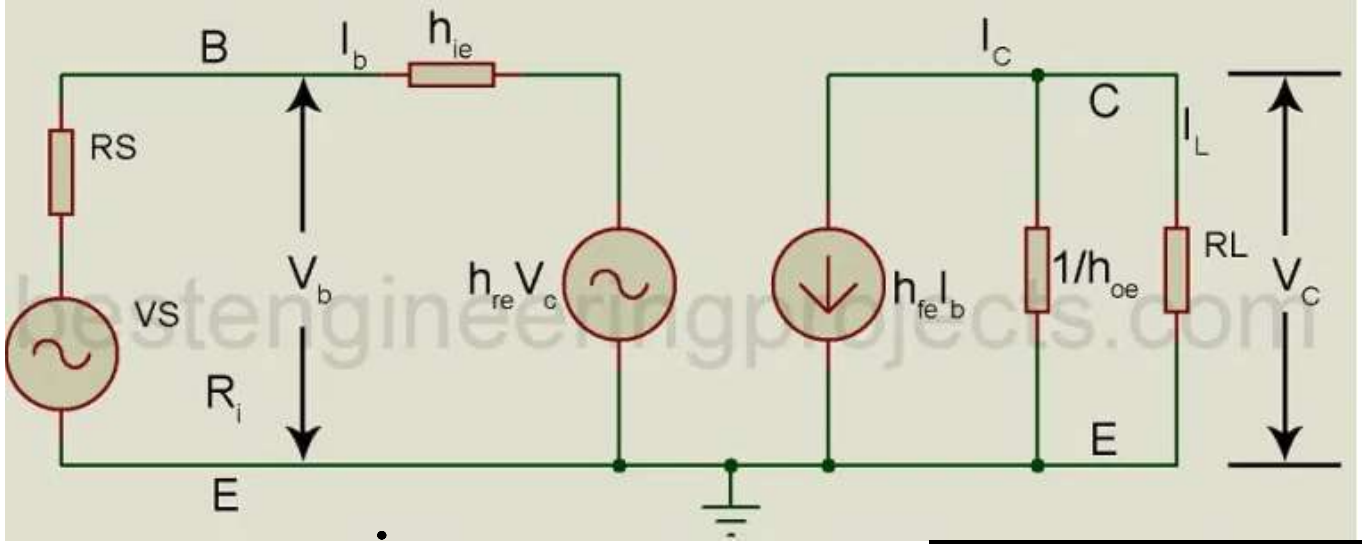
$$\boxed{v_b = h_{ie} i_b + h_{re} (A_i i_b R_L)}$$

$$\boxed{v_b = i_b (h_{ie} + h_{re} A_i R_L)}$$

$$\boxed{\Rightarrow R_i = \frac{v_b}{i_b} = h_{ie} + h_{re} A_i R_L}$$

CE Amplifier Without Emitter Resistance

(Using Hybrid Model)



Voltage Gain A_v

$$\boxed{A_v = \frac{v_c}{v_b}}$$

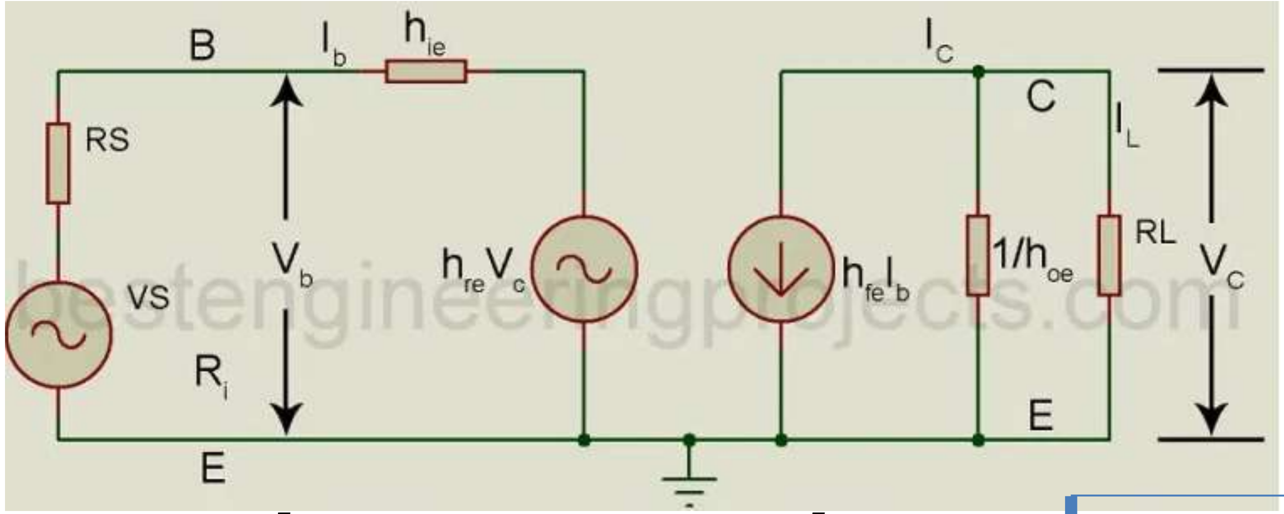
But, $A_i = -\dfrac{i_c}{i_b} \Rightarrow i_c = -A_i\, i_b$

$$\boxed{v_c = i_L R_L = -i_c R_L = A_i i_b R_L}$$

$$\boxed{\frac{1}{R_i} = \frac{i_b}{v_b}}$$

$$\boxed{\Rightarrow A_v = \frac{v_c}{v_b} = \frac{A_i i_b R_L}{v_b} = \frac{A_i R_L}{R_i}}$$

CE Amplifier Without Emitter Resistance
(Using Hybrid Model)



Output Admittance Y_o

$$\boxed{Y_o = \frac{i_c}{v_c}}$$

$$i_c = h_{fe} i_b + h_{oe} v_c$$

Dividing By V_c

$$\frac{i_c}{v_c} = \frac{h_{fe} i_b}{v_c} + \frac{h_{oe} v_c}{v_c} \Rightarrow \frac{i_c}{v_c} = \frac{h_{fe} i_b}{v_c} + h_{oe}$$

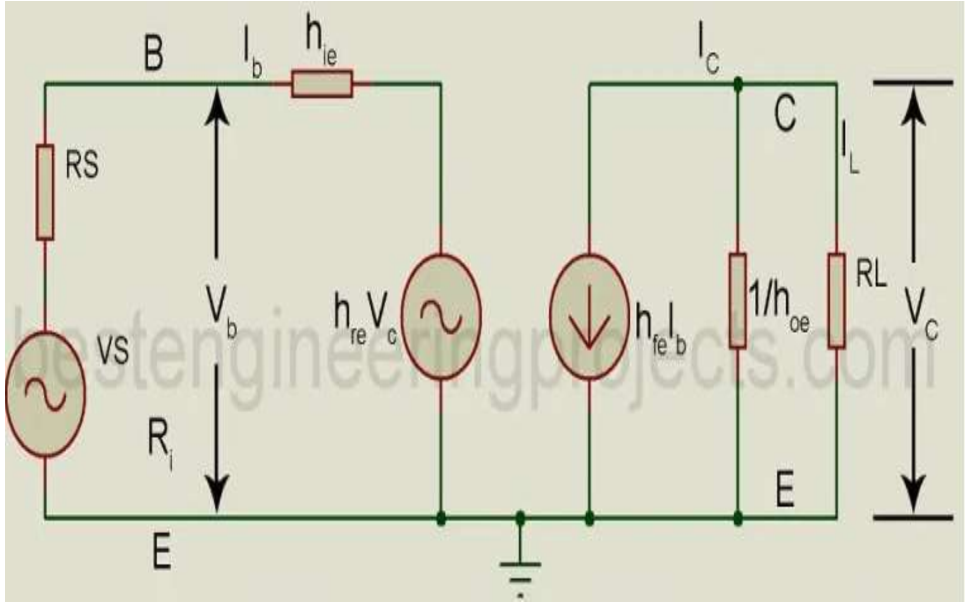
$$v_s = 0, R_s i_b + h_{ie} i_b + h_{re} v_c = 0$$

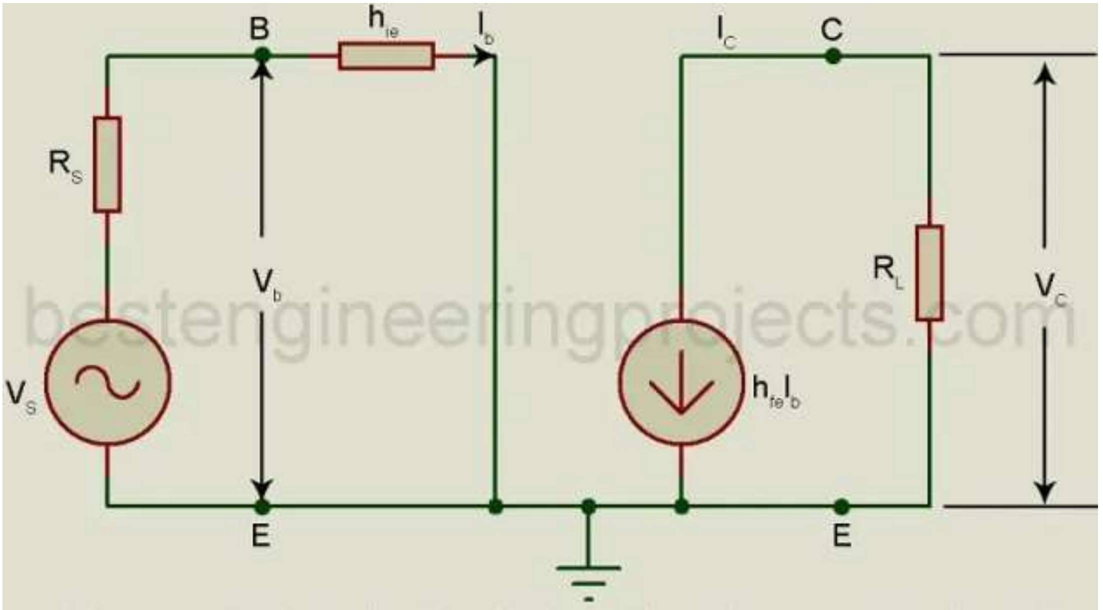
$$(R_s + h_{ie}) i_b = -h_{re} v_c$$

$$\boxed{\Rightarrow \frac{i_b}{v_c} = -\frac{h_{re}}{R_s + h_{ie}}}$$

$$\boxed{\Rightarrow Y_0 = h_{oe} - \frac{h_{fe} h_{re}}{R_s + h_{ie}} \text{ and } R_0 = \frac{1}{Y_0}}$$

CE Amplifier Without Emitter Resistance
(Using Approximate Hybrid Model)





$$A_i = \frac{i_c}{i_b} = -\frac{h_{fe}}{1+h_{oe}R_L}$$

$$R_i = \frac{v_b}{i_b} = h_{ie} + h_{re}A_iR_L$$

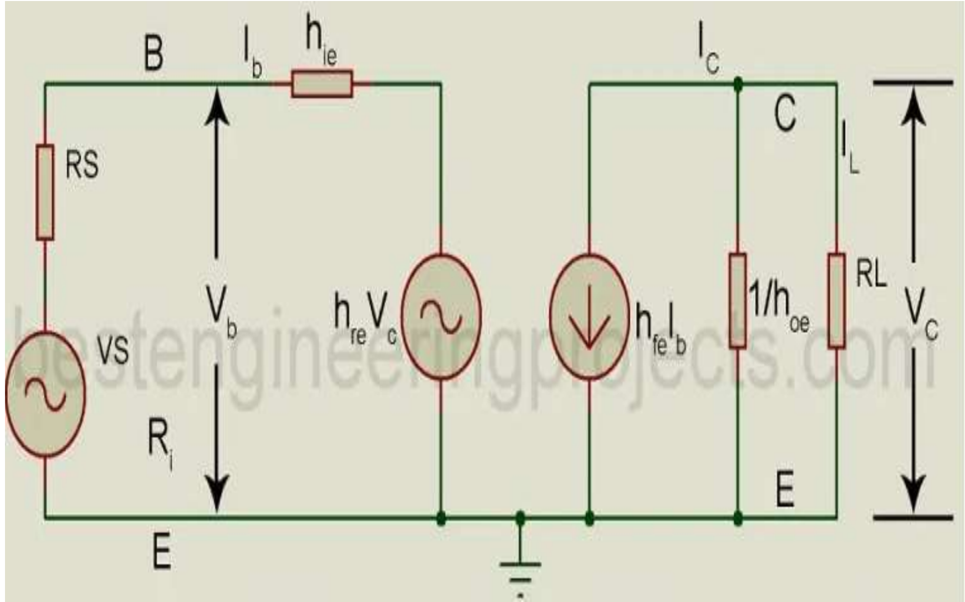
Neglecting

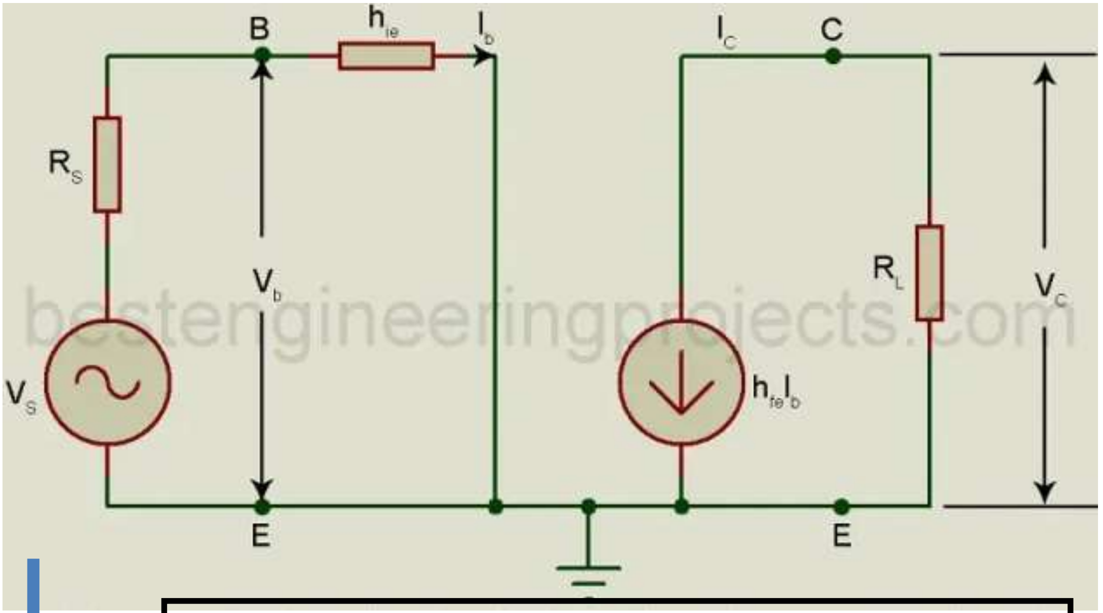
$$h_{oe} = 0, and\ h_{re} = 0$$

$$A_i = \frac{i_c}{i_b} = -h_{fe}$$

$$\Rightarrow R_i = h_{ie}$$

CE Amplifier Without Emitter Resistance
(Using Approximate Hybrid Model)



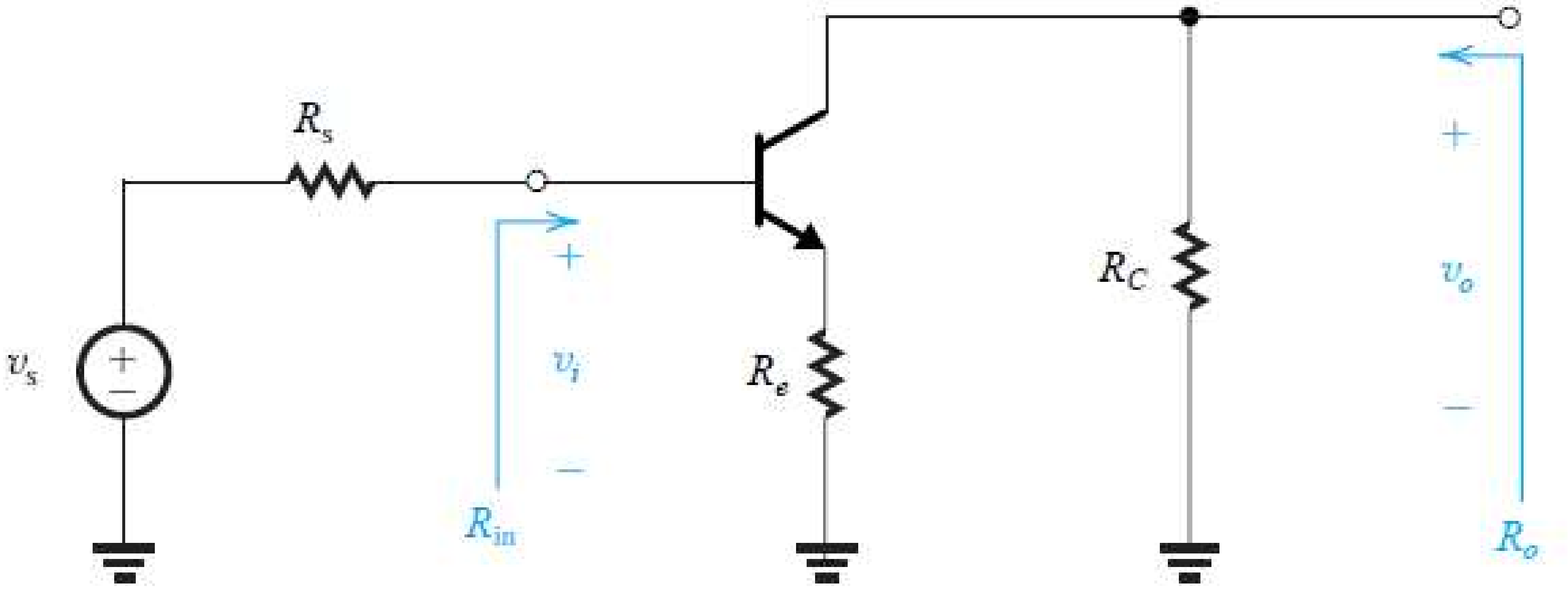


$$\Rightarrow A_v = \frac{A_i R_L}{R_i} = \frac{A_i R_L}{h_{ie}}$$

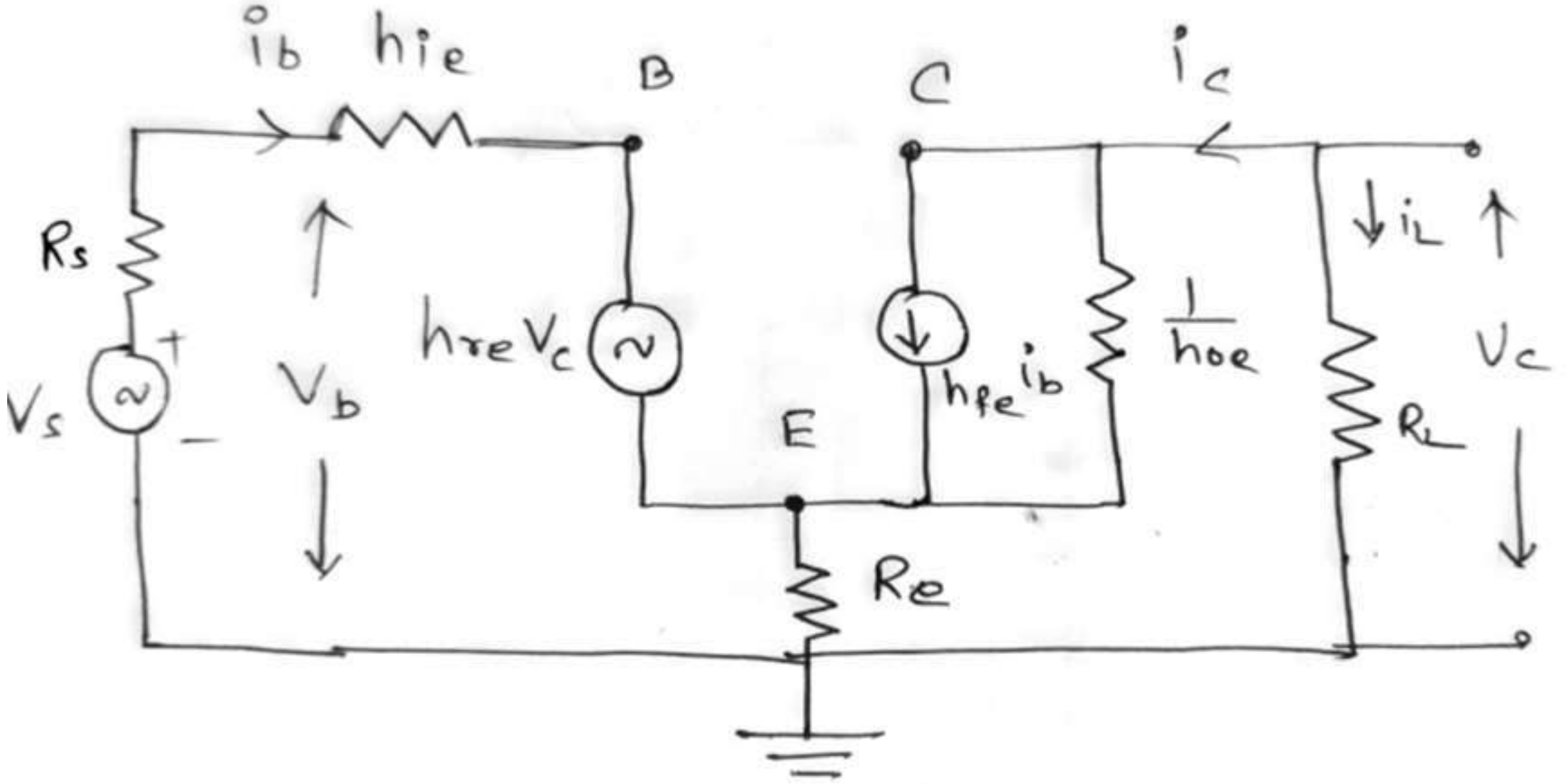
$$\Rightarrow Y_0 = h_{oe} - \frac{h_{fe} h_{re}}{R_s + h_{ie}} \text{ and } R_0 = \frac{1}{Y_0}$$

$$\Rightarrow Y_0 = 0 \text{ and } R_0 = \frac{1}{Y_0} = \infty$$

CE Amplifier With Emitter Resistance



CE Amplifier With Emitter Resistance
(Using Hybrid Model)



CE Amplifier With Emitter Resistance

(Using Hybrid Model)

$$A_i = -\frac{h_{fe}}{1+h_{oe}R_L}$$

$$R_i = \frac{v_b}{i_b} = h_{ie} + h_{re}A_i R_L$$

$$A_v = \frac{A_i R_L}{R_i}$$

$$Y_0 = h_{oe} - \frac{h_{fe}h_{re}}{R_s + h_{ie}} \text{ and } R_0 = \frac{1}{Y_0}$$

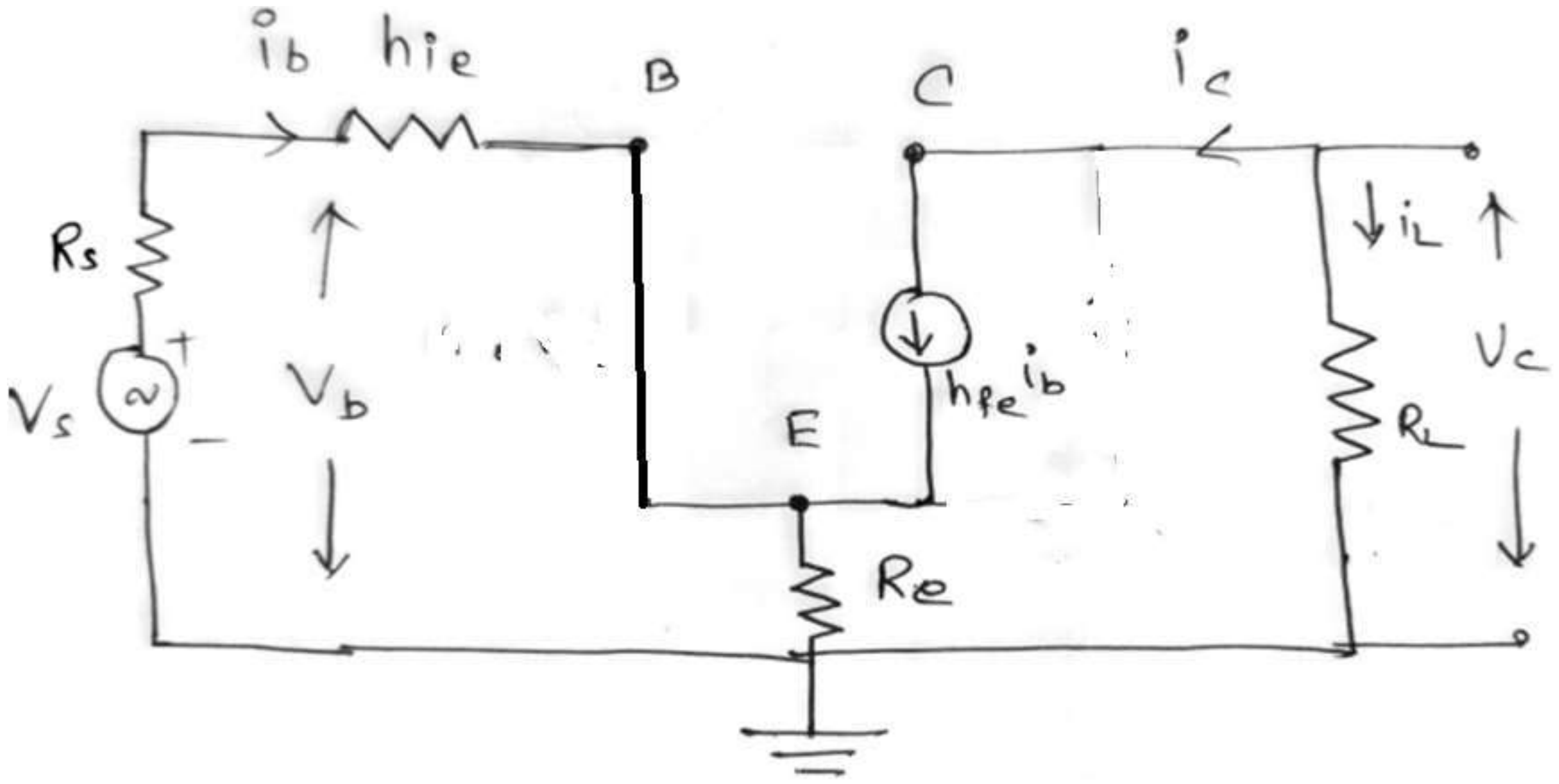
$$A_i = \frac{h_{oe}R_e - h_{fe}}{1+h_{oe}(R_L+R_e)}$$

$$R_i = h_{ie} + h_{re}A_i(R_L+R_e) + R_e(1-A_i) - R_e h_{re}$$

$$A_v = \frac{A_i R_L}{R_i}$$

$$R_0 = \frac{1+h_{fe}}{h_{oe}} + \frac{(R_s+h_{ie})(1+h_{oe}R_e)}{h_{oe}R_e} \text{ and } Y_0 = \frac{1}{R_0}$$

CE Amplifier With Emitter Resistance
(Using Approximate Hybrid Model)



CE Amplifier With Emitter Resistance
(Using Approximate Hybrid Model)

$$A_i = \frac{h_{oe}R_e - h_{fe}}{1 + h_{oe}(R_L + R_e)}$$

$$R_i = h_{ie} + h_{re}A_i(R_L + R_e) + R_e(1 - A_i) - R_e h_{re}$$

$$A_v = \frac{A_i R_L}{R_i}$$

$$R_0 = \frac{1 + h_{fe}}{h_{oe}} + \frac{(R_s + h_{ie})(1 + h_{oe}R_e)}{h_{oe}R_e} \; and \; Y_0 = \frac{1}{R_0}$$

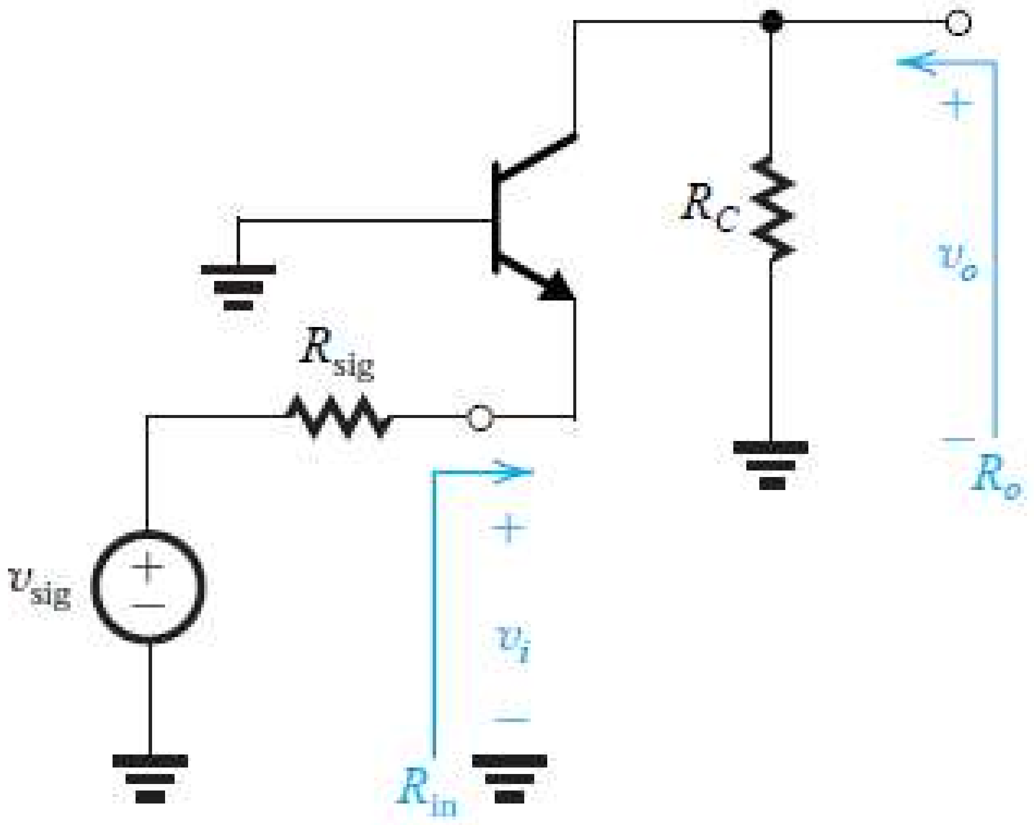
$$A_i = -h_{fe}$$

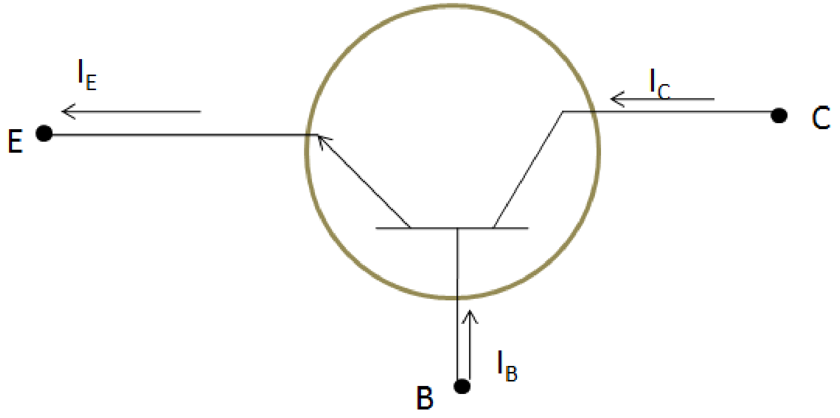
$$R_i = h_{ie} + (1 + h_{fe})R_e$$

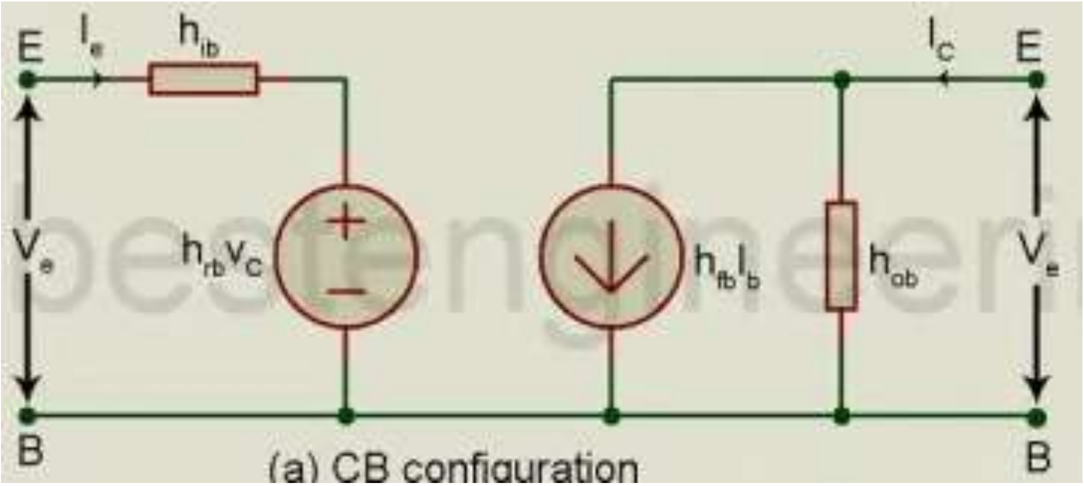
$$A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe}R_L}{h_{ie} + (1 + h_{fe})R_e}$$

$$Y_0 = 0, and \; R_0 = \infty$$

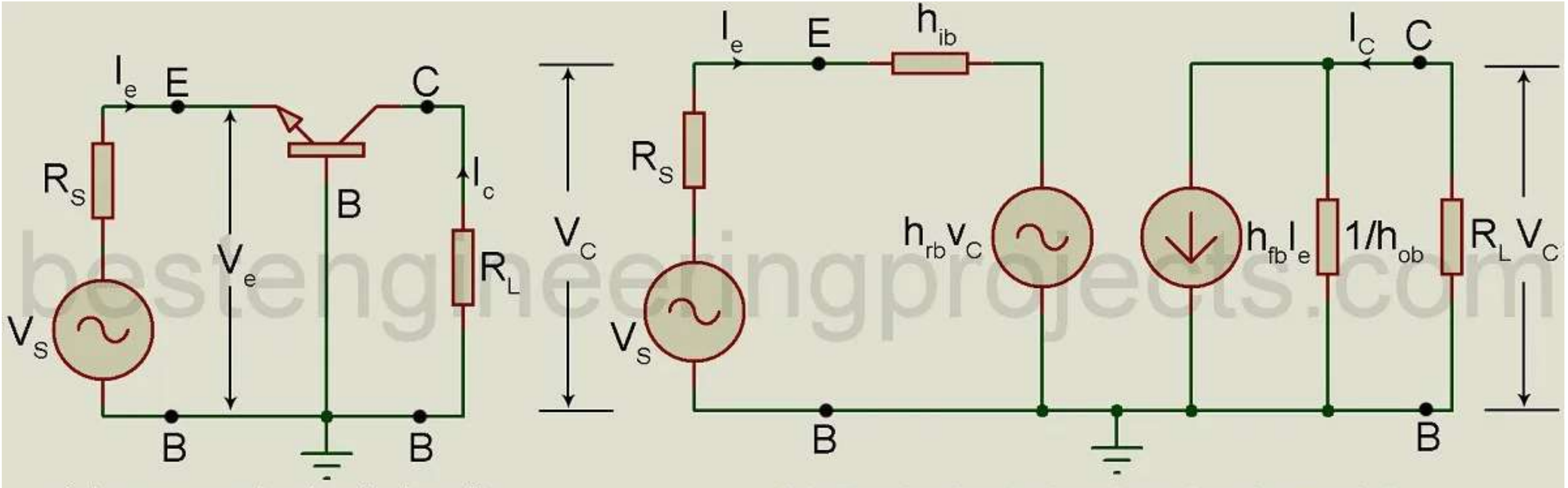
CB Amplifier(**Using Hybrid Model)**





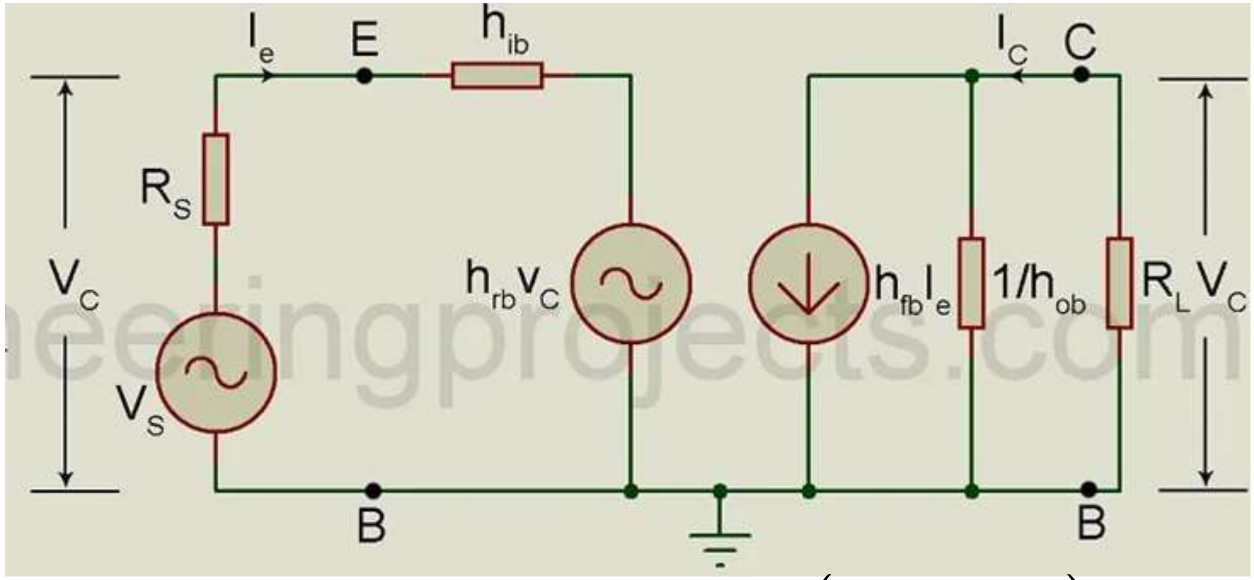


CB Amplifier(**Using Hybrid Model)**



(a) a.c. equivalent circuit (b) Equivalent circuit using h-model

CB Amplifier **(Using Hybrid Model)**



$$A_i = \frac{i_L}{i_e} = -\frac{i_c}{i_e}$$

$$i_c = h_{fb} i_e + h_{ob} v_c$$

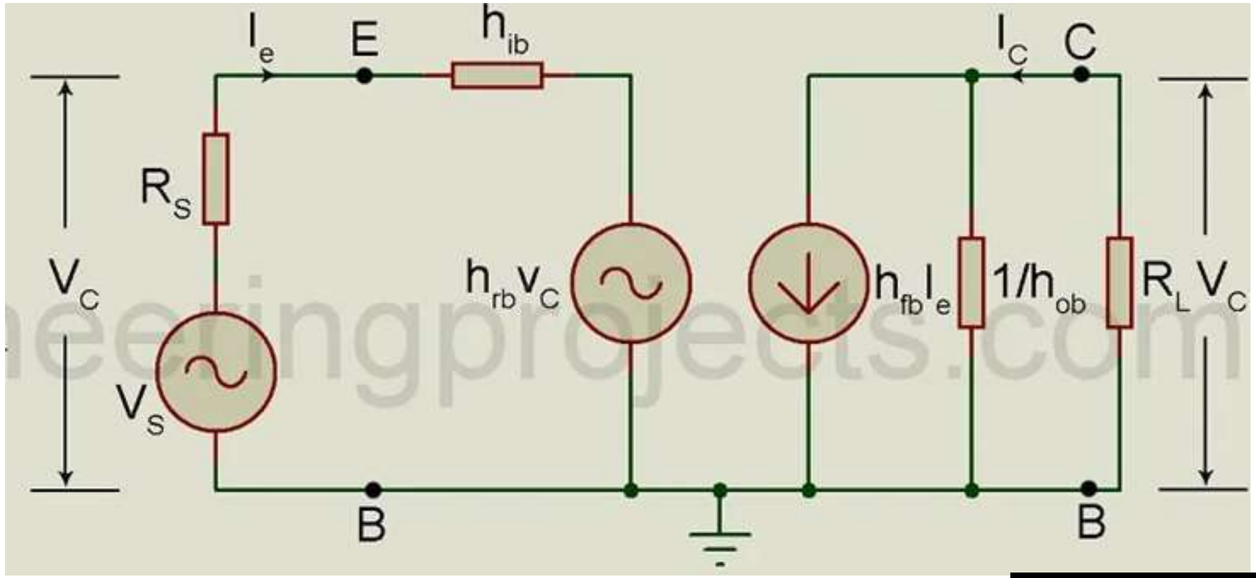
$$v_c = i_L R_L = -i_c R_L$$

$$i_c = h_{fb} i_e + h_{ob}\left(-i_c R_L\right)$$

$$i_c\left(1 + h_{ob} R_L\right) = h_{fb} i_e$$

$$\boxed{A_i = \frac{i_c}{i_e} = -\frac{h_{fb}}{1 + h_{ob} R_L}}$$

CB Amplifier (**Using Hybrid Model**)



$$\boxed{R_i = \frac{v_e}{i_e}}$$

$$\boxed{v_e = h_{ib} i_e + h_{rb} v_c}$$

But, $A_i = -\frac{i_c}{i_e} \Rightarrow i_c = -A_i i_e$

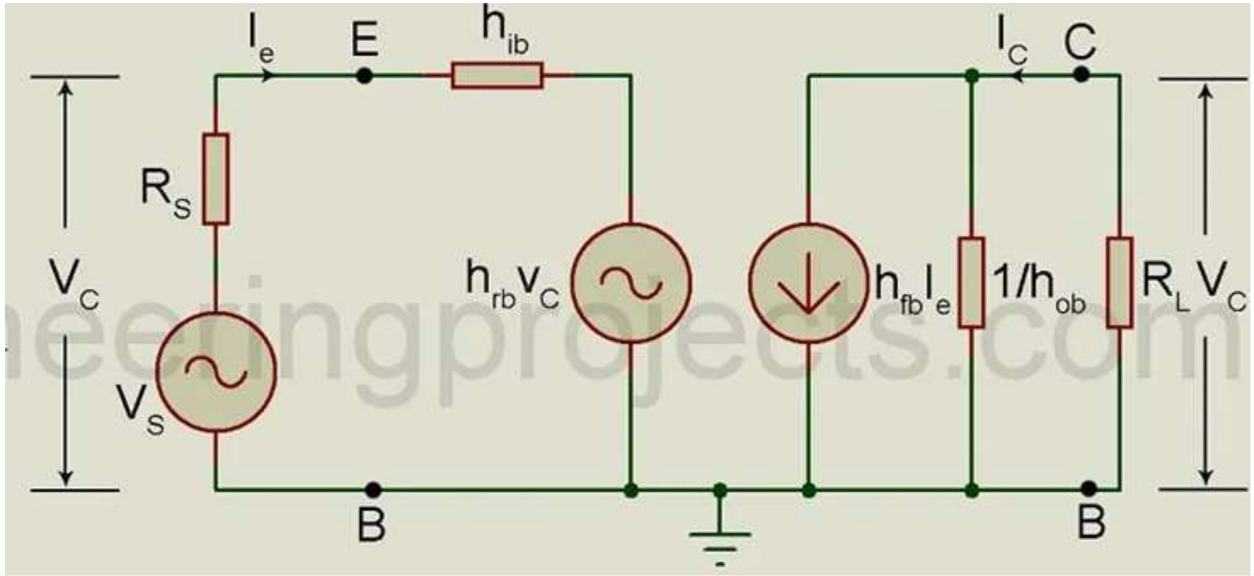
$$\boxed{v_c = i_L R_L = -i_c R_L = A_i i_e R_L}$$

$$\boxed{v_e = h_{ib} i_e + h_{rb}(A_i i_e R_L)}$$

$$\boxed{v_e = i_e (h_{ib} + h_{rb} A_i R_L)}$$

$$\boxed{\Rightarrow R_i = \frac{v_e}{i_e} = h_{ib} + h_{rb} A_i R_L}$$

CB Amplifier **(Using Hybrid Model)**



$$\boxed{A_v = \frac{v_c}{v_e}}$$

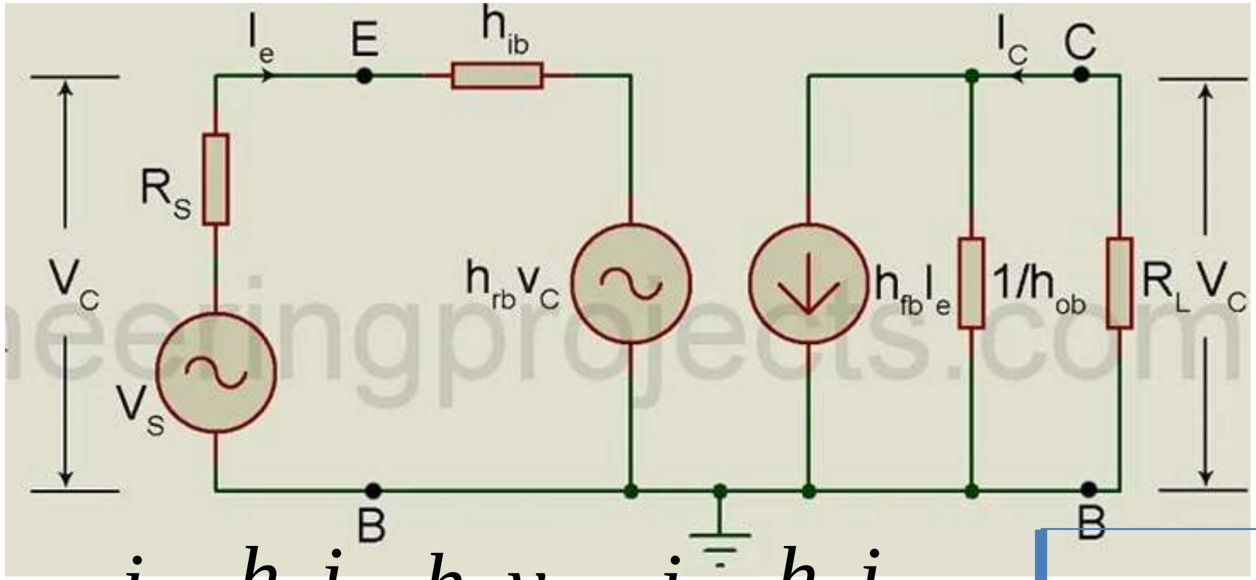
But, $A_i = -\frac{i_c}{i_e} \Rightarrow i_c = -A_i\, i_e$

$$\boxed{v_c = i_L R_L = -i_c R_L = A_i i_e R_L}$$

$$\boxed{\frac{1}{R_i} = \frac{i_e}{v_e}}$$

$$\boxed{\Rightarrow A_v = \frac{v_c}{v_e} = \frac{A_i i_e R_L}{v_e} = \frac{A_i R_L}{R_i}}$$

CB Amplifier **(Using Hybrid Model)**



$$\frac{i_c}{v_c}=\frac{h_{fb}i_e}{v_c}+\frac{h_{ob}v_c}{v_c}\Rightarrow\frac{i_c}{v_c}=\frac{h_{fb}i_e}{v_c}+h_{ob}$$

$$v_s=0, R_s i_e+h_{ib}i_e+h_{rb}v_c=0$$

$$(R_s+h_{ib})i_e=-h_{rb}v_c$$

Output Admittance Y_o

$$\boxed{Y_o=\frac{i_c}{v_c}}$$

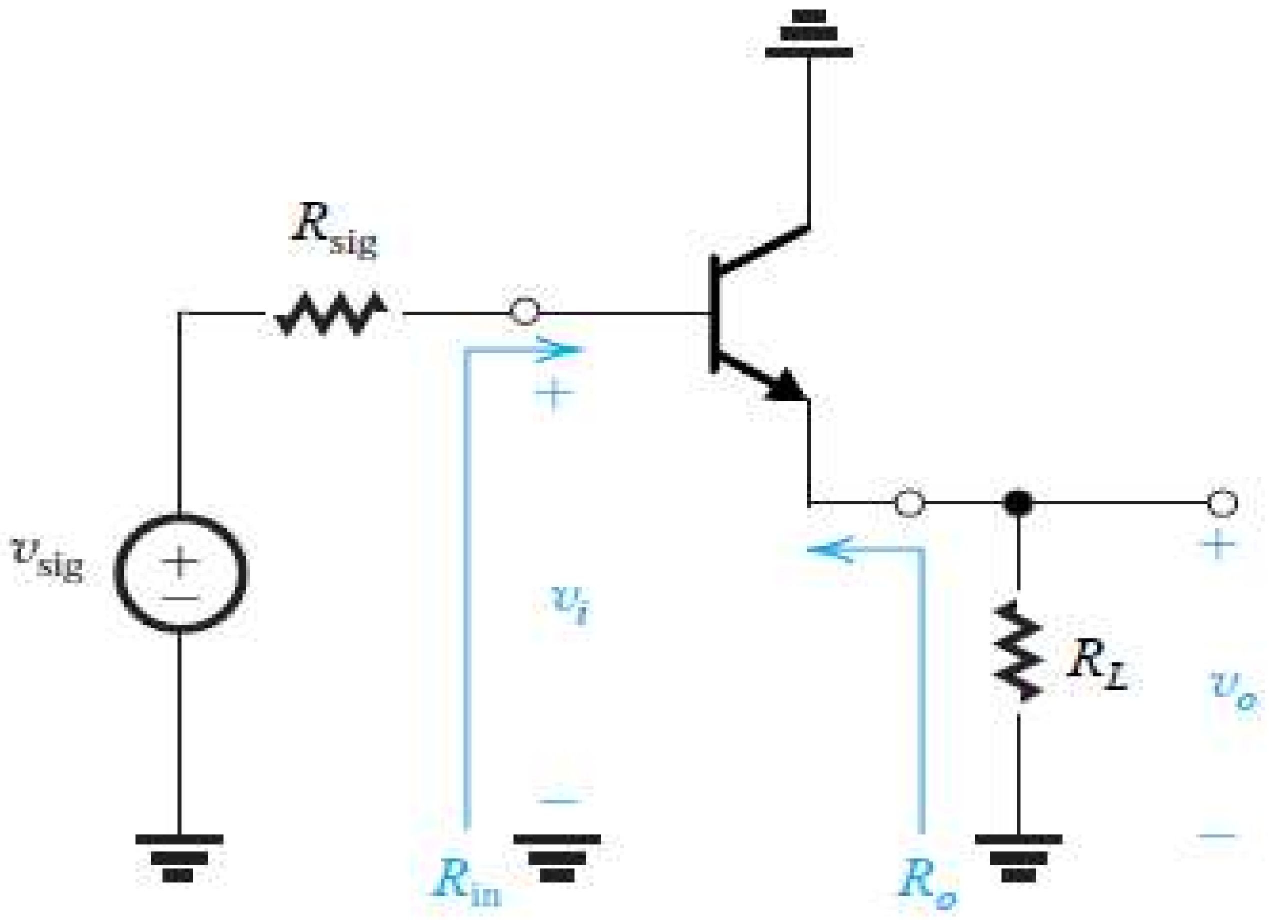
$$i_c=h_{fb}i_e+h_{ob}v_c$$

Dividing By V_c

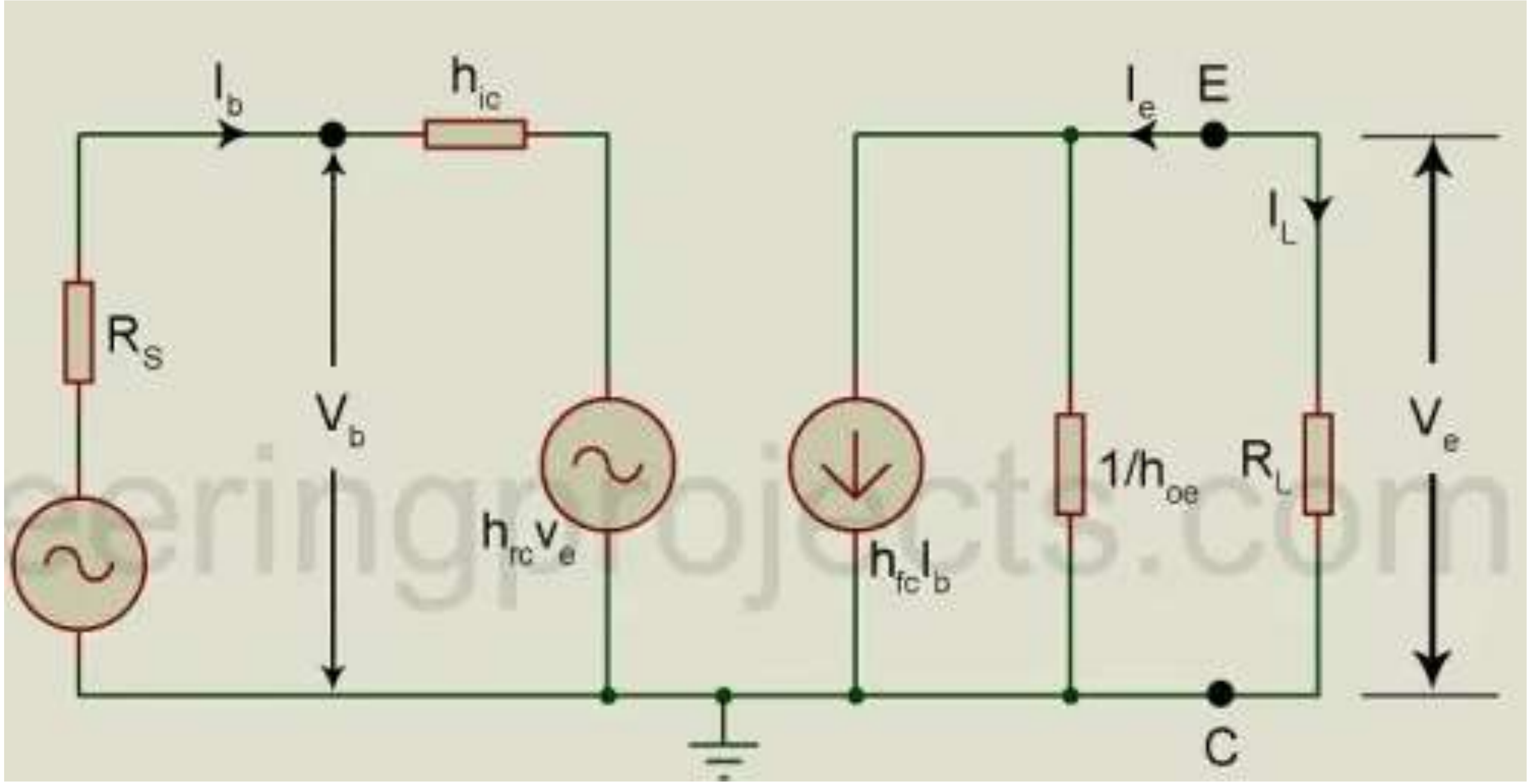
$$\boxed{\Rightarrow\frac{i_e}{v_c}=-\frac{h_{rb}}{R_s+h_{ib}}}$$

$$\boxed{\Rightarrow Y_0=h_{ob}-\frac{h_{fb}h_{rb}}{R_s+h_{ib}}\ and\ R_0=\frac{1}{Y_0}}$$

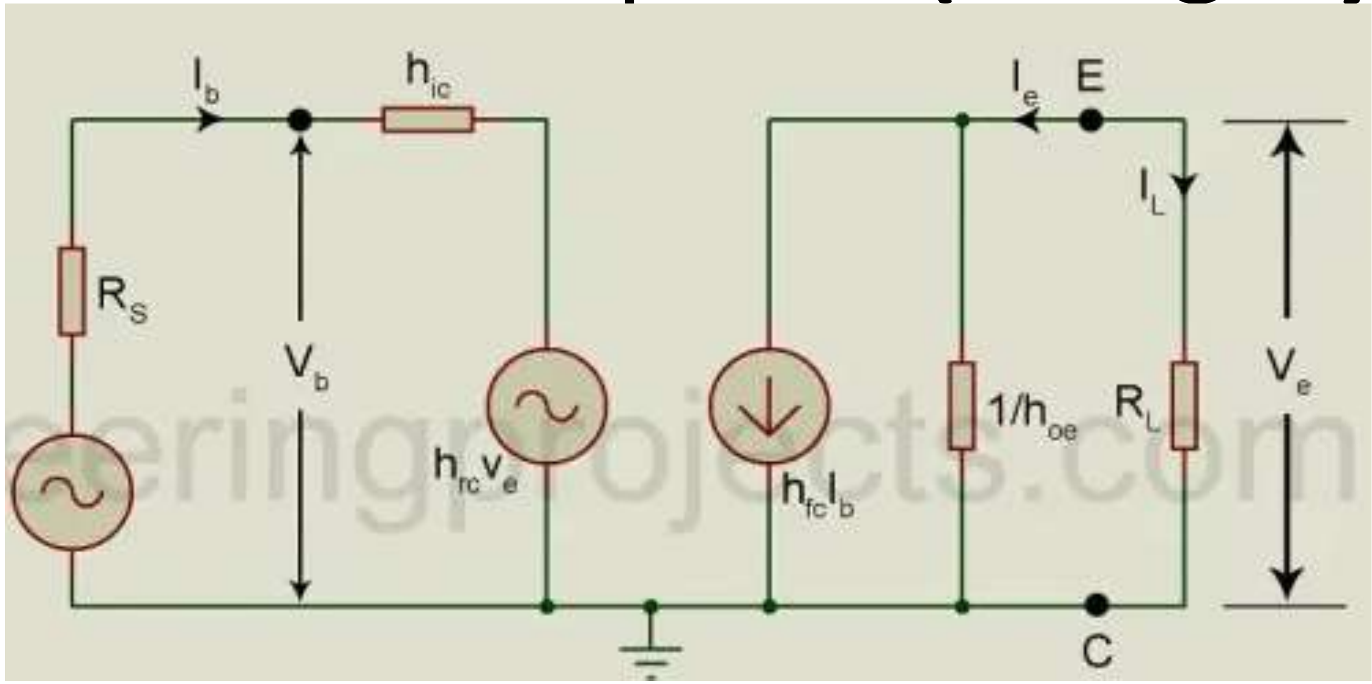
CC Amplifier(**Using Hybrid Model)**



CB Amplifier(**Using Hybrid Model)**



CB Amplifier (**Using Hybrid Model)**



$$A_i = \frac{i_L}{i_b} = -\frac{i_e}{i_b}$$

$$i_e = h_{fc} i_b + h_{oc} v_e$$

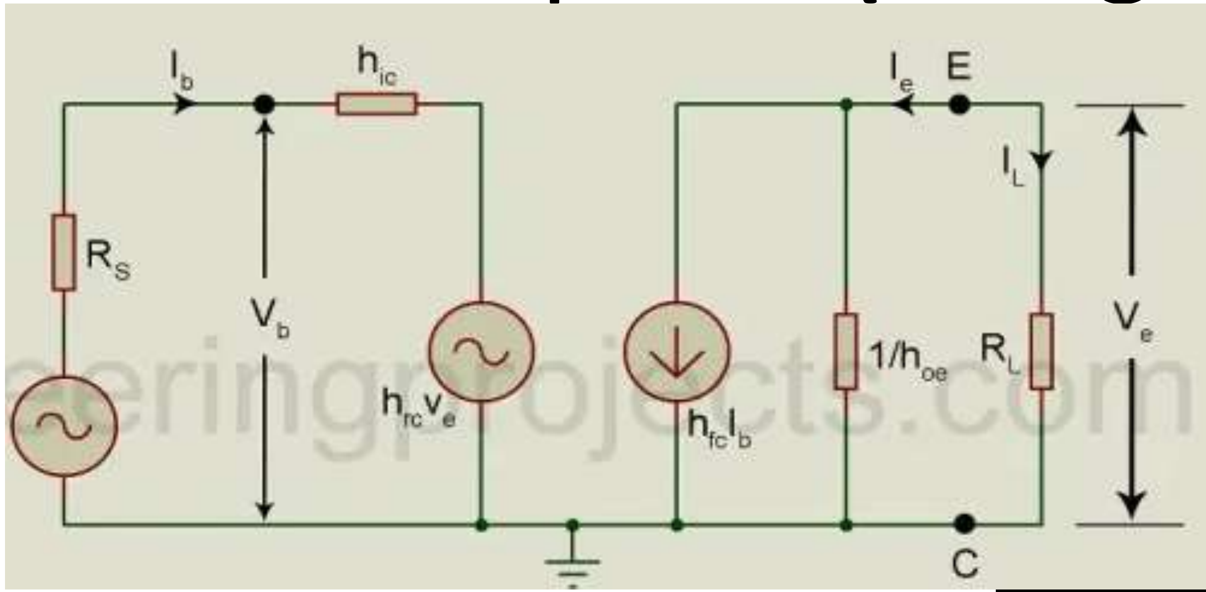
$$v_c = i_L R_L = -i_e R_L$$

$$i_e = h_{fc} i_b + h_{oc}(-i_e R_L)$$

$$i_e(1 + h_{oc} R_L) = h_{fc} i_b$$

$$\boxed{A_i = \frac{i_e}{i_b} = -\frac{h_{fc}}{1 + h_{oc} R_L}}$$

CB Amplifier **(Using Hybrid Model)**



$$\boxed{R_i = \frac{v_b}{i_b}}$$

$$\boxed{v_b = h_{ic} i_b + h_{rc} v_e}$$

But, $A_i = -\frac{i_e}{i_b} \Rightarrow i_e = -A_i\, i_b$

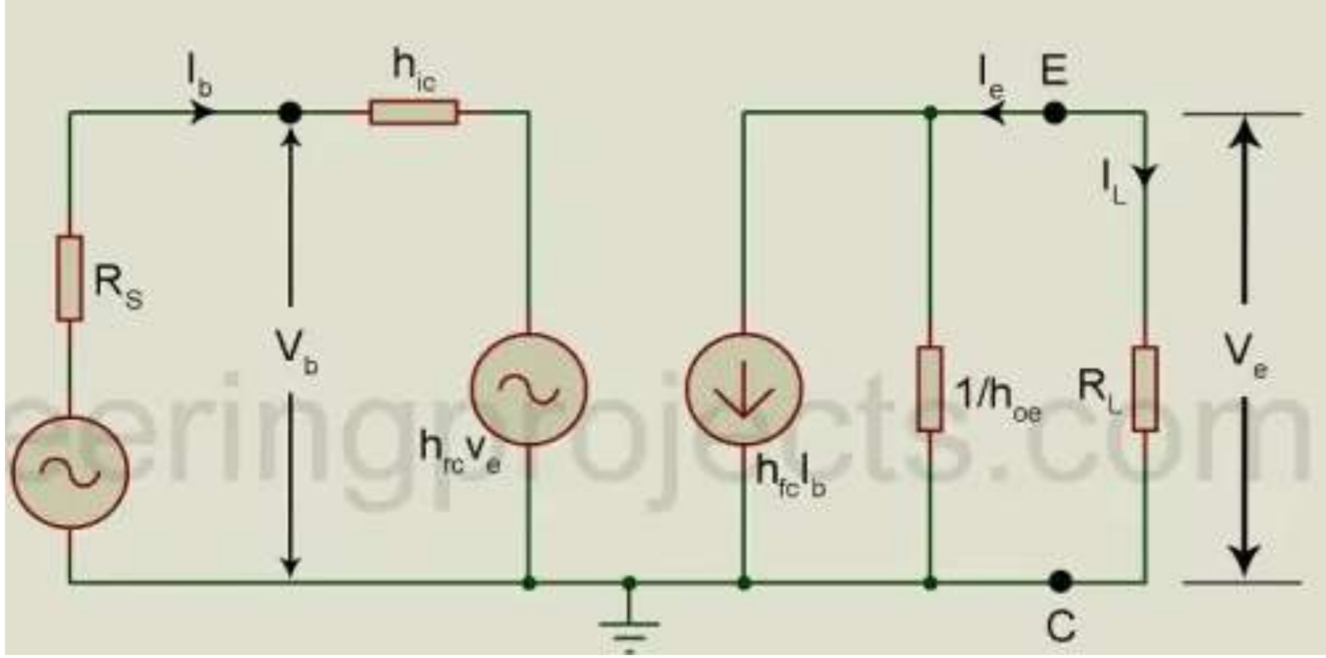
$$\boxed{v_e = i_L R_L = -i_e R_L = A_i i_b R_L}$$

$$\boxed{v_b = h_{ic} i_b + h_{rc}\left(A_i i_b R_L\right)}$$

$$\boxed{v_b = i_b\left(h_{ic} + h_{rc} A_i R_L\right)}$$

$$\boxed{\Rightarrow R_i = \frac{v_b}{i_b} = h_{ic} + h_{rc} A_i R_L}$$

CB Amplifier **(Using Hybrid Model)**



$$\boxed{A_v = \frac{v_e}{v_b}}$$

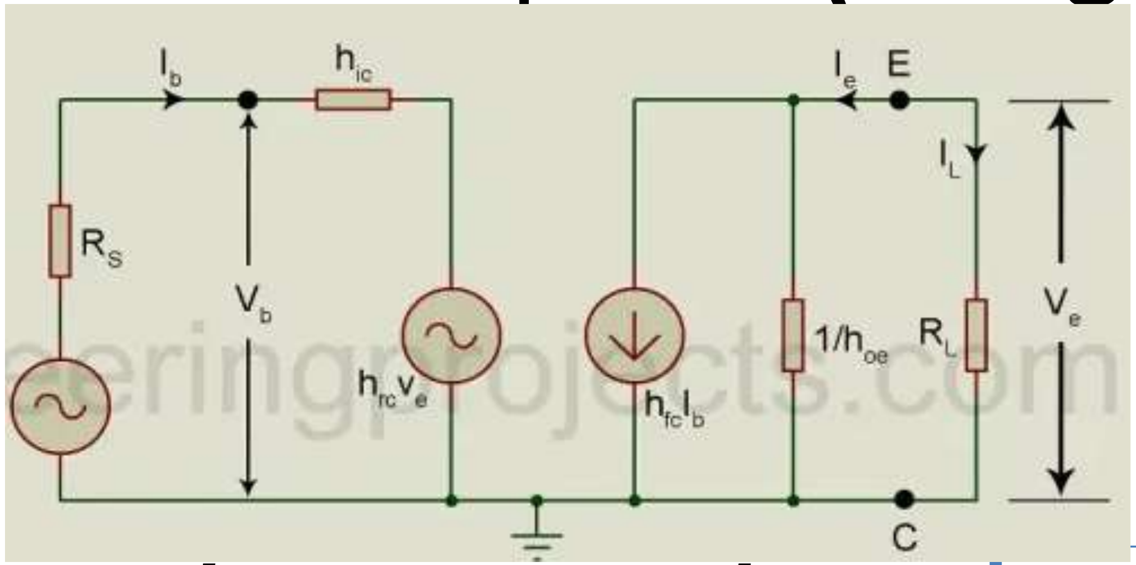
$$\text{But, } A_i = -\frac{i_e}{i_b} \Rightarrow i_e = -A_i\, i_b$$

$$\boxed{v_e = i_L R_L = -i_e R_L = A_i i_b R_L}$$

$$\boxed{\frac{1}{R_i} = \frac{i_b}{v_b}}$$

$$\boxed{\Rightarrow A_v = \frac{v_e}{v_b} = \frac{A_i i_b R_L}{v_b} = \frac{A_i R_L}{R_i}}$$

CB Amplifier **(Using Hybrid Model)**



Output Admittance Y_o

$$\boxed{Y_o = \frac{i_e}{v_e}}$$

$$i_e = h_{fc} i_b + h_{oc} v_e$$

Dividing By V_e

$$\frac{i_e}{v_e} = \frac{h_{fc} i_b}{v_e} + \frac{h_{ob} v_e}{v_e} \Rightarrow \frac{i_e}{v_e} = \frac{h_{fc} i_b}{v_e} + h_{oc}$$

$$v_s = 0, R_s i_b + h_{ic} i_b + h_{rc} v_e = 0$$

$$(R_s + h_{ic}) i_b = -h_{rc} v_e$$

$$\boxed{\Rightarrow \frac{i_b}{v_e} = -\frac{h_{rc}}{R_s + h_{ic}}}$$

$$\boxed{\Rightarrow Y_0 = h_{oc} - \frac{h_{fc} h_{rc}}{R_s + h_{ic}} \text{ and } R_0 = \frac{1}{Y_0}}$$

Conversion Formulae for Hybrid Parameters

From CB to CE	From CE to CB	From CE to CC
$h_{ie} = \frac{h_{ib}}{1+h_{fb}}$	$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$	$h_{ic} = h_{ie}$
$h_{oe} = \frac{h_{ob}}{1+h_{fb}}$	$h_{ob} = \frac{h_{oe}}{1+h_{fe}}$	$h_{oc} = h_{oe}$
$h_{fe} = \frac{-h_{fb}}{1+h_{fb}}$	$h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$	$h_{fc} = (1+h_{fe})$
$h_{re} = \frac{h_{ib}\,h_{ob}}{1+h_{fb}} - h_{rb}$	$h_{rb} = \frac{h_{ie}\,h_{oe}}{1+h_{fe}} - h_{re}$	$h_{rc} = 1 - h_{re} \cong 1$

CE Amplifier Circuit

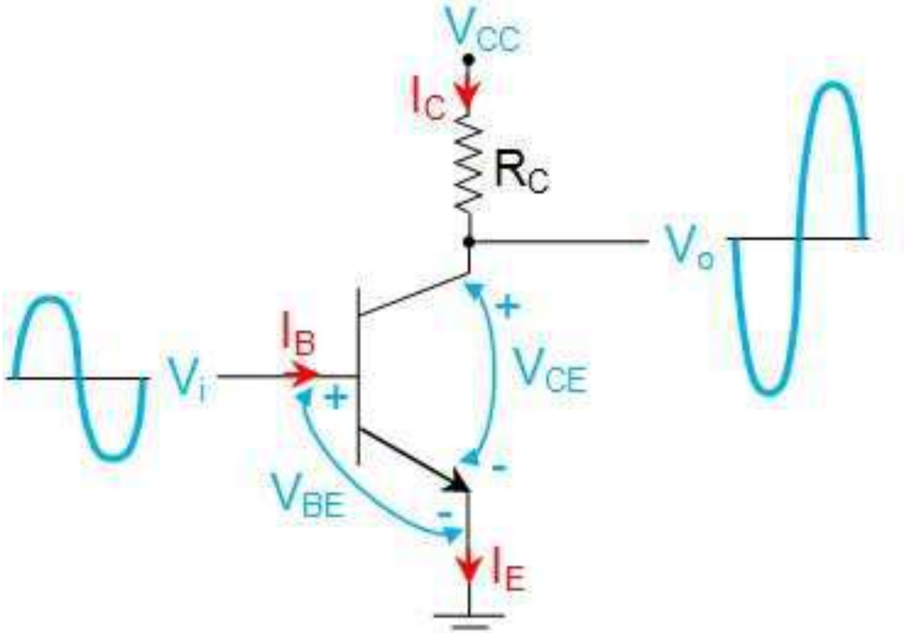


Figure 1   A Simple Common Emitter Amplifier

$$V_0 = V_{CC} - I_C R_C$$

❖Collector terminal (output terminal) is connected to supply voltage V_{CC} through the collector resistor R_C.

❖Base terminal is provided with the AC signal which needs to be amplified.

❖Emitter terminal is grounded (hence also referred to as Grounded Emitter configuration).

CE Amplifier Circuit

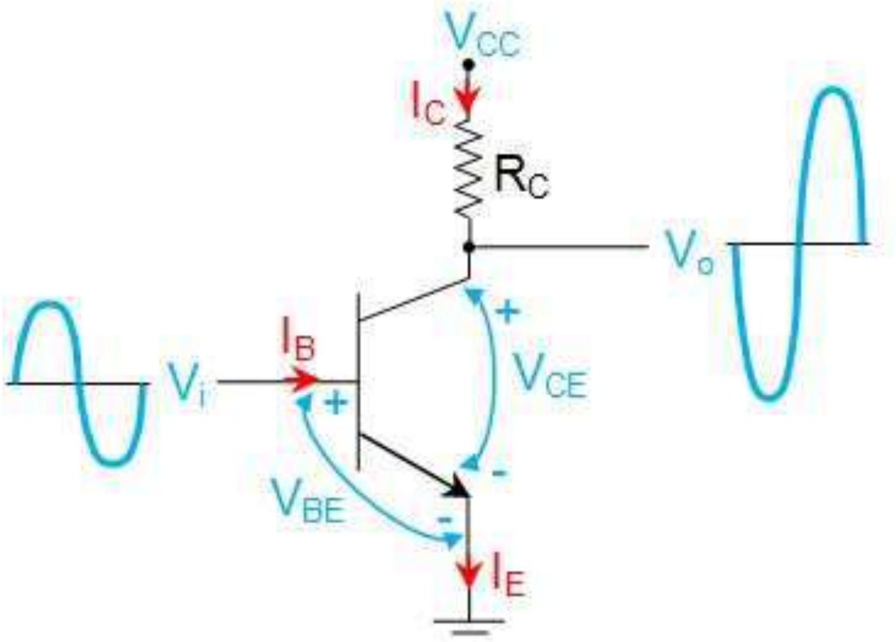


Figure 1 A Simple Common Emitter Amplifier

❖In this kind of arrangement, as the input voltage V_i increases, the base current I_B also increases which in turn increases the collector current I_C.

❖This causes an increase in the voltage drop across the collector resistor, R_C which results in a decreased output voltage V_0 as emphasized by the following relationship

$$V_0 = V_{CC} - I_C R_C$$

CE Amplifier Circuit

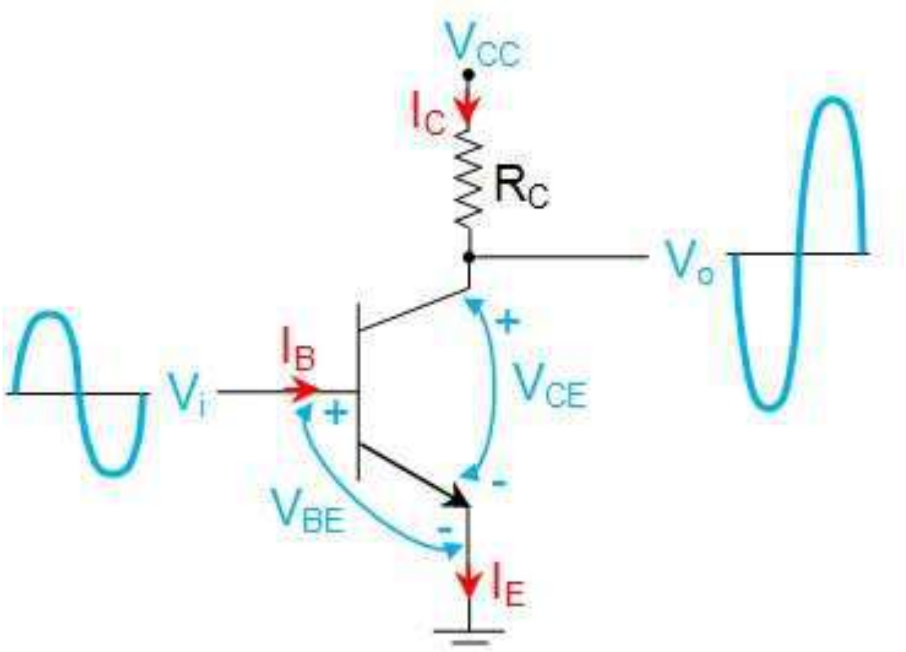


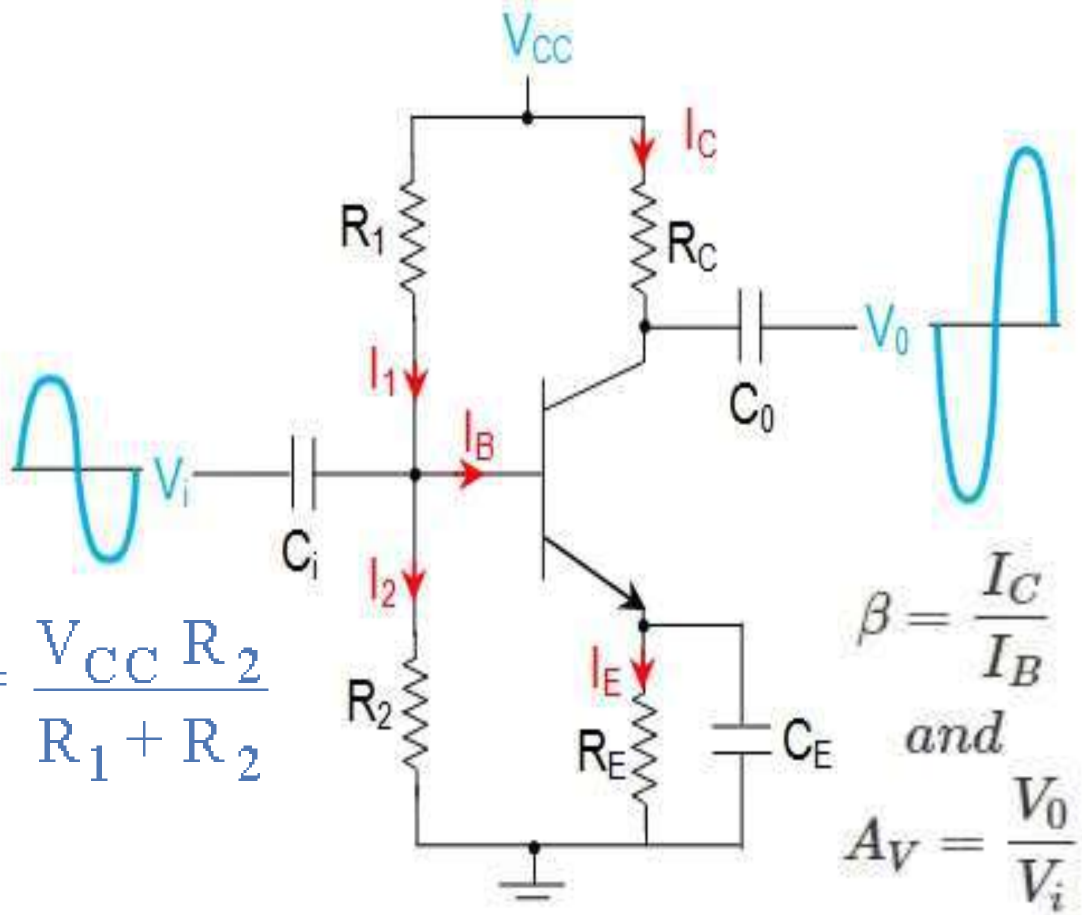
Figure 1 A Simple Common Emitter Amplifier

$$V_0 = V_{CC} - I_C R_C$$

❖Similarly as the input voltage goes on decreasing, I_B and hence I_C decrease, due to which the voltage drop across R_C also decreases thereby increasing the output voltage.

❖This indicates that for the positive half-cycle of the input waveform, one would get amplified negative half-cycle while for the negative input pulse, the output would be a amplified positive pulse. Hence there exists a phase-shift of 180^o between the input and the output waveforms of the **common emitter amplifier** for which it is also referred to as [Inverting Amplifier].

CE Amplifier Circuit



$$V_B = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$\beta = \frac{I_C}{I_B}$$

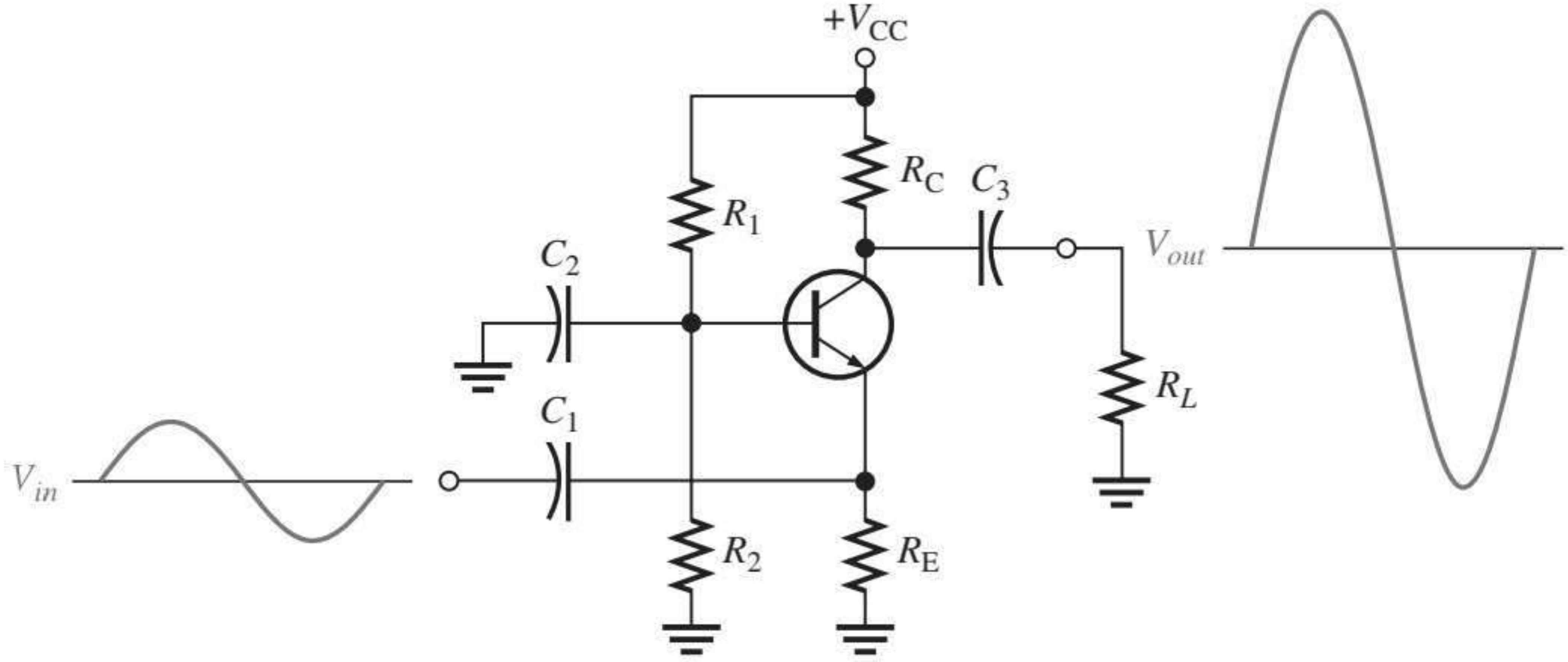
and

$$A_V = \frac{V_0}{V_i} = -\frac{R_C}{R_E}$$

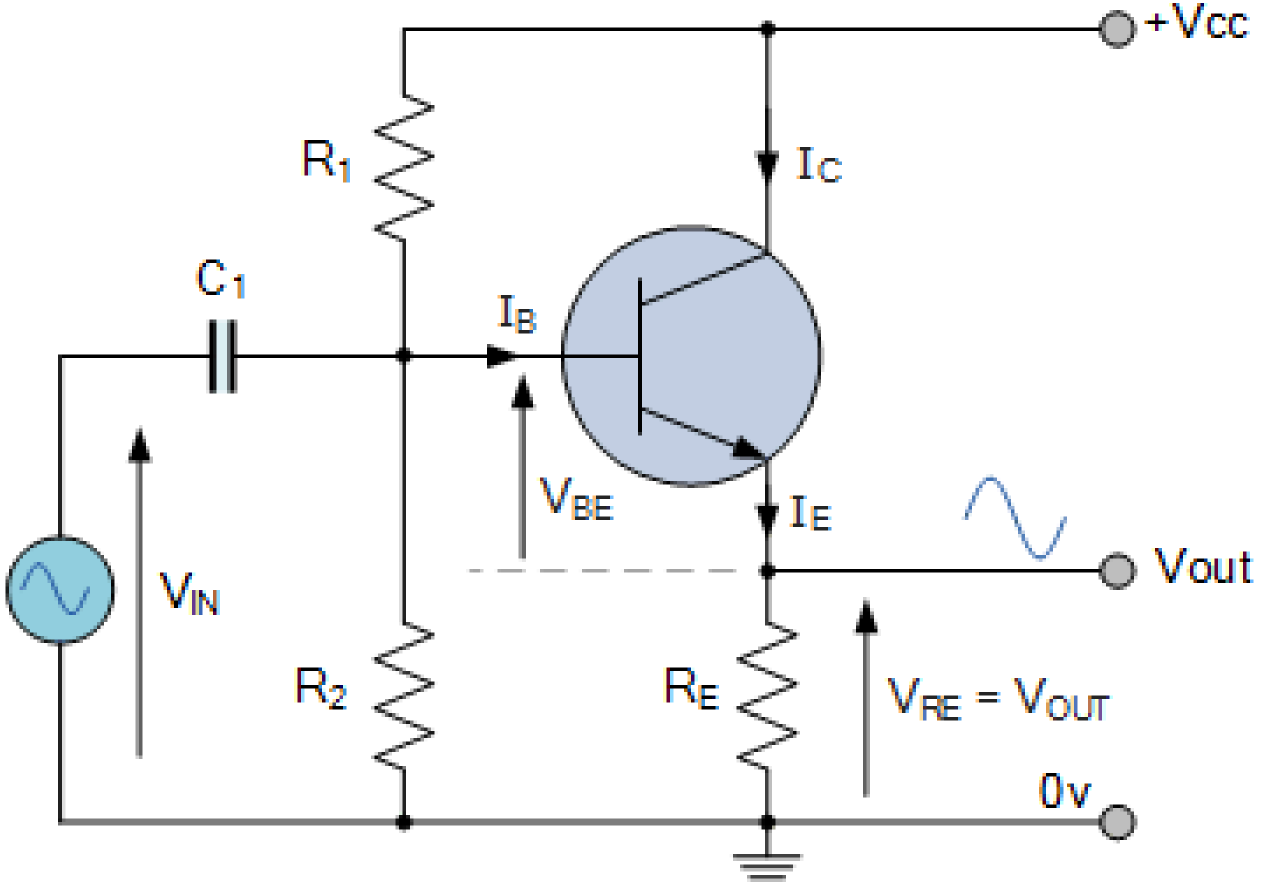
Figure 2 Common Emitter Amplifier with Biasing and Decoupling Details

- ❖**R1** and **R2**-Voltage Divider Bias
- ❖ Ci and Co-Coupling Capacitor for blocks any DC Components and passes AC Signal for Amplification
- ❖ Rc for Controlling Ic and Provide Output Voltage.
- ❖ RE provides biasing stabilization.
- ❖ CE provides low reactance path to the amplified AC signal.

CB Amplifier Circuit



CC Amplifier Circuit(Emitter Follower)



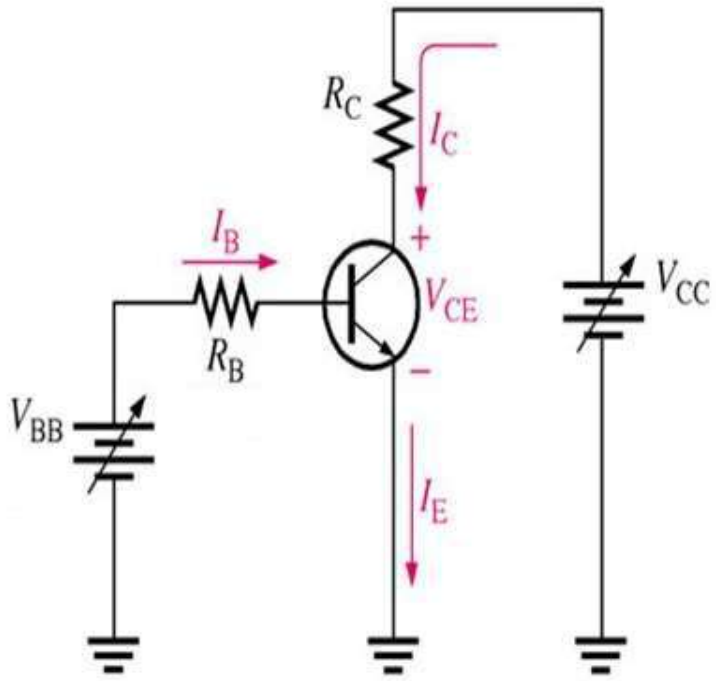
Comparison of BJT Amplifier

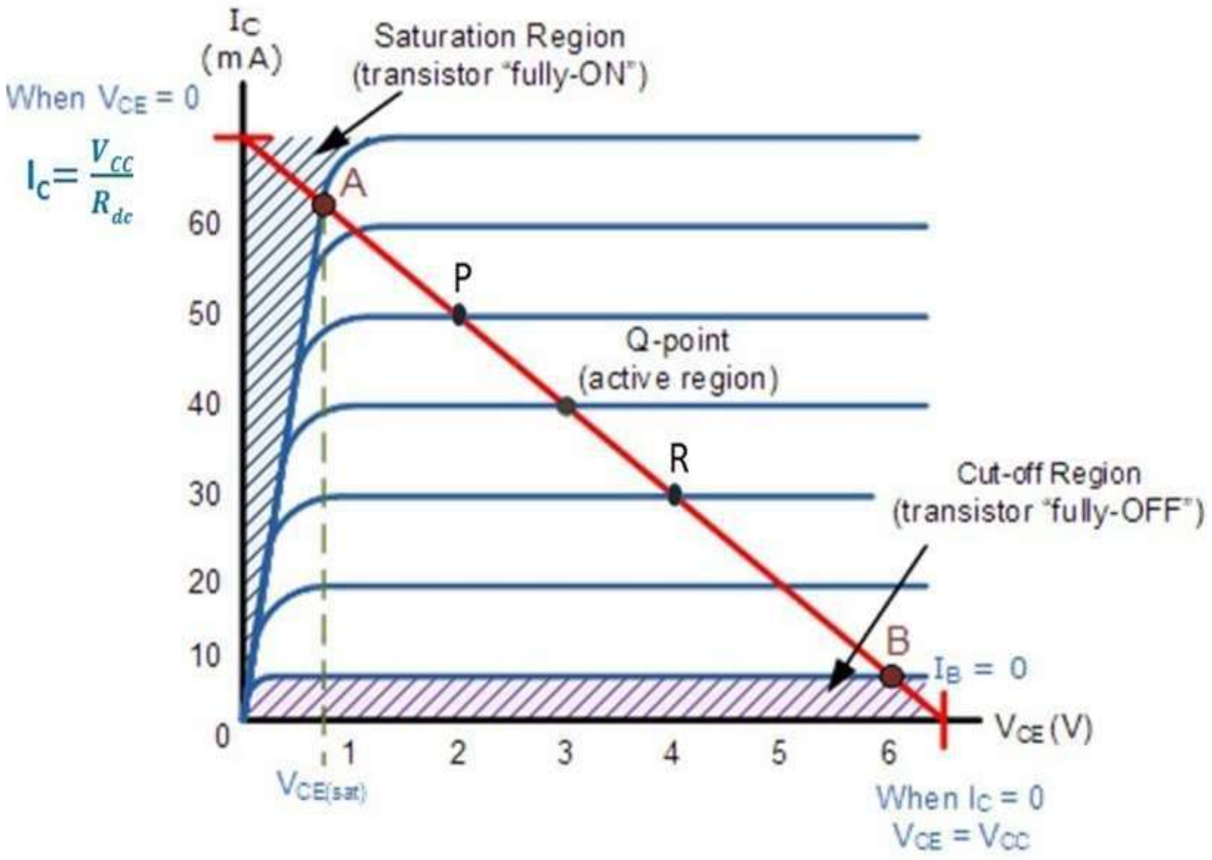
Characteristics	CE Amplifier	CB Amplifier	CC amplifier (Emitter Follower)
Current Gain	High	Less Than Unity	High
Voltage Gain	High	High	Less Than Unity
Input Resistance	Medium	Lowest	Highest
Output Resistance	Moderately High	Highest	Lowest
Phase Shift between Input and Output	180 °	0°	0°
Application	For Audio Frequency Applications	For High Frequency Applications	For Impedance Matching

Biasing in BJT Amplifier Circuits

- Fixed Bias(Base Bias)
- Self Bias/Voltage Divider Bias Circuits
- **Biasing Using a Collector-to-Base Feedback Resistor**
- Biasing using a Constant-Current Source

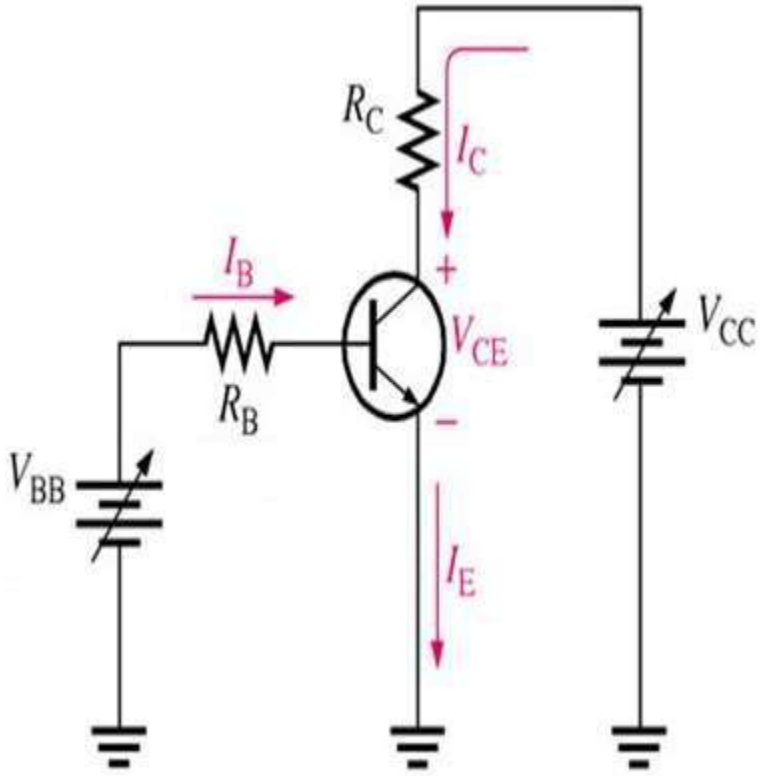
Biasing in BJT Amplifier Circuits

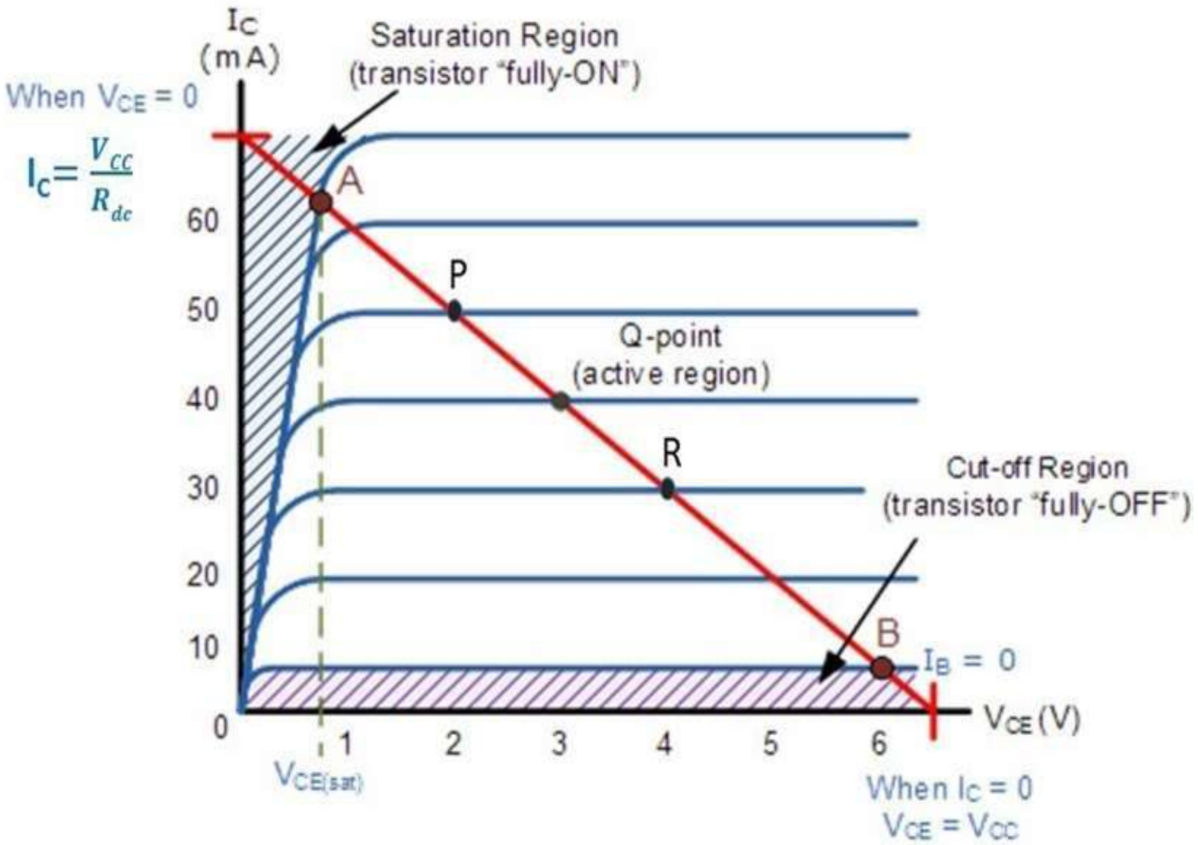




❖ The biasing problem is that of establishing a **constant dc current** in the collector of the BJT.

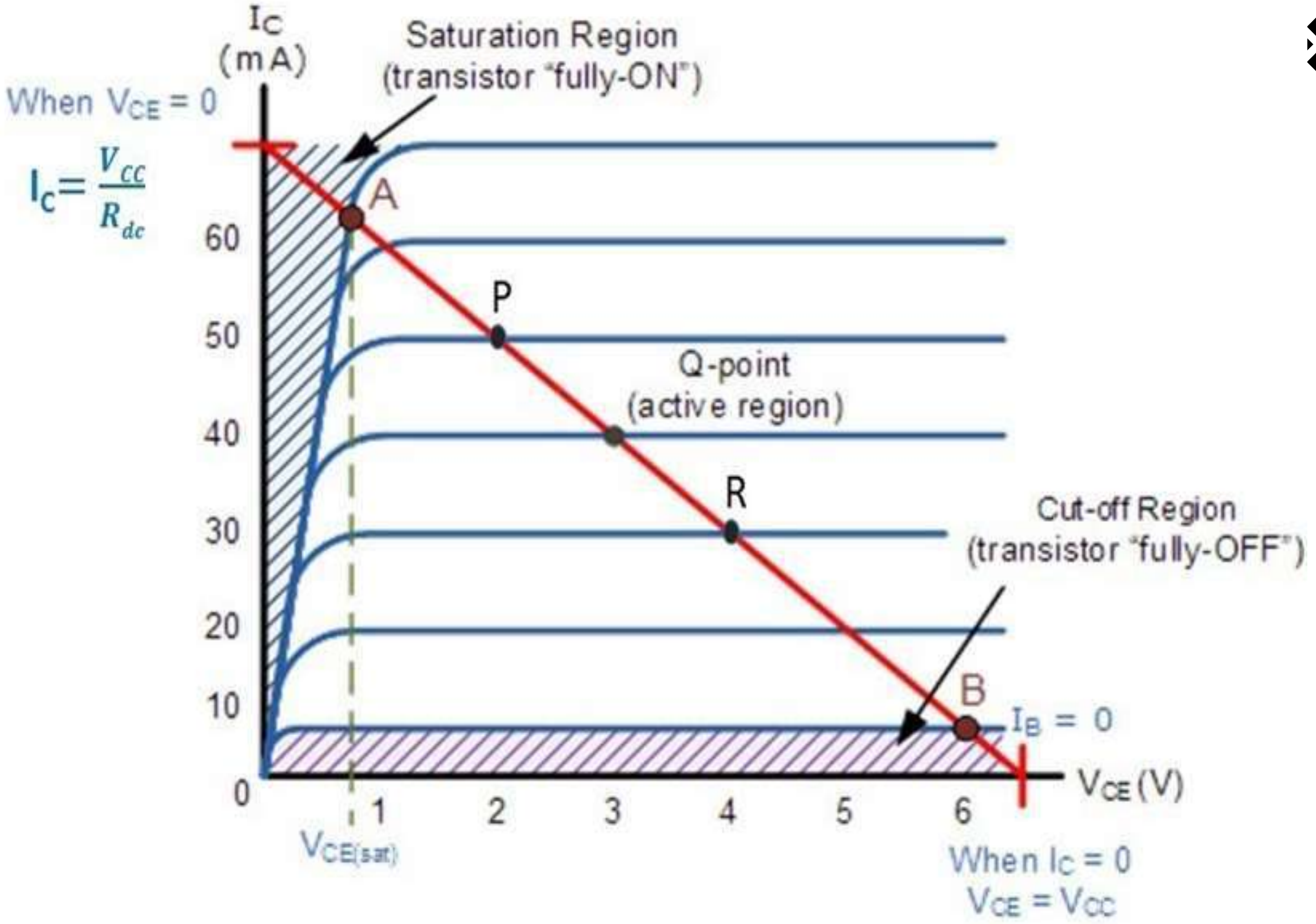
Biasing in BJT Amplifier Circuits





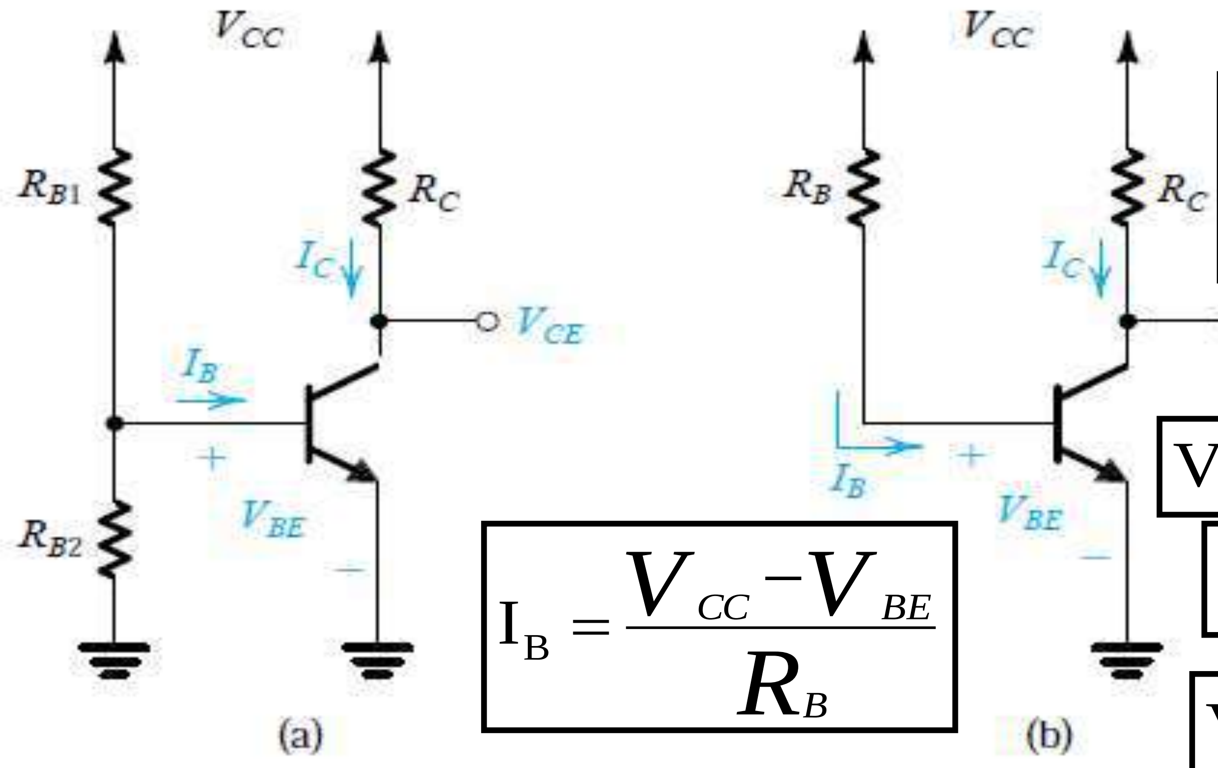
❖ This current has to be **calculable, predictable, and insensitive** to variations in temperature and to the large variations in the value of β encountered among transistors of the same type.

Biasing in BJT Amplifier Circuits



- Another important consideration in bias design is **locating the dc bias point** in **the *iC–vCE*** *plane to allow for maximum* output signal swing.

Fixed Bias/Base Bias



$$\boxed{I_C = \beta I_B}$$

$$\boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}}$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

$$\boxed{V_E = 0}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$$

$$\boxed{V_{CE} = V_C - V_E} \quad \boxed{V_{CE} = V_C}$$

$$\boxed{V_{BE} = V_B - V_E} \quad \boxed{V_{BE} = V_B}$$

Two obvious schemes for biasing the BJT: **(a) by fixing *VBE; (b) by fixing IB. Both result*** in wide variations in *IC and hence in VCE and therefore are considered to be "bad." Neither scheme is* recommended.

Fixed Bias/Base Bias

- **First, attempting to bias the BJT by fixing the voltage *VBE by, for instance,* using a voltage divider across the power supply *VCC, is not* a viable approach:**
- The very sharp exponential relationship ***iC–vBE*** *means that any small and* inevitable differences in *VBE from the desired value will result in large differences in IC and* in *VCE.*
- *Second, biasing the BJT by establishing a constant current in the base,*where is also not a recommended approach.
- Here the typically large variations in the value of β among units of the same device type will result in correspondingly **large variations** in *IC and hence in VCE.*

Fixed Bias/Base Bias

ADVANTAGES OF FIXED BIAS CIRCUIT

1. Simple circuit as it uses few components.

2. It provides max flexibility, because the biasing conditions are easily set by changing the value of R_B.

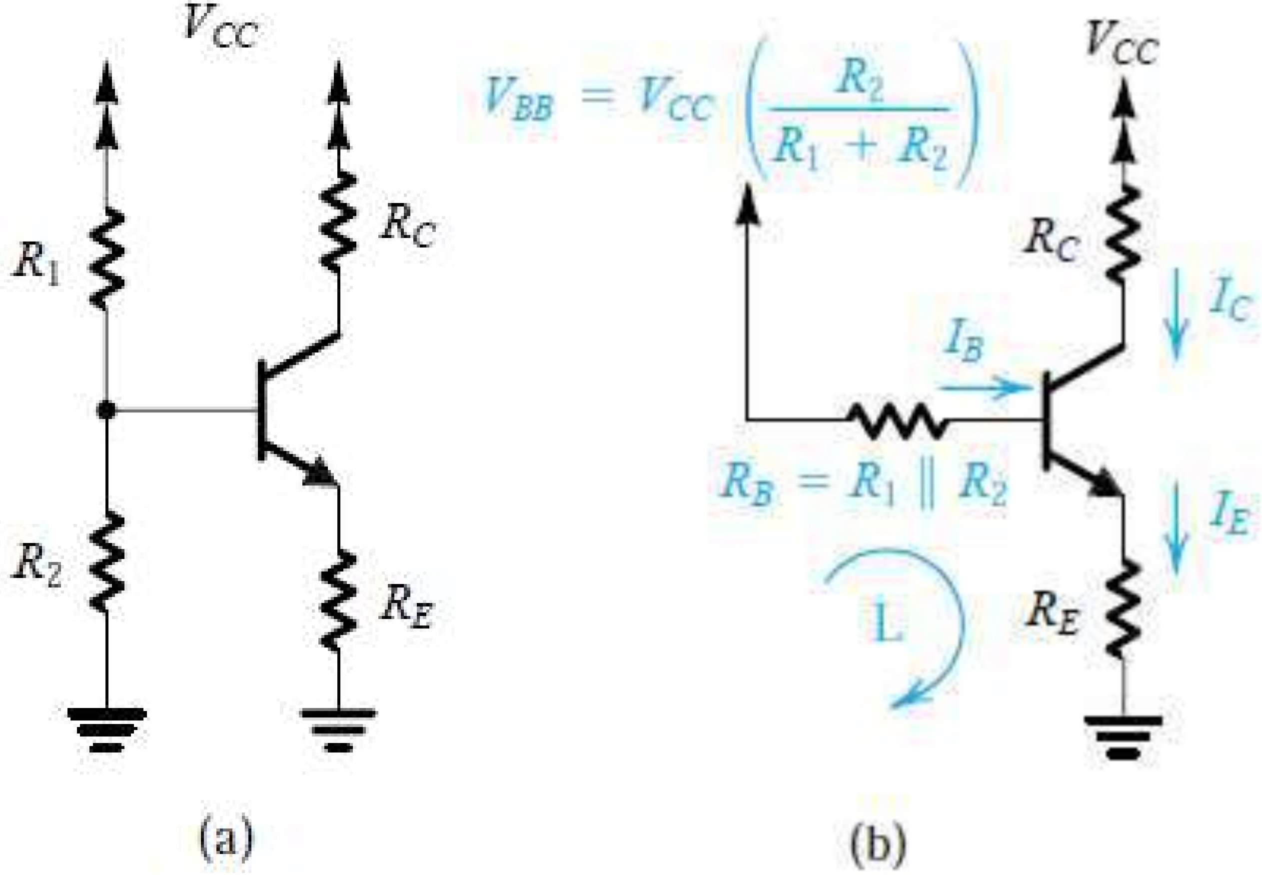
DISADVANTAGES OF FIXED BIAS CIRCUIT

Poor stability

1. There is no means to stop self increase of I_C due to increase in temperature.
   So, thermal stability is not provided.

2. If β increases due to transistor replacement then, Ic also increases by factor β
Therefore there is a chance of thermal runaway $I_C = \beta I_B$

Self Bias/Voltage Divider Bias



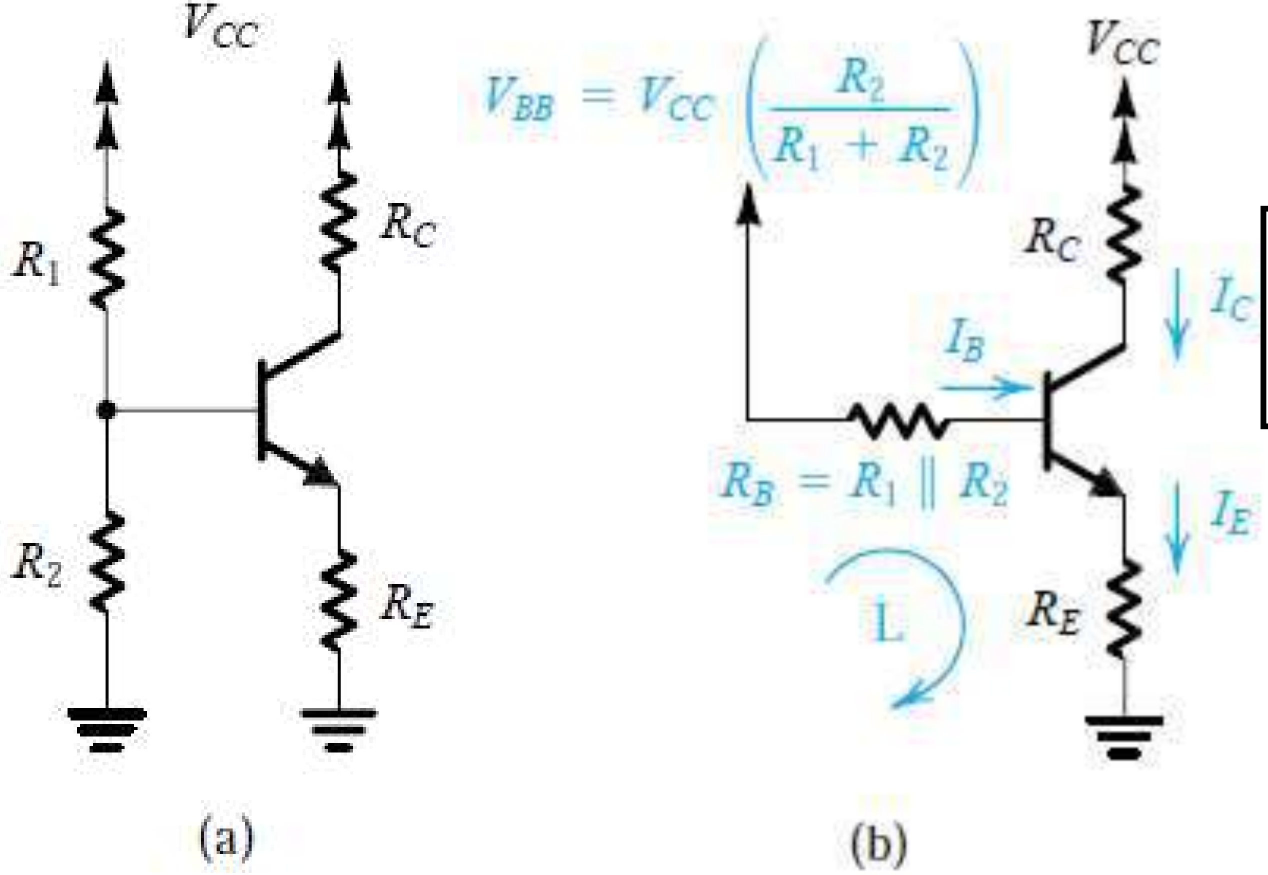
Classical biasing for BJTs using a single power supply: **(a) circuit; (b) circuit with the** voltage divider supplying the base replaced with its Thévenin equivalent.

❖The arrangement most commonly used for biasing a discrete-circuit transistor amplifier if only a **single power supply** is available.

❖The technique consists of supplying the base of the transistor with a fraction of the supply voltage *VCC through the* ***voltage*** **divider** ***R1, R2.***

❖*In addition,* ***a resistor RE*** *is connected to the emitter.*

Self Bias/Voltage Divider Bias

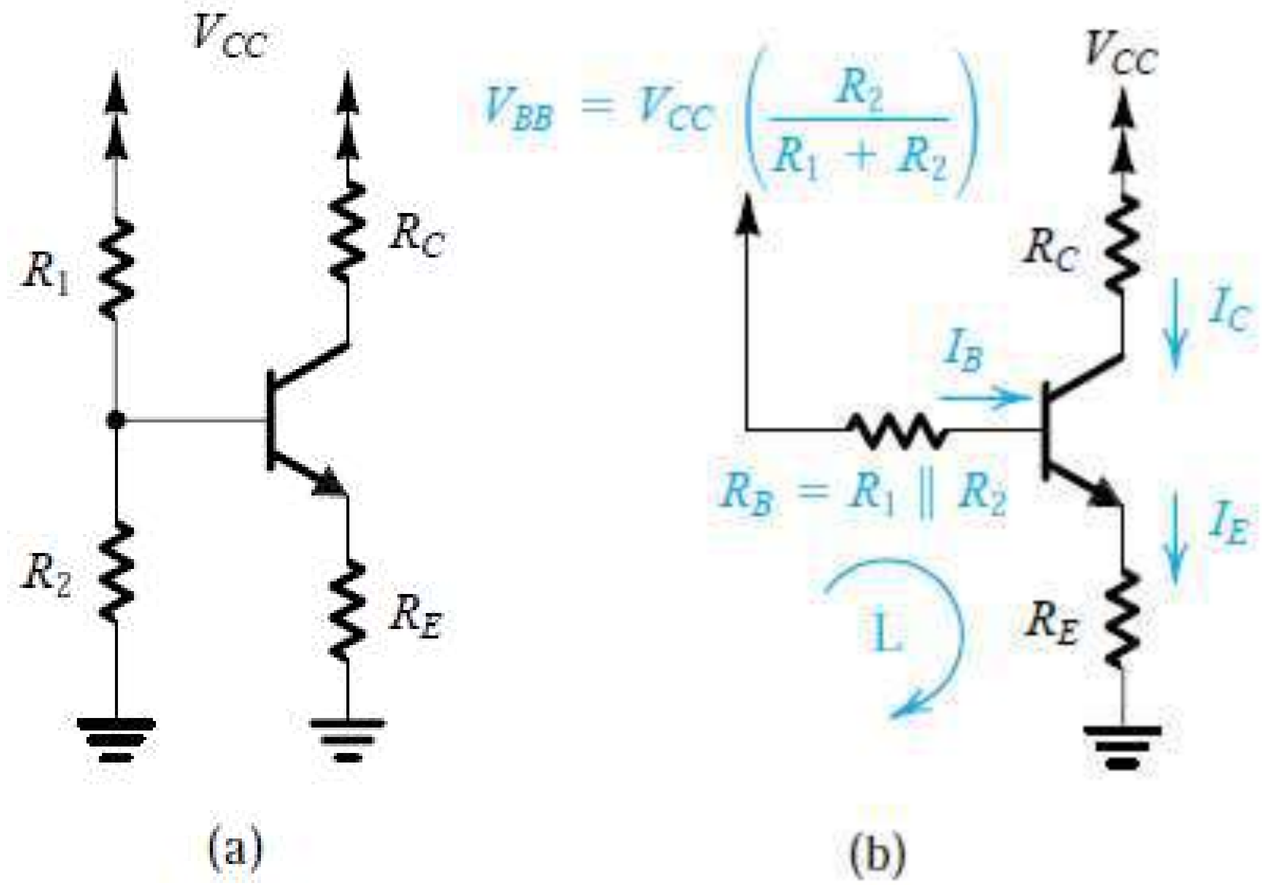


$$V_{BB} = V_{CC}\left(\frac{R_2}{R_1 + R_2}\right)$$

$$R_B = \left(\frac{R_1 R_2}{R_1 + R_2}\right)$$

Classical biasing for BJTs using a single power supply: **(a) circuit; (b) circuit with the** voltage divider supplying the base replaced with its Thévenin equivalent.

Self Bias/Voltage Divider Bias



Classical biasing for BJTs using a single power supply: **(a) circuit; (b) circuit with the** voltage divider supplying the base replaced with its Thévenin equivalent.

The current *IE can be determined by writing a Kirchhoff loop equation for the base–emitter–* ground loop, labeled L, and substituting

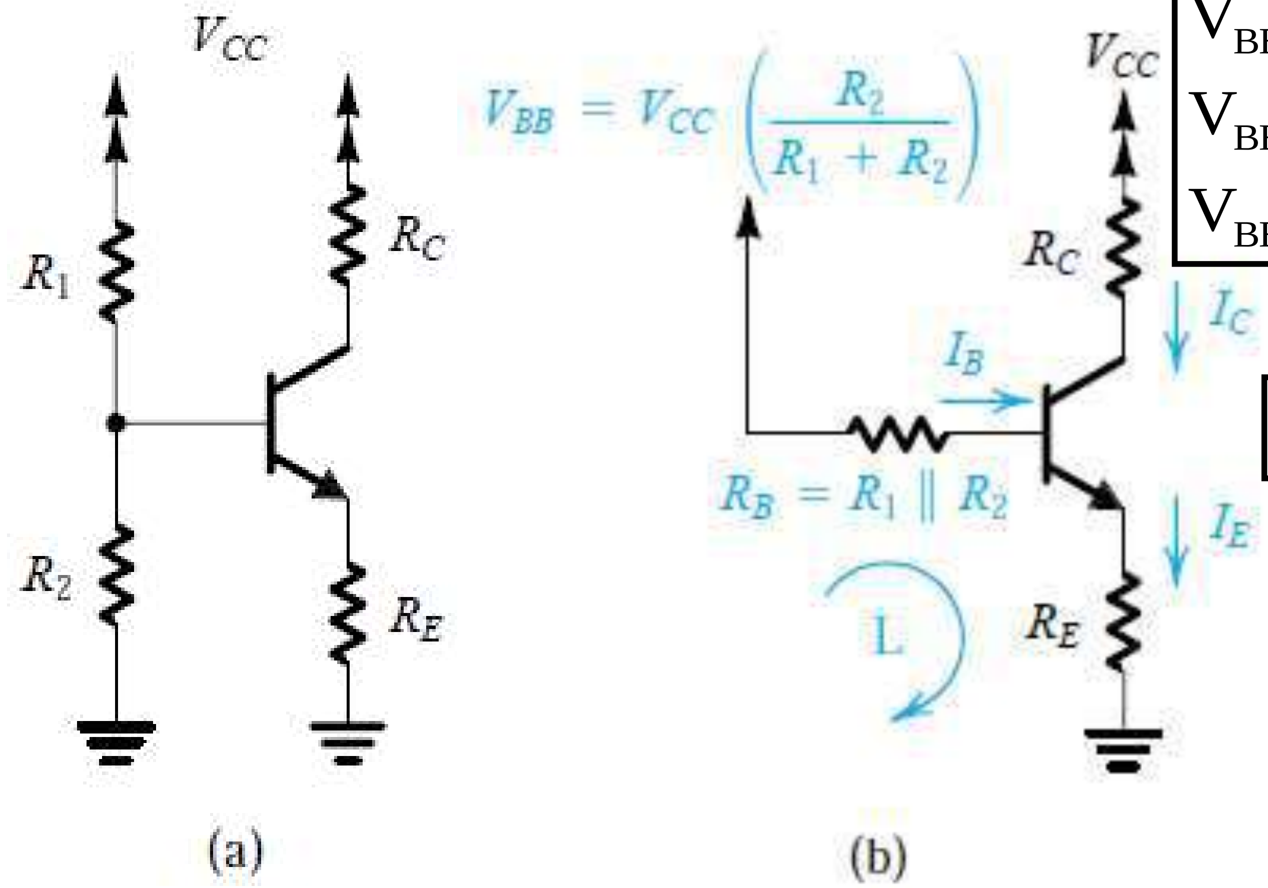
$$\boxed{I_B = \frac{I_E}{\beta + 1}}$$

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

$$V_{BB} = \left(\frac{I_E}{\beta + 1}\right) R_B + V_{BE} + I_E R_E$$

$$\boxed{I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{\beta + 1}}}$$

Self Bias/Voltage Divider Bias

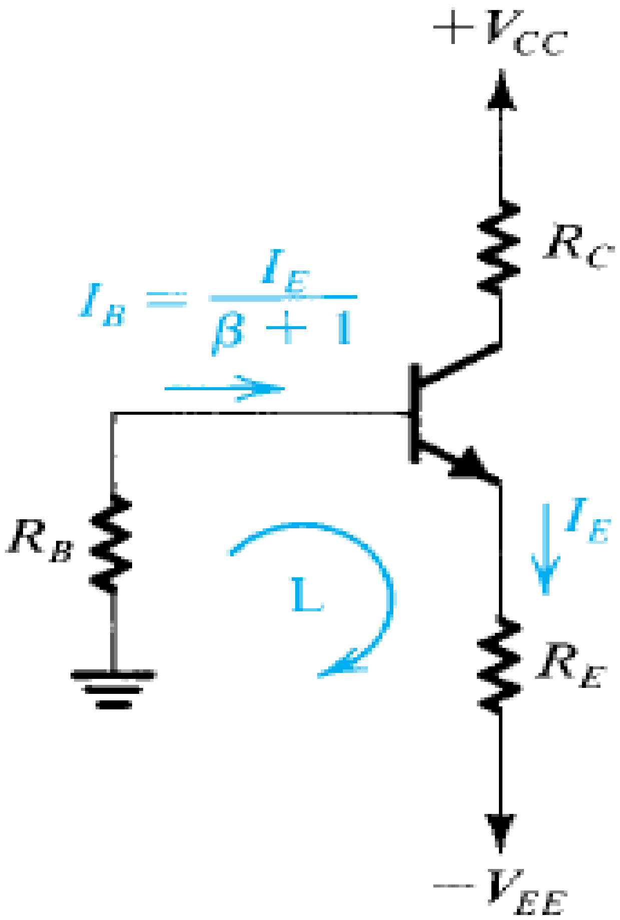


$$\boxed{\begin{aligned} V_{BB} &= V_{BE} + I_B R_B + I_E R_E \\ V_{BE} &= V_{BB} - I_B R_B - (I_B + I_C) R_E \\ V_{BE} &= V_{BB} - I_B (R_B + R_E) - I_C R_E \end{aligned}}$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C - I_E R_E}$$

Classical biasing for BJTs using a single power supply: **(a) circuit; (b) circuit with the** voltage divider supplying the base replaced with its Thévenin equivalent.

Self Bias/Voltage Divider Bias



❖Biasing the BJT using two power supplies. Resistor *RB is* needed only if the signal is to be capacitively coupled to the base.

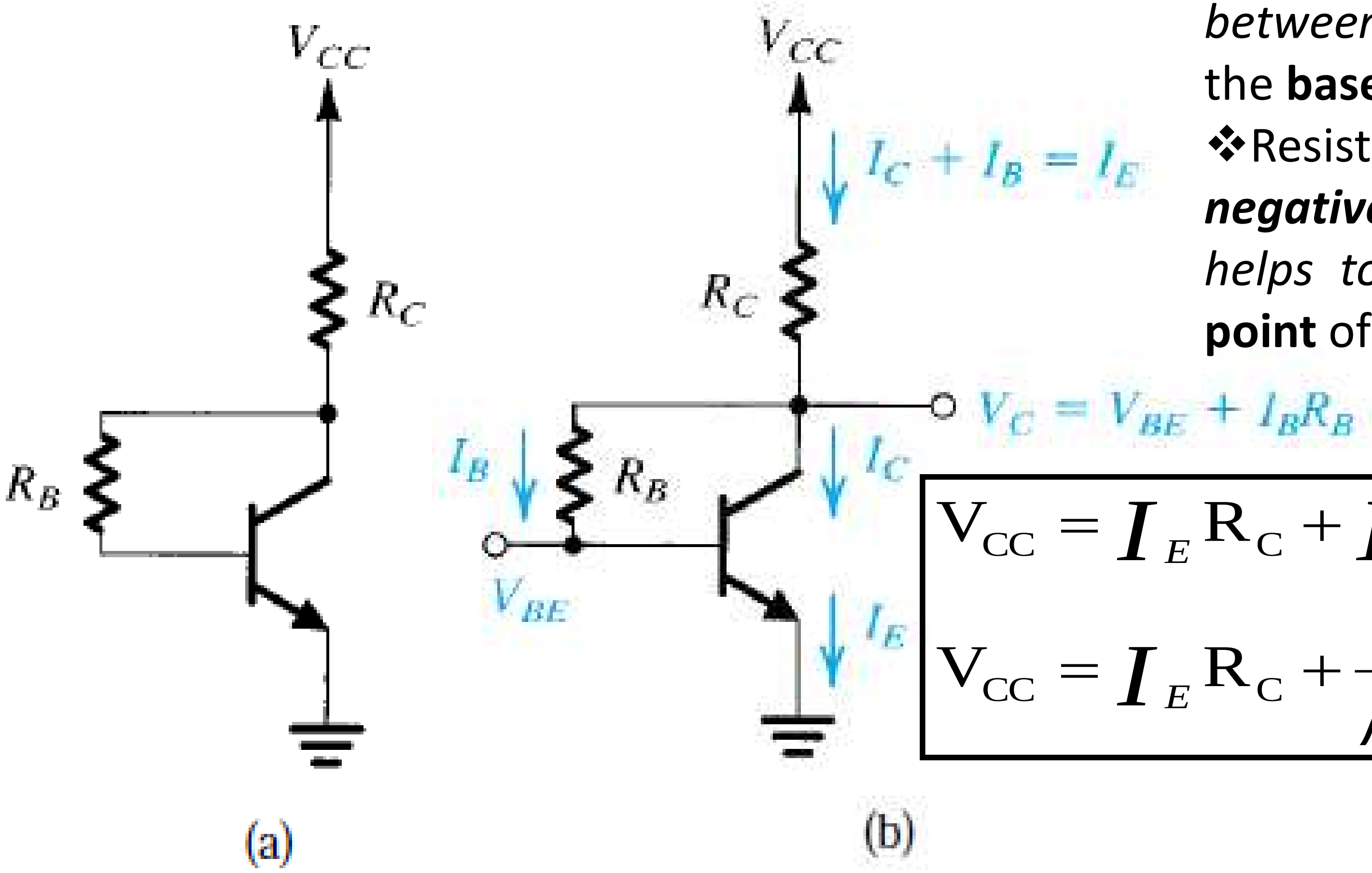
❖ Otherwise, the base can be connected directly to ground, or to a grounded signal source, resulting in almost total β -independence of the bias current.

$$\boxed{I_E = \frac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{\beta + 1}}}$$

Biasing Using a Collector-to-Base Feedback Resistor

❖The circuit employs a **resistor** ***RB*** *connected between the* ***collector*** and the **base**.

❖Resistor *RB provides* ***negative feedback****, which helps to* ***stabilize*** *the* ***bias point*** of the BJT.

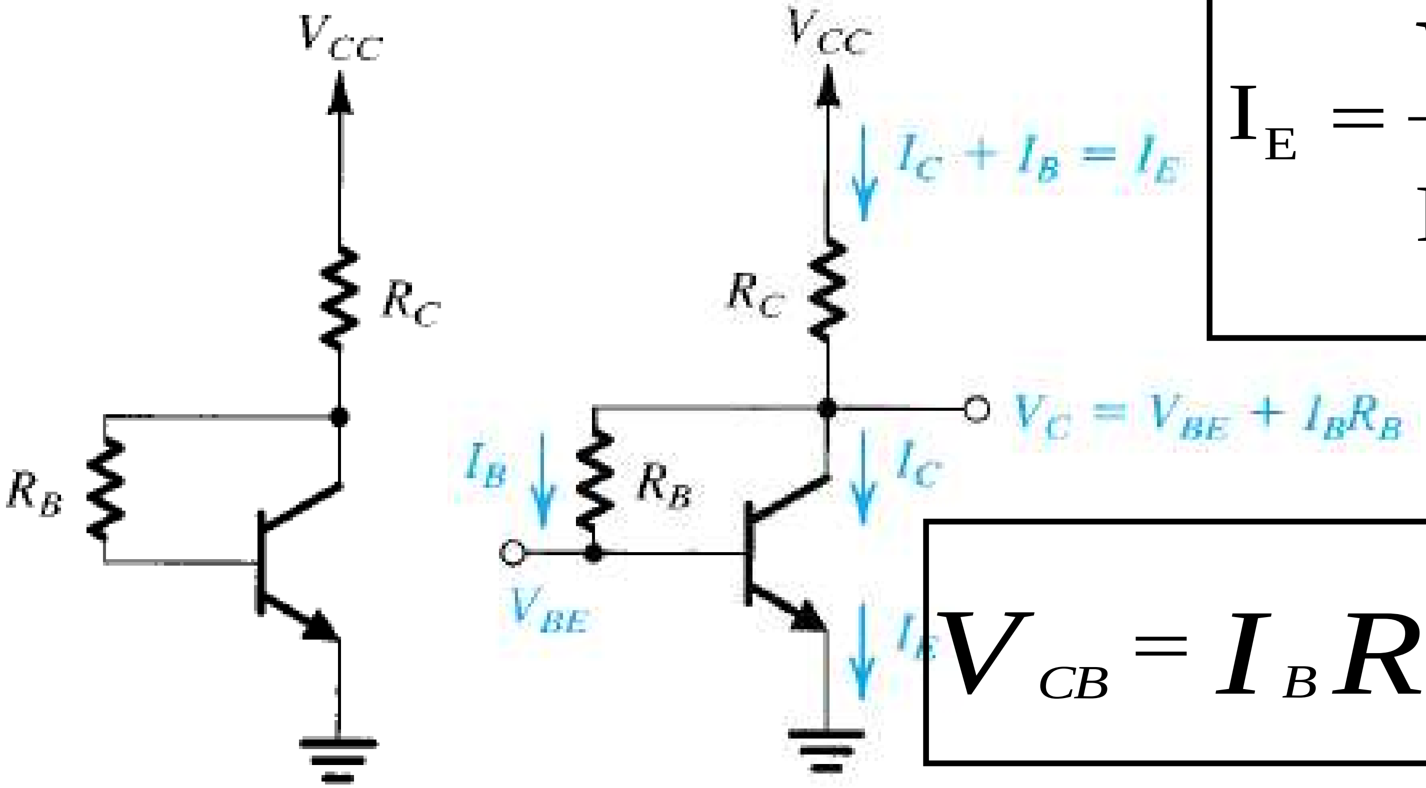


$$\mathrm{V_{CC}} = I_E \mathrm{R_C} + I_B \mathrm{R_B} + V_{BE}$$

$$\mathrm{V_{CC}} = I_E \mathrm{R_C} + \frac{I_E}{\beta + 1} \mathrm{R_B} + V_{BE}$$

(a) A CE transistor amplifier biased by a feedback resistor ***RB.***
(b) Analysis of the circuit in **(a).**

Biasing Using a Collector-to-Base Feedback Resistor



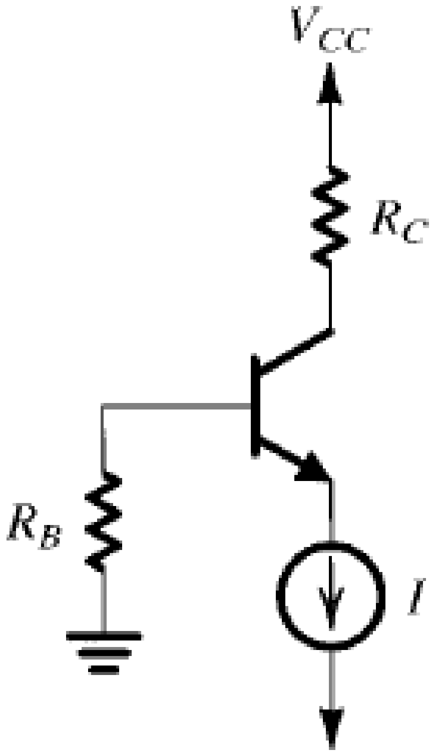
(a) (b)

$$\mathrm{I_E} = \frac{V_{CC} - V_{BE}}{\mathrm{R_{CE}} + \frac{\mathrm{R_B}}{\beta + 1}}$$

$$V_{CB} = I_B R_B = I_E \frac{R_B}{\beta + 1}$$

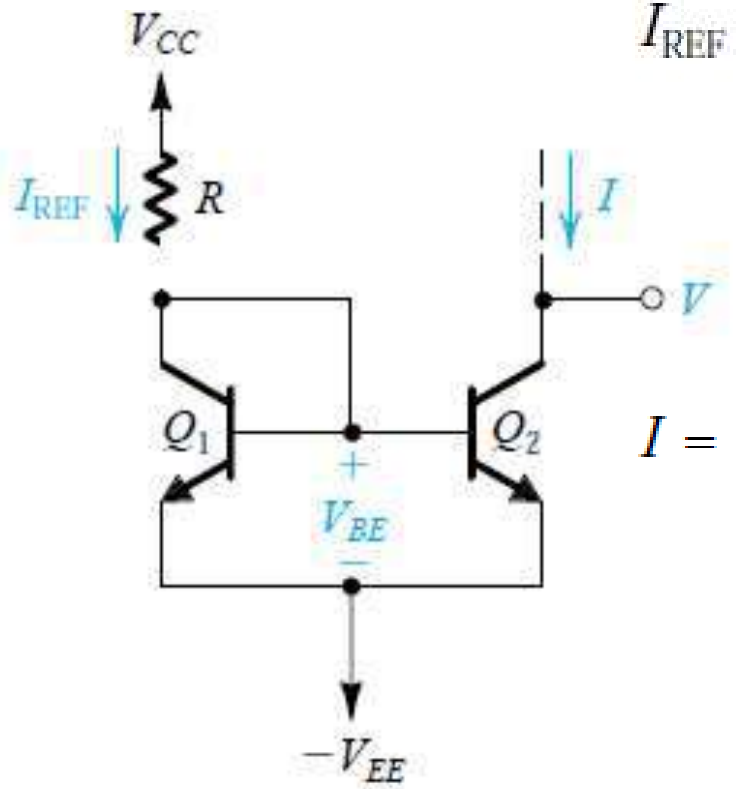
(a) A CE transistor amplifier biased by a feedback resistor *RB.*
(b) Analysis of the circuit in **(a).**

Biasing Using a Constant-Current Source



(a)

Current Mirror

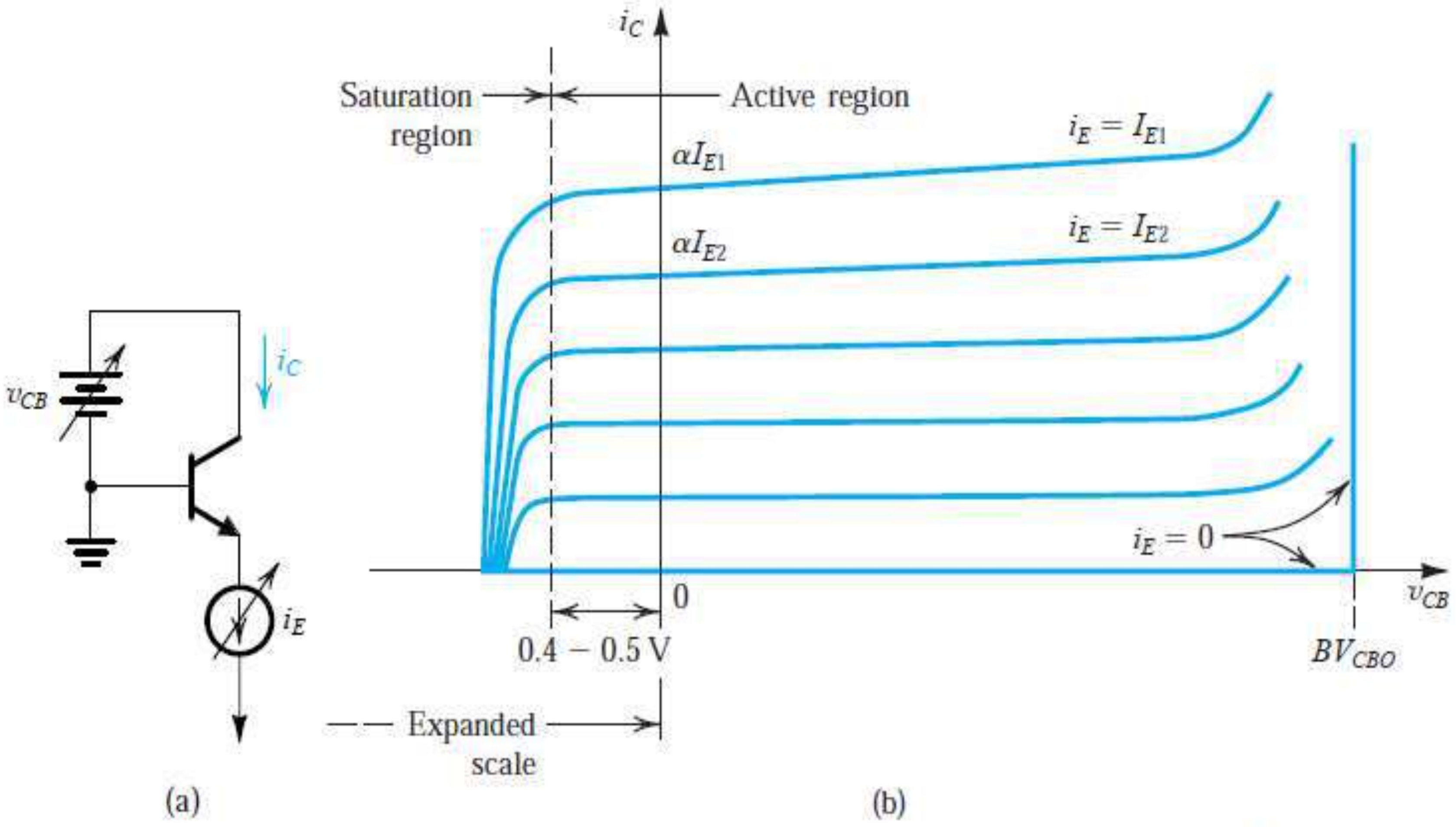


(b)

$$I_{REF} = \frac{V_{CC} - (-V_{EE}) - V_{BE}}{R}$$

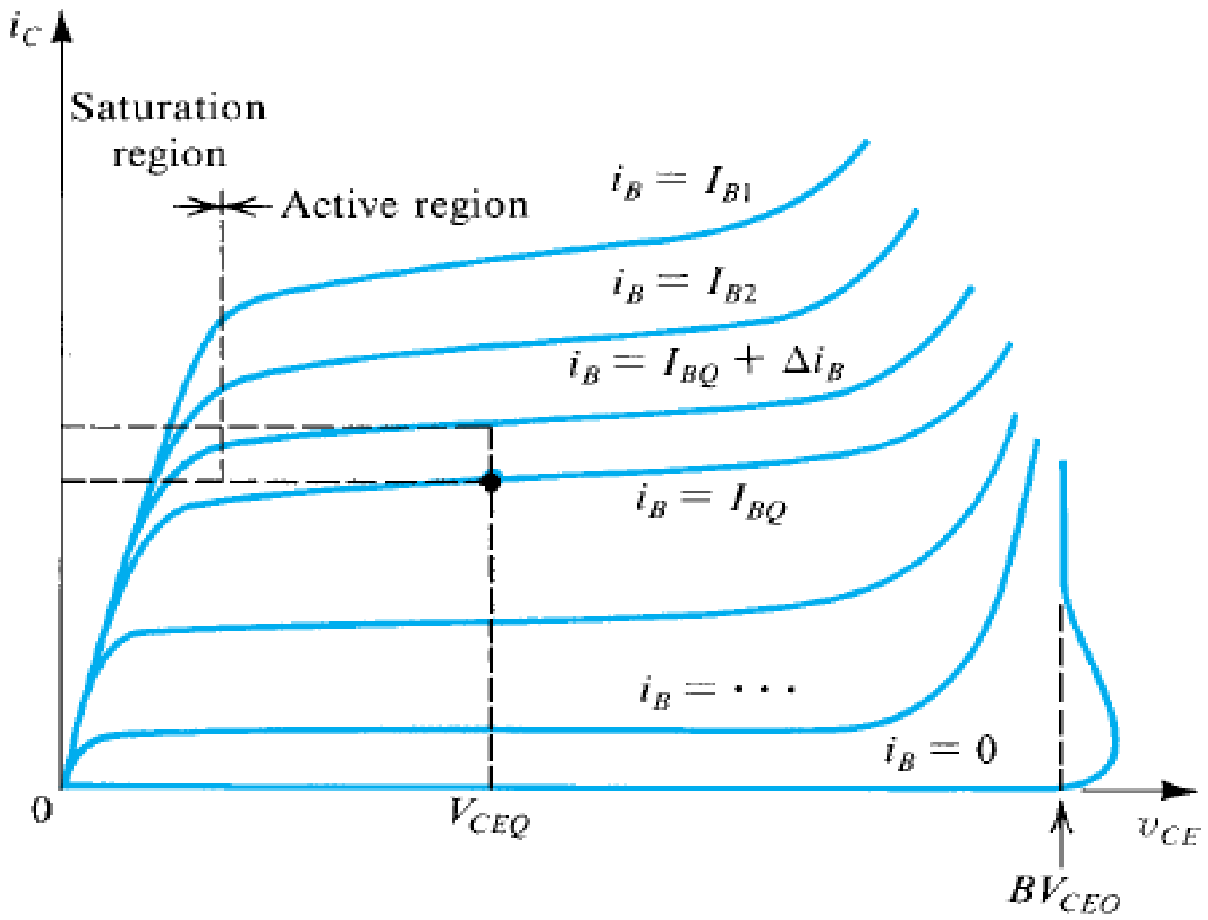
$$I = I_{REF} = \frac{V_{CC} + V_{EE} - V_{BE}}{R}$$

Transistor Breakdown and Temperature Effects



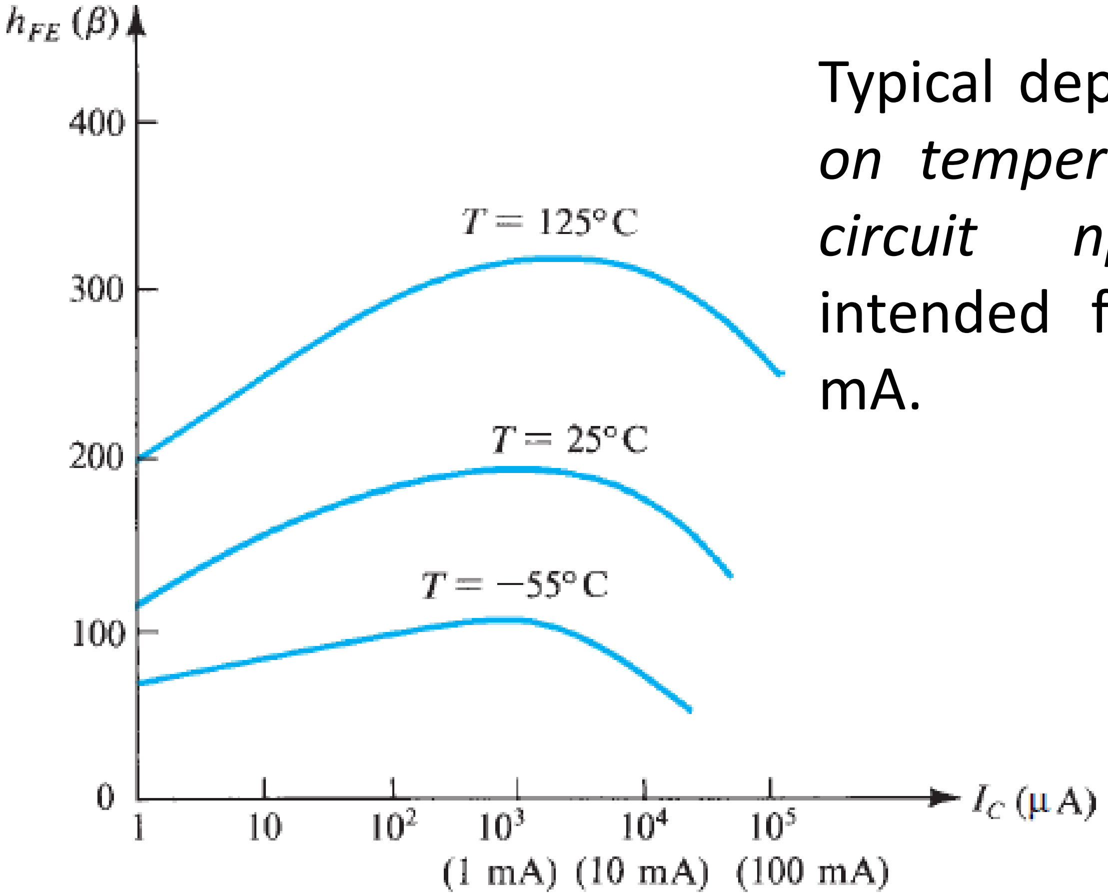
The BJT common-base characteristics including the transistor breakdown region.

Transistor Breakdown and Temperature Effects



The BJT common-emitter characteristics including the breakdown region.

Transistor Breakdown and Temperature Effects



Typical dependence of β on *IC and on temperature in an integrated-circuit npn silcon transistor* intended for operation around 1 mA.

(20A04101T) ELECTRONIC DEVICES & CIRCUITS

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Unit- 4

- MOS Field-Effect Transistors (MOSFETs):
- Introduction
- Device Structure and Physical Operation
  - Device Structure
  - Operation with Zero Gate Voltage
  - Creating a Channel for Current Flow
  - Operation for Different Drain to Source Voltages(Vds)
- The P-channel MOSFET
- CMOS
- V-I Characteristics
  - iD – vDS Characteristics
  - iD – vGS Characteristics
  - Finite Output Resistance in Saturation
  - Characteristics of the p- Channel MOSFET

- MOSFET Circuits at DC
- Applying the MOSFET in Amplifier Design
  - Voltage Transfer Characteristics
  - Biasing the MOSFET to Obtain Linear Amplification
  - The Small Signal Voltage Gain
  - Graphical Analysis
  - The Q-point
- Problem solving.

Introduction

- Compared to BJTs, MOSFETs can be made quite small (i.e., requiring a small area on the silicon IC chip), and their manufacturing process is relatively simple .
- Also, their operation requires comparatively little power.
- To pack large numbers of MOSFETs (as many as 2 billion) on a single IC chip to implement very sophisticated, very-large-scale-integrated (VLSI) digital circuits such as those for memory and microprocessors.

Historical Background

- Evolution of IC Technology

Year	Technology	Number of components	Typical products
1947	Invention of transistor	1	–
1950–1960	Discrete components	1	Junction diodes and transistors
1961–1965	Small-scale integration	10–100	Planner devices, logic gates, flip-flops
1966–1970	Medium-scale integration	100–1000	Counters, MUXs, decoders, adders
1971–1979	Large-scale integration	1000–20,000	8-bit μp, RAM, ROM
1980–1984	Very-large-scale integration	20,000–50,000	DSPs, RISC processors, 16-bit, 32-bit μP
1985–	Ultra-large-scale integration	>50,000	64-bit μp, dual-core μP

MUX multiplexer, *μP* microprocessor, *RAM* random-access memory, *ROM* read-only memory, *DSP* digital signal processor, *RISC* reduced instruction set computer

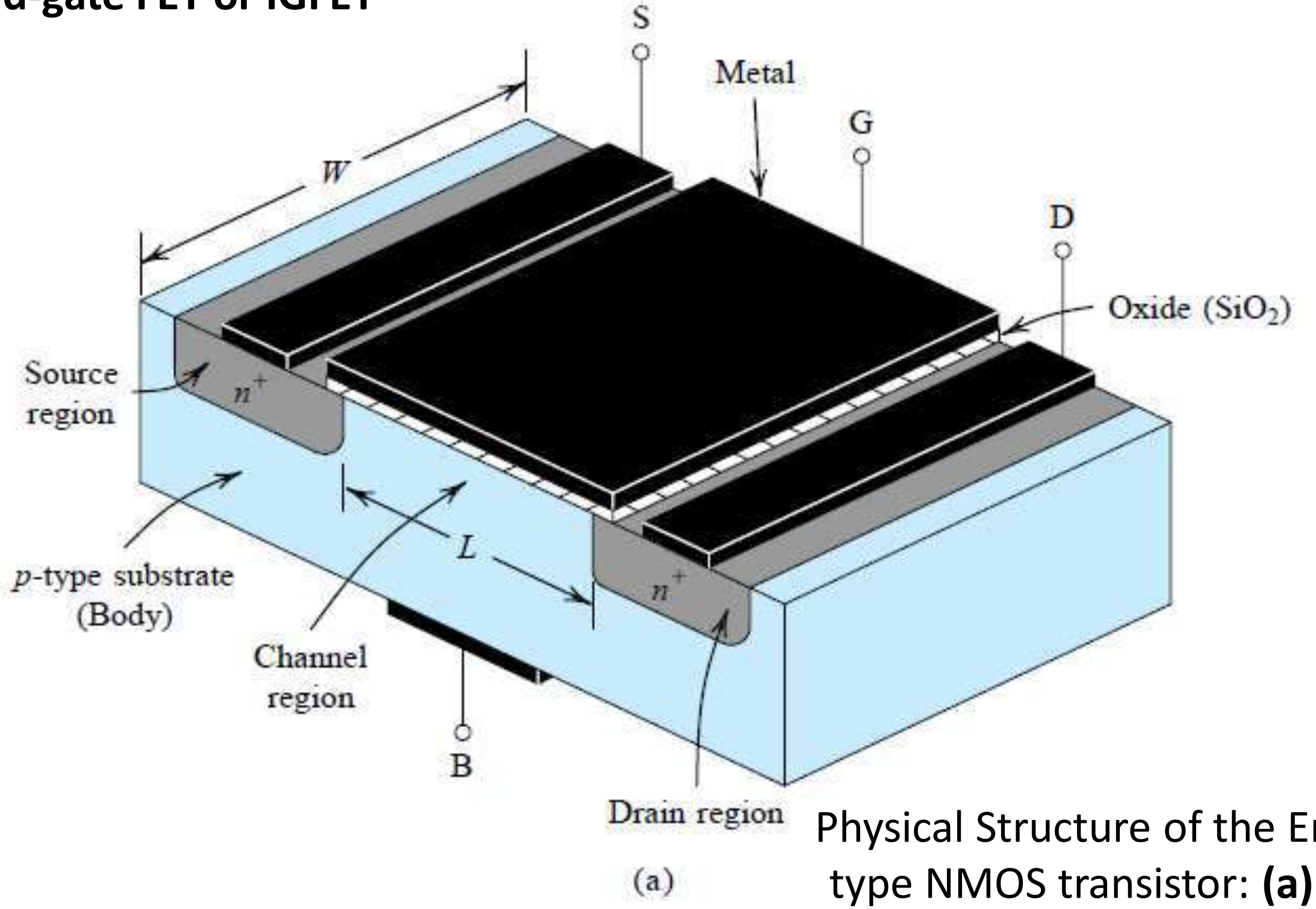
Introduction

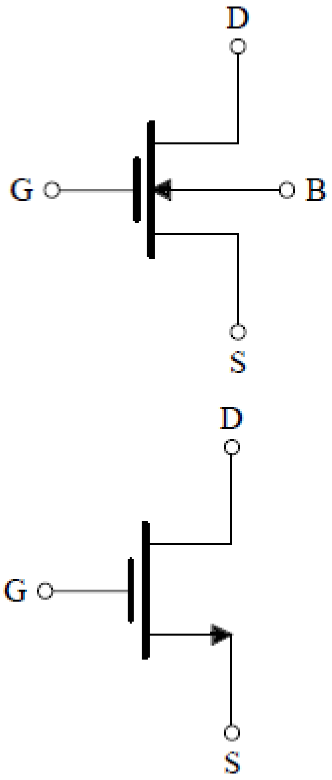
- Analog circuits such as amplifiers and filters can also be implemented in MOS technology, albeit in smaller, less-dense chips.
- Also, both analog and digital functions are increasingly being implemented on the same IC chip, in what is known as mixed-signal design.

Device Structure and Physical Operation-

Device Structure

Insulated-gate FET or IGFET

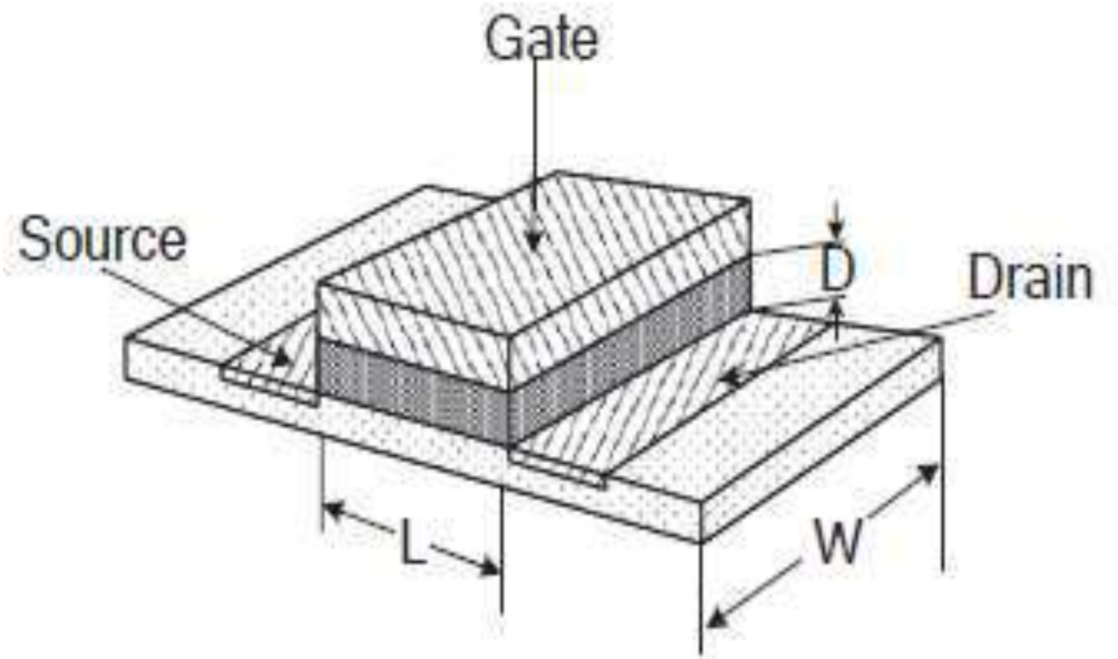


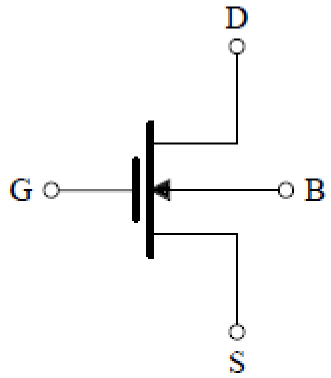


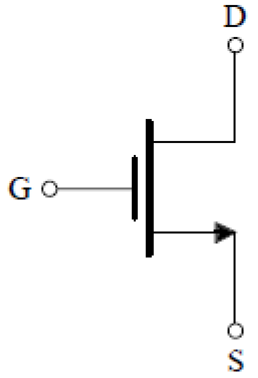
Physical Structure of the Enhancement-type NMOS transistor: **(a) perspective view;**

Device Structure and Physical Operation-

Device Structure



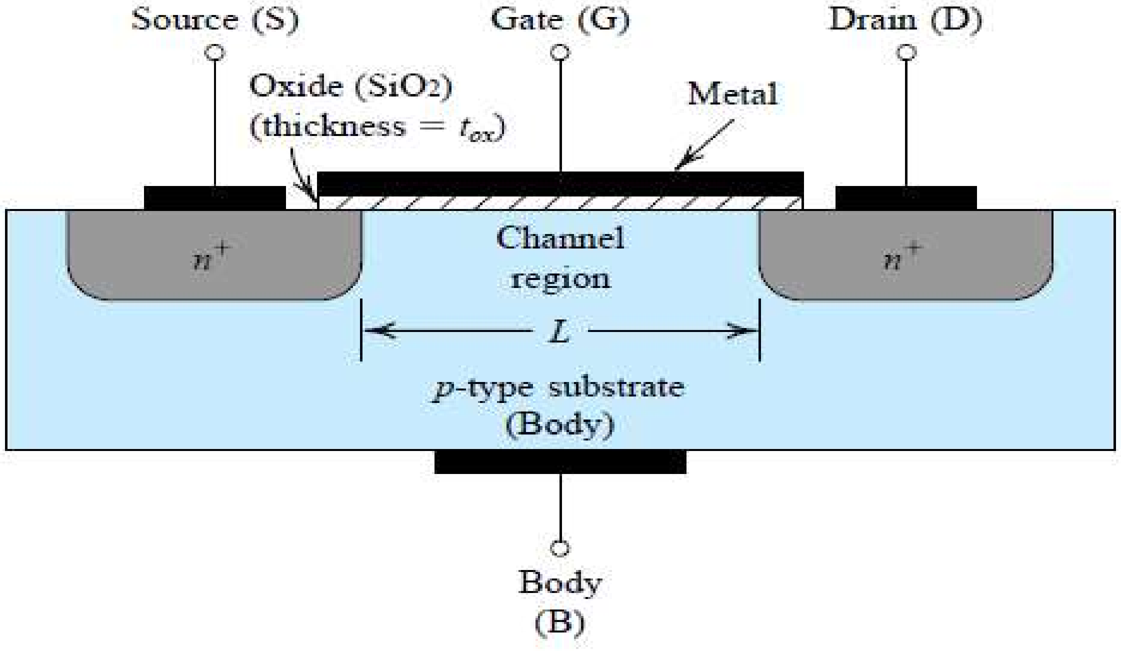




Physical Structure of the Enhancement-type NMOS transistor: **(a) perspective view;**

Device Structure and Physical Operation-

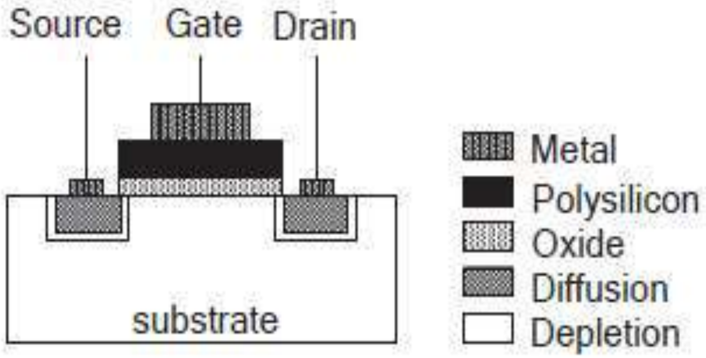
Device Structure

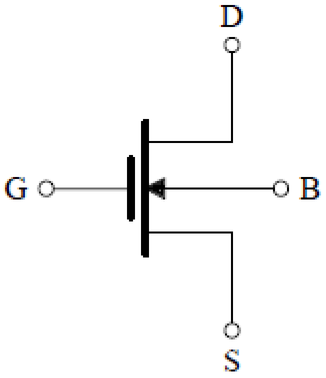


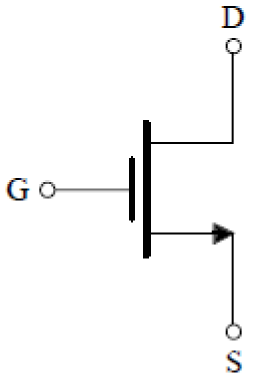
(b)

(b) Cross Section.

Typically *L = 0.03 µm to 1 µm, W = 0.1 µm to 100 µm, and the thickness of the oxide layer (tox) is in the* range of 1 to 10 nm.

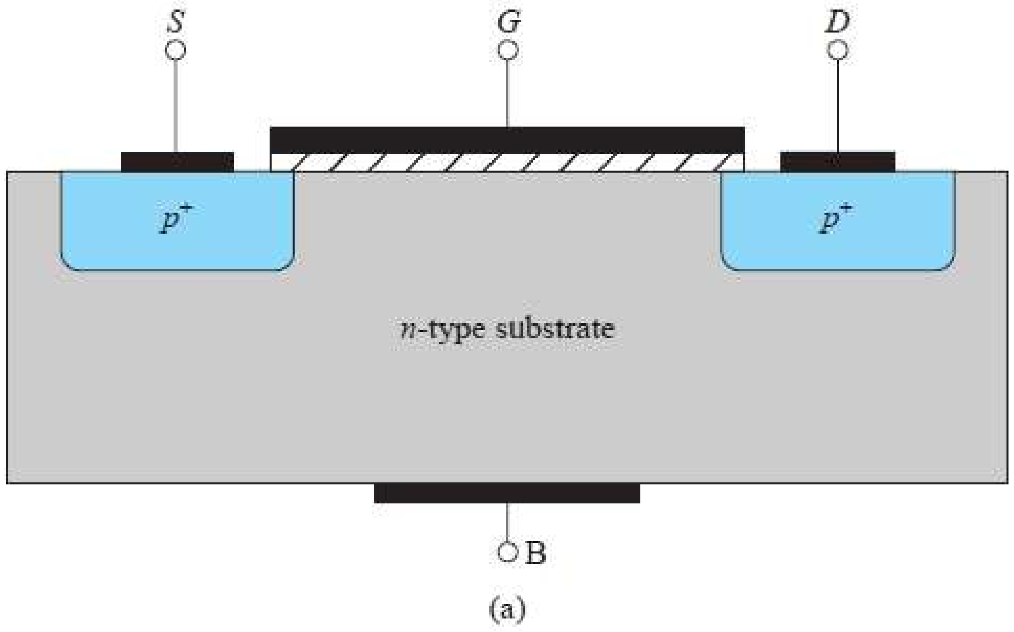




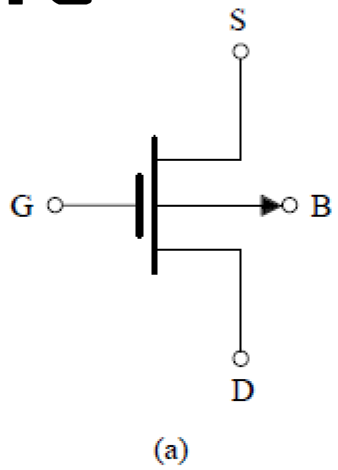


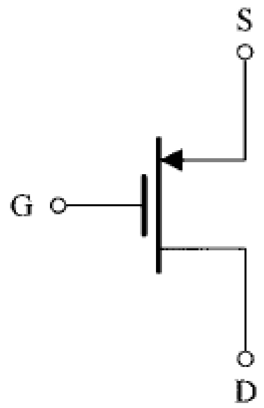
Device Structure and Physical Operation-

Device Structure



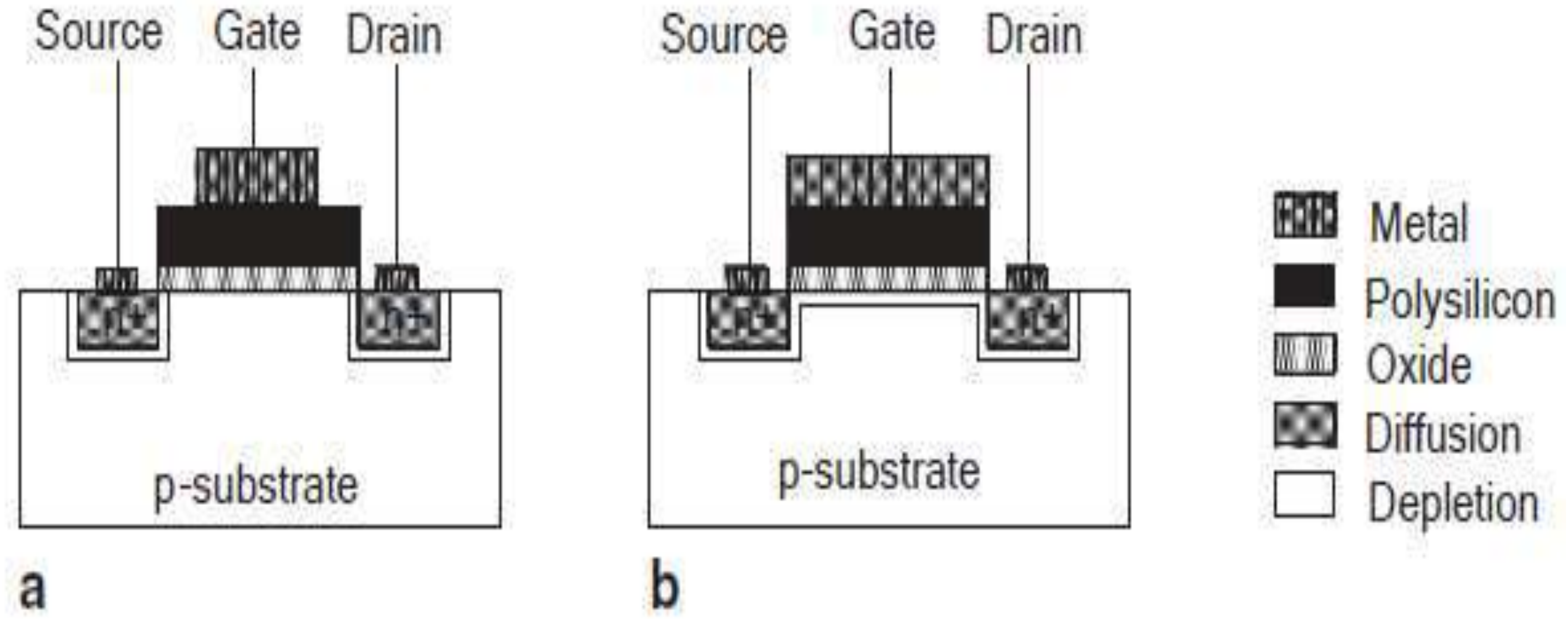
(a) Physical structure of the PMOS transistor





Device Structure and Physical Operation-

Device Structure



(a) nMOS enhancement-mode transistor
(b) nMOS depletion-mode transistor

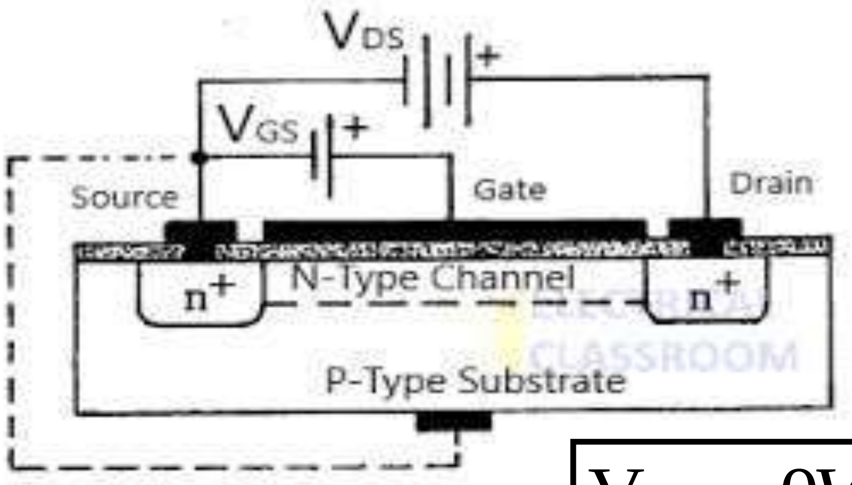
Device Structure and Physical Operation- **Operation with Zero Gate Voltage**

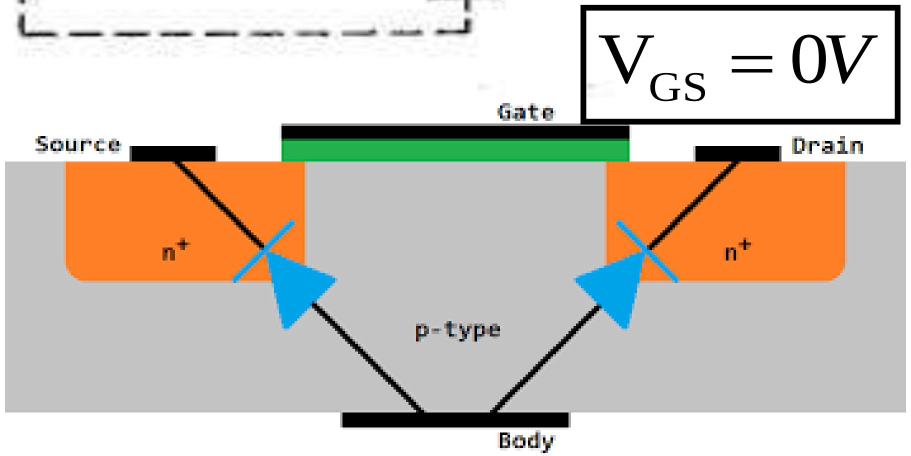
❖With zero voltage applied to the gate, two back-to-back diodes exist in series between drain and source.

❖One diode is formed by the *pn junction between the n+ drain region and the ptype* substrate, and the other diode is formed by the *pn junction between the p-type substrate* and the *n+ source region.*

❖*These back-to-back diodes prevent current conduction from drain* to source when a voltage *vDS is applied.*

❖ *In fact, the path between drain and source has a very* high resistance (of the order of 10^12 Ω).

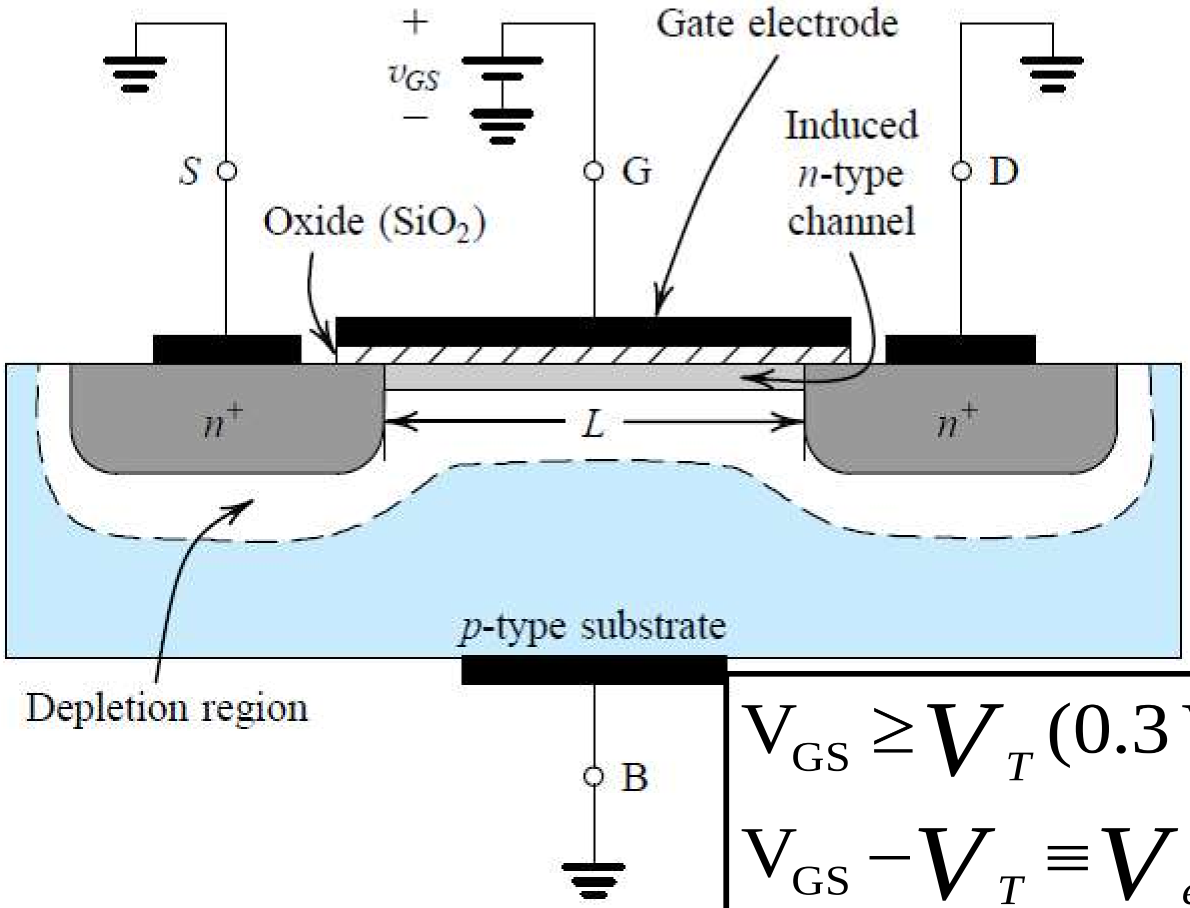




Device Structure and Physical Operation-
Creating a Channel for Current Flow

$$Q = CV$$

$$C = \frac{\varepsilon A}{D}$$



- ❖The enhancement-type NMOS transistor with a positive voltage applied to the gate.
- ❖An *n channel is induced at the top of the substrate beneath the gate.*

$$V_{GS} \geq V_T \,(0.3\,\text{V to}\,1.0\,\text{V})$$

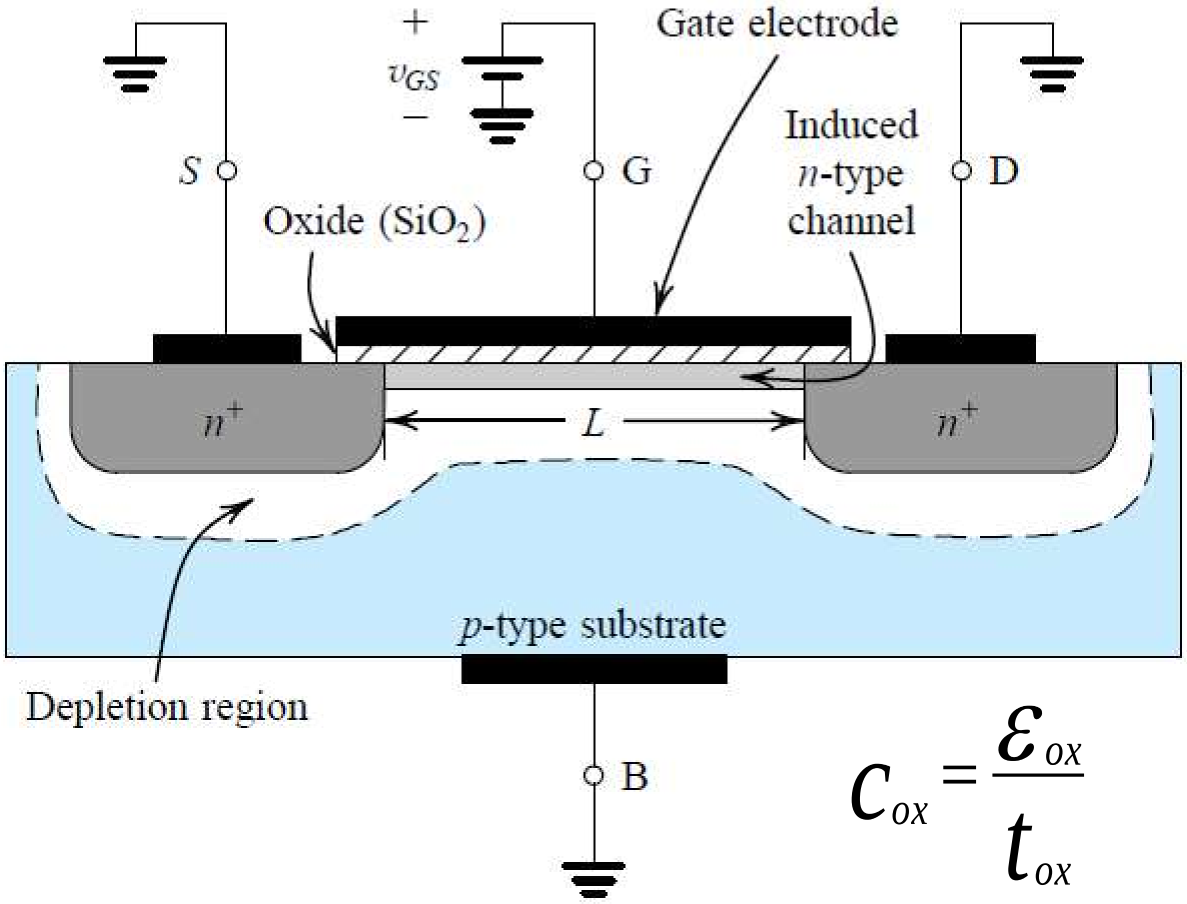
$$V_{GS} - V_T \equiv V_{eff}$$

Device Structure and Physical Operation-
Creating a Channel for Current Flow

$$Q = CV$$

$$C = \frac{\varepsilon A}{D}$$

$$C = \frac{\varepsilon A}{D}$$



$$Q = CV_{eff}$$

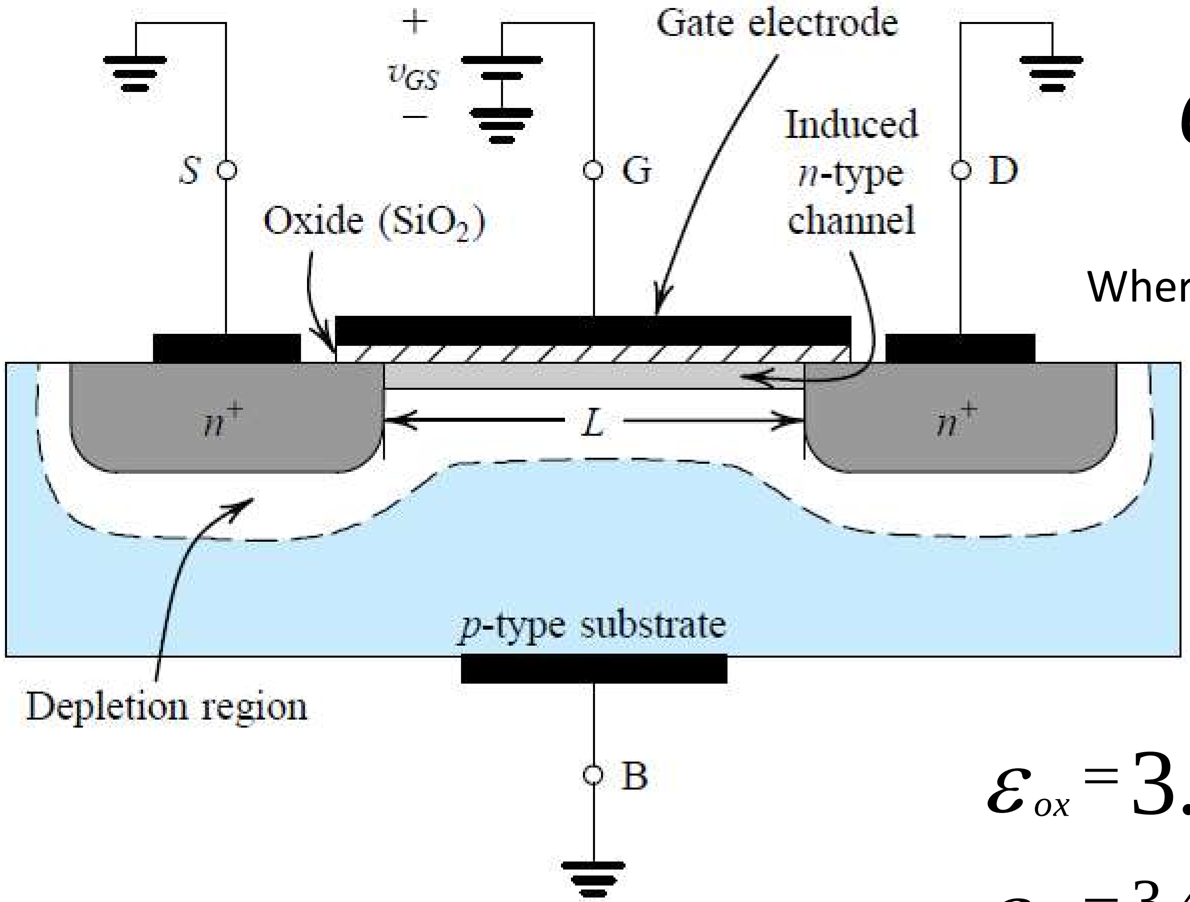
$$C = \frac{\varepsilon_{ox} WL}{t_{ox}}$$

$$Q = \frac{\varepsilon_{ox} WL}{t_{ox}} V_{eff}$$

$$Q = c_{oc} WL V_{eff}$$

$$c_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Device Structure and Physical Operation- **Creating a Channel for Current Flow**



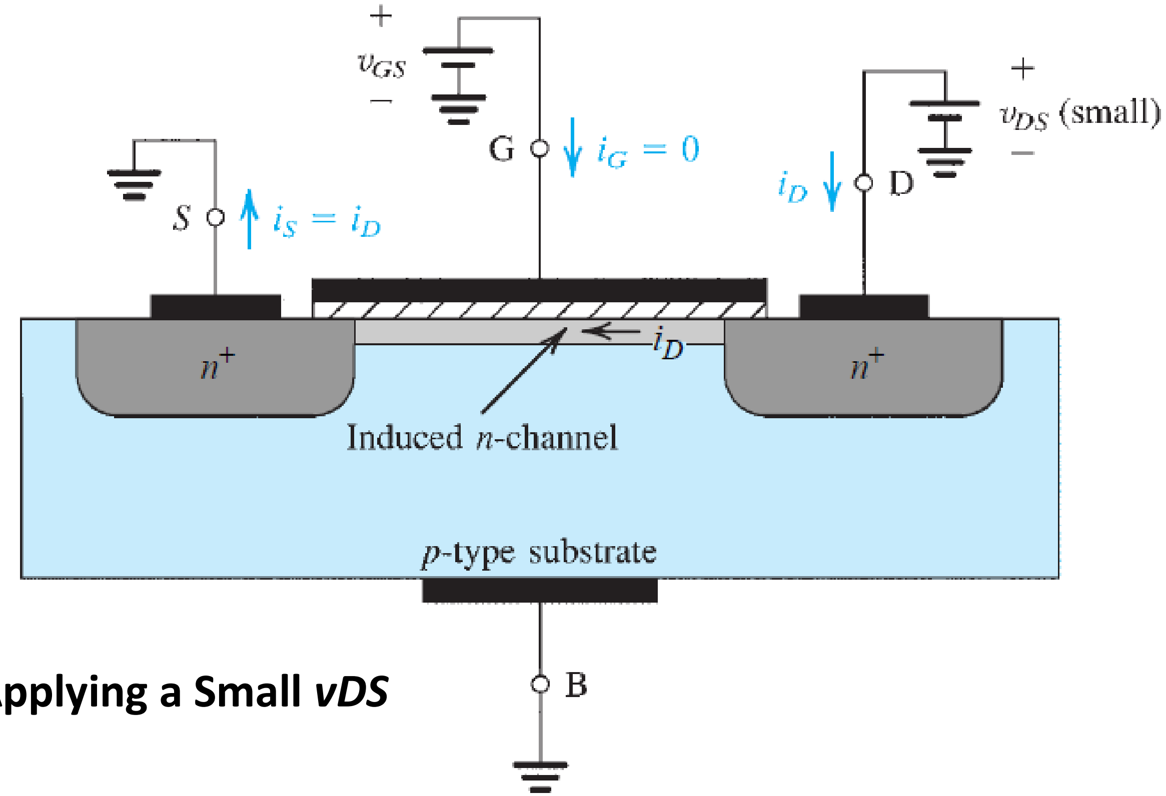
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Where ε_{ox} is the permittivity of the silicon dioxide,

$$\varepsilon_{ox} = 3.9 \times \varepsilon_o = \varepsilon_o \times 8.854 \times 10^{-12}$$

$$\varepsilon_{ox} = 3.45 \times 10^{-11} F/m$$

Device Structure and Physical Operation-
Creating a Channel for Current Flow



Applying a Small *vDS*

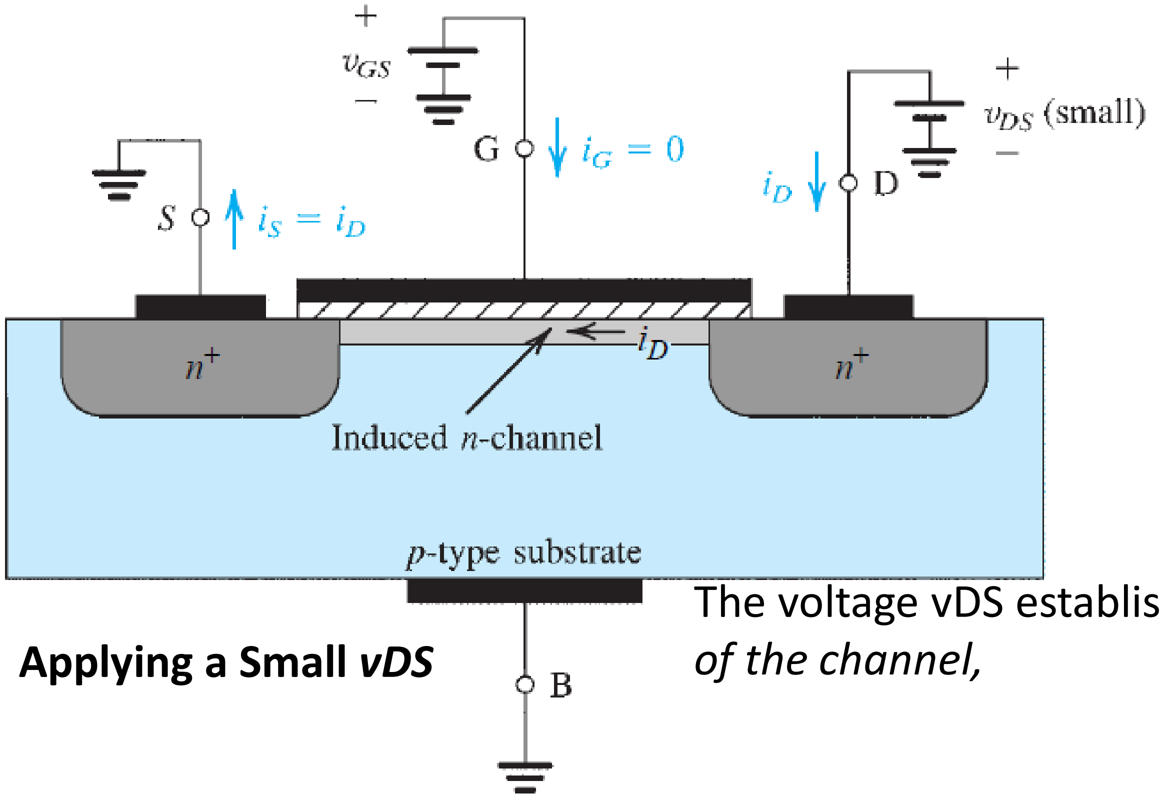
❖An NMOS transistor with *vGS > Vt and with a small vDS applied.*

❖*The device acts as a resistance* whose value is determined by *vGS.*

❖*Specifically, the channel conductance is proportional to vGS − Vt, and thus iD* is proportional to (*vGS − Vt)vDS.*

❖*Note that the depletion region is not shown (for simplicity).*

Device Structure and Physical Operation-
Creating a Channel for Current Flow



Applying a Small *vDS*

iD,current is the charge per unit channel length

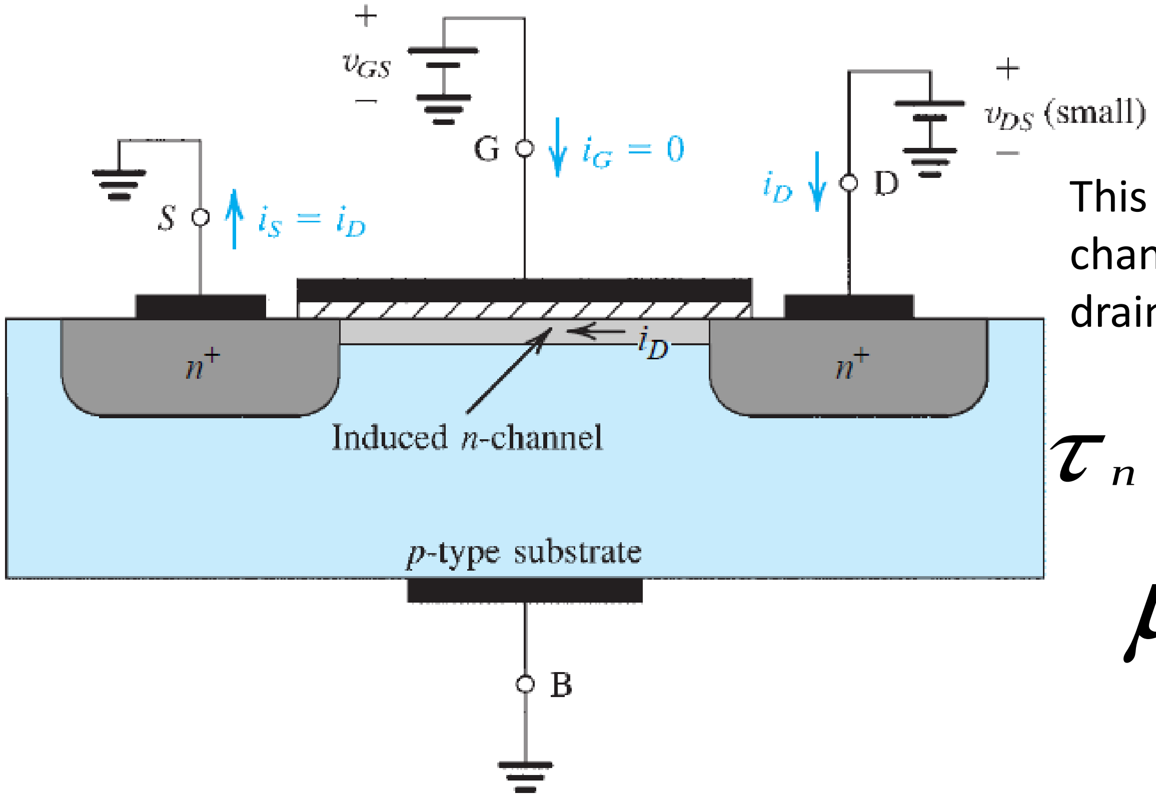
$$Q = C_{ox} WL V_{eff}$$

$$\frac{Q}{L} = C_{ox} W V_{eff}$$

The voltage vDS establishes an electric field *E across the length of the channel,*

$$E = \frac{V_{DS}}{L}$$

Device Structure and Physical Operation-
Creating a Channel for Current Flow



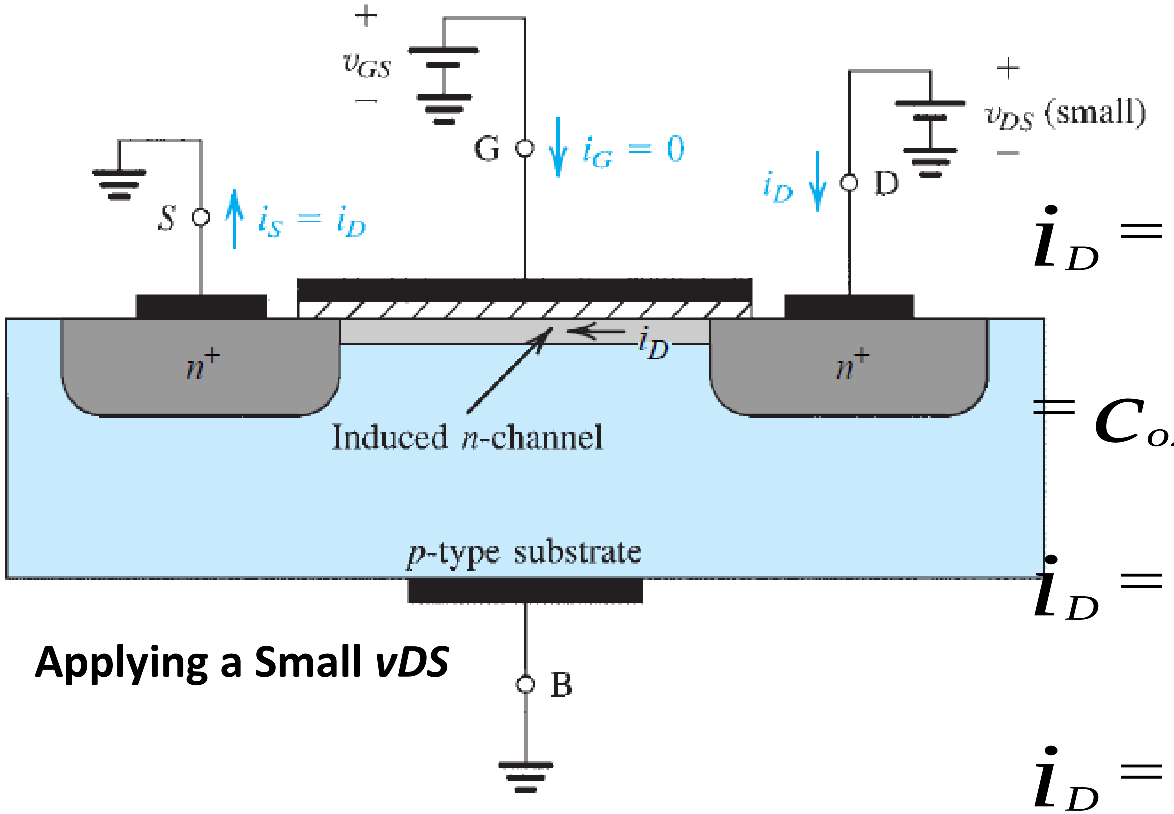
Applying a Small *vDS*

This electric field in turn causes the channel electrons to drift toward the drain with a velocity given by

$$\tau_n = \mu_n E = \mu_n \frac{v_{DS}}{L}$$

$$\mu_n - mobility$$

Device Structure and Physical Operation-
Creating a Channel for Current Flow



Applying a Small *vDS*

The value of iD can now be found by multiplying the charge per unit channel length by the electron drift velocity

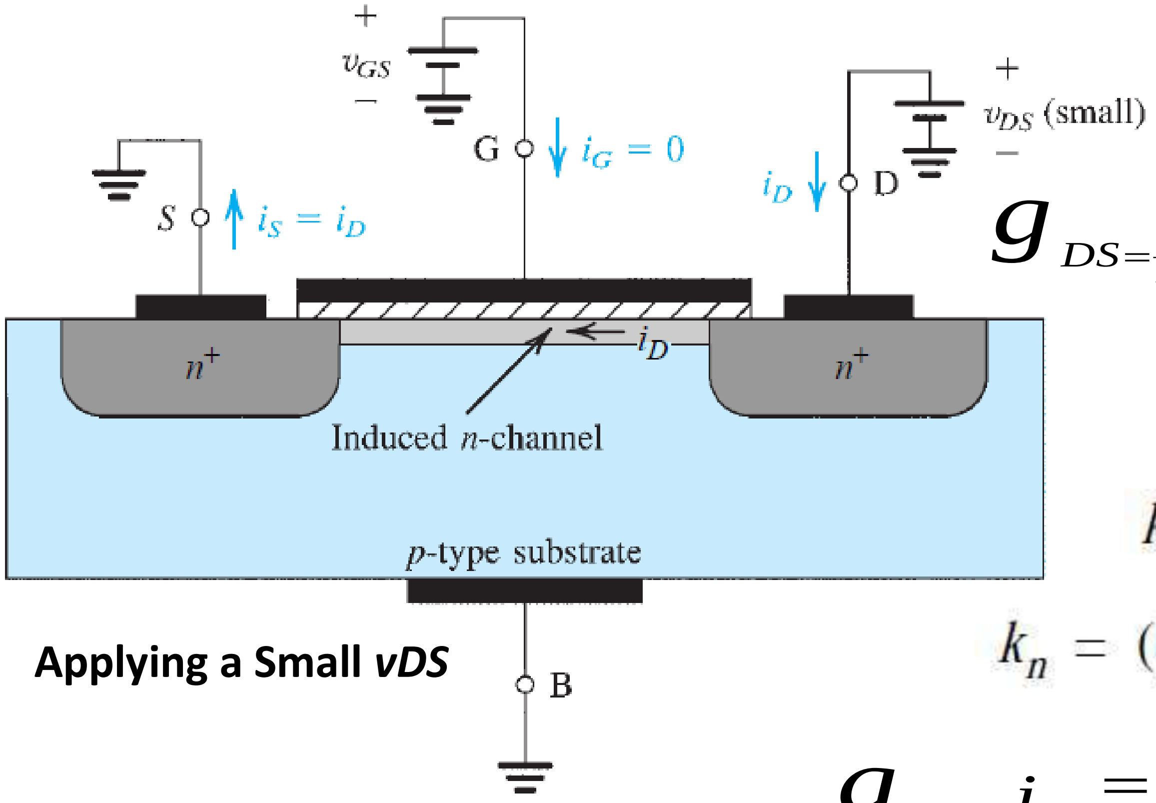
$$i_D = \frac{Q}{L}\tau_n$$

$$= C_{ox} W V_{eff} \times \mu_n \frac{v_{DS}}{L}$$

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)V_{eff}\right]v_{DS}$$

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - v_T)\right]v_{DS}$$

Device Structure and Physical Operation-
Creating a Channel for Current Flow



Applying a Small *vDS*

The conductance of the channel

$$g_{DS} = \frac{i_D}{v_{DS}} = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - v_T)\right]$$

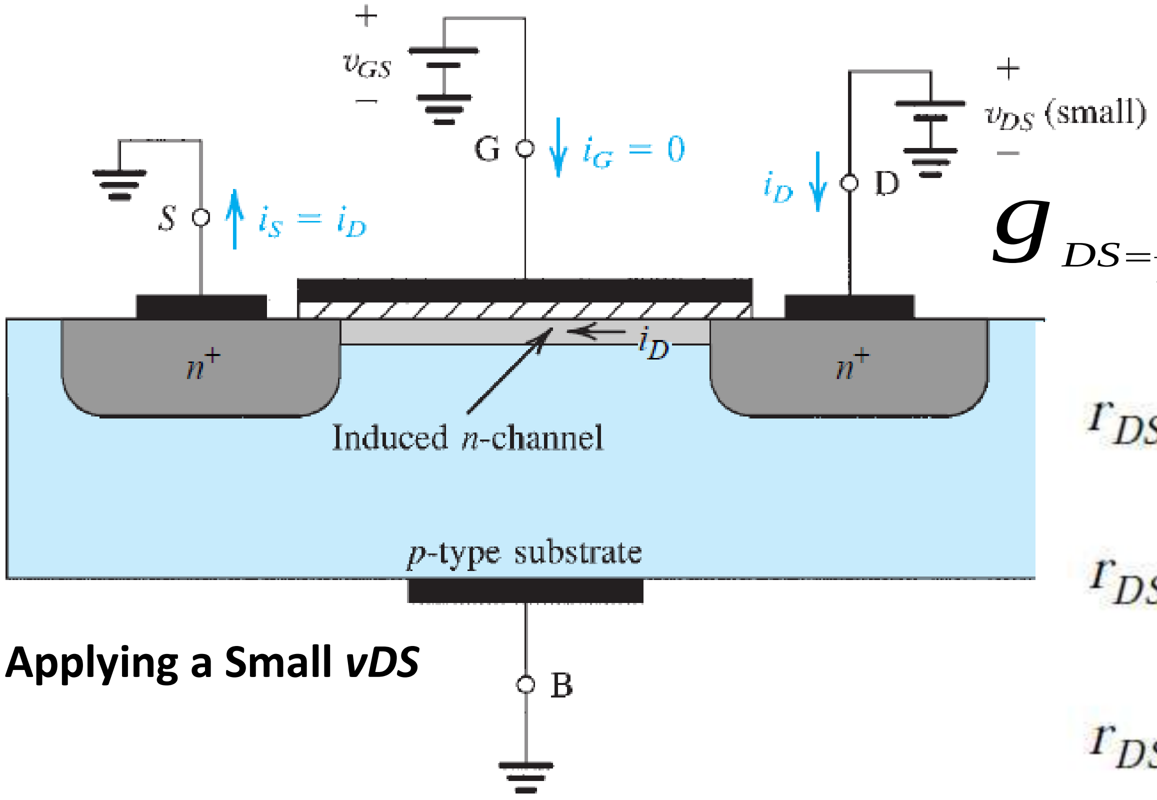
$$k_n' = \mu_n C_{ox}$$

$$k_n = k_n' (W/L)$$

$$k_n = (\mu_n C_{ox})(W/L)$$

$$g_{DS} = \frac{i_D}{v_{DS}} = [k_n(v_{GS} - v_T)] = k_n v_{eff}$$

Device Structure and Physical Operation-
Creating a Channel for Current Flow



Applying a Small *vDS*

The conductance of the channel

$$g_{DS} = \frac{i_D}{v_{DS}} = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - v_T)\right]$$

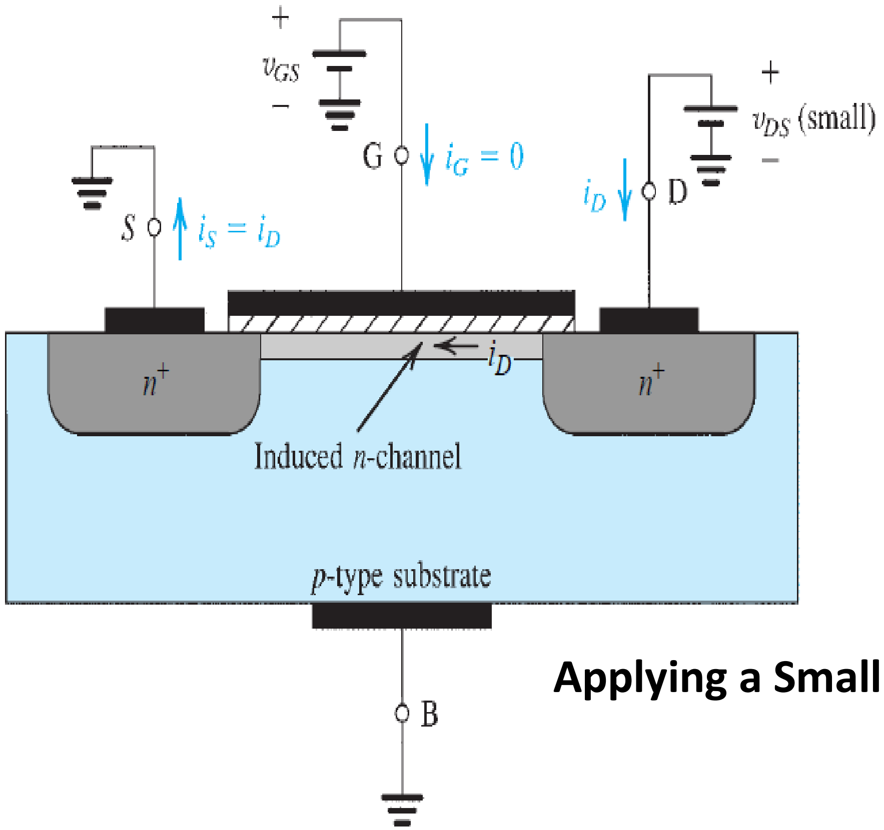
$$r_{DS} = \frac{1}{g_{DS}}$$

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)v_{OV}}$$

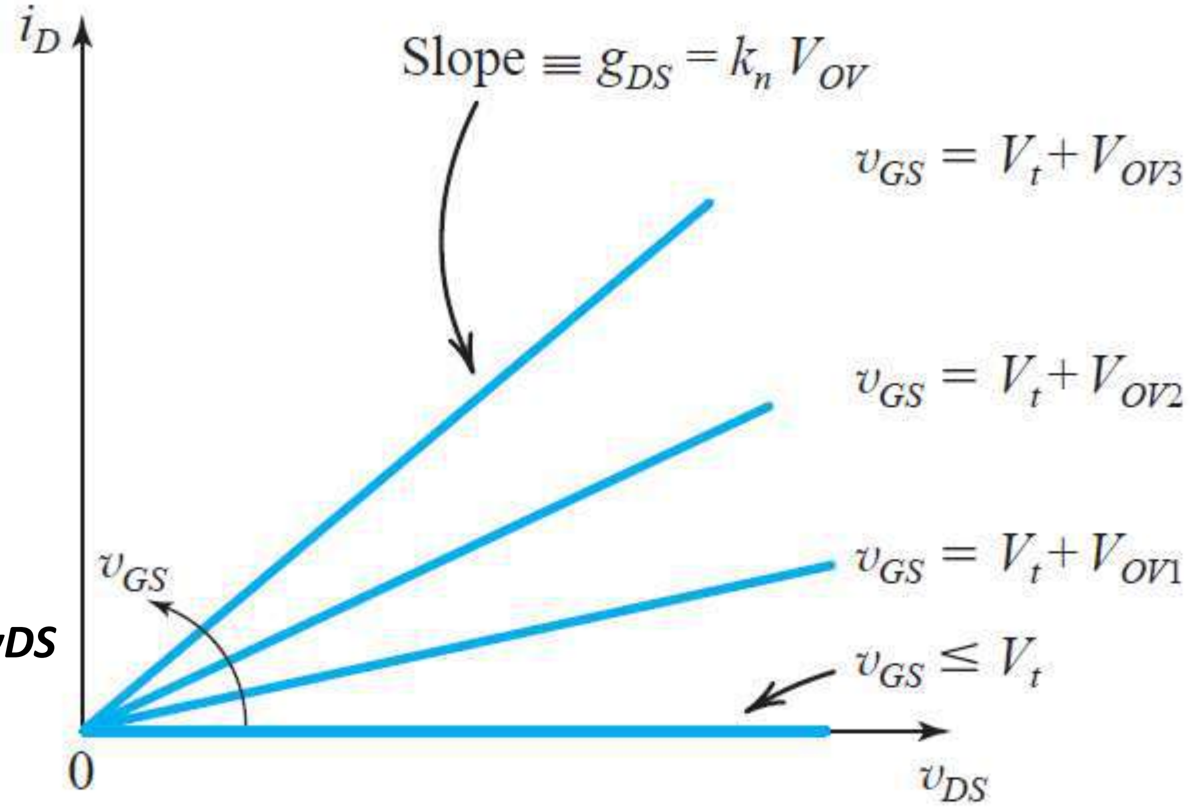
$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)(v_{GS} - V_t)}$$

Device Structure and Physical Operation-

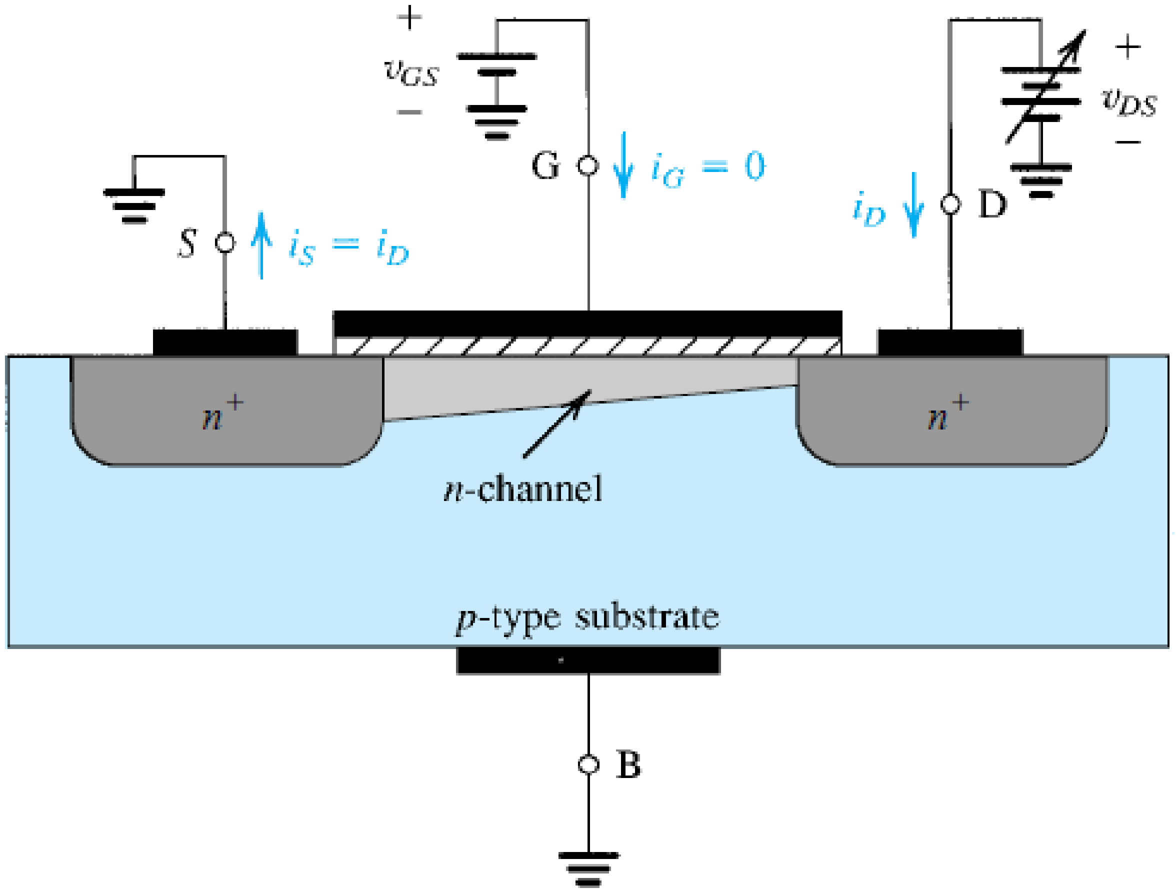
Creating a Channel for Current Flow



Applying a Small *vDS*



Device Structure and Physical Operation- **Creating a Channel for Current Flow**



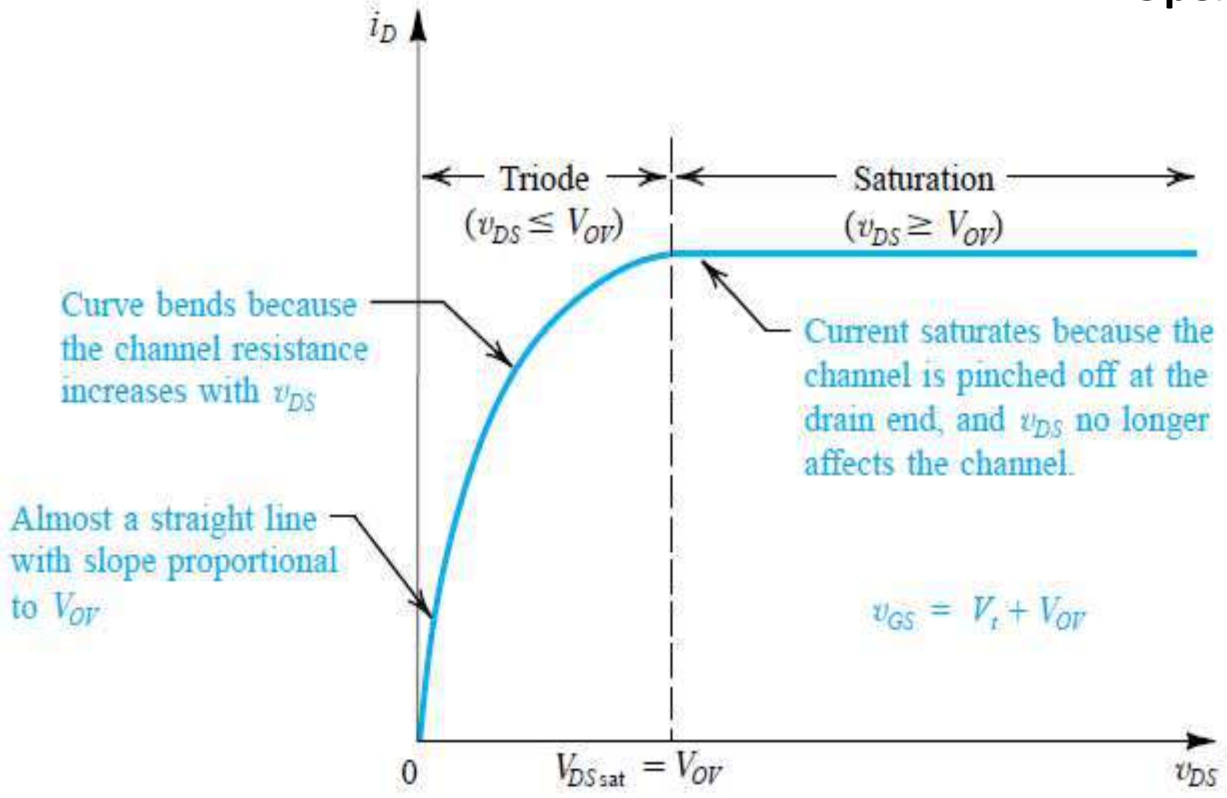
Operation as *vDS Is Increased*

Operation of the enhancement NMOS transistor as *vDS* is increased. The induced channel acquires a tapered shape, and its resistance increases as is *vDS* increased. Here, is kept constant at a value > *Vt;*

vGS = Vt + VOV

Device Structure and Physical Operation- **Creating a Channel for Current Flow**

Operation as *vDS Is Increased*



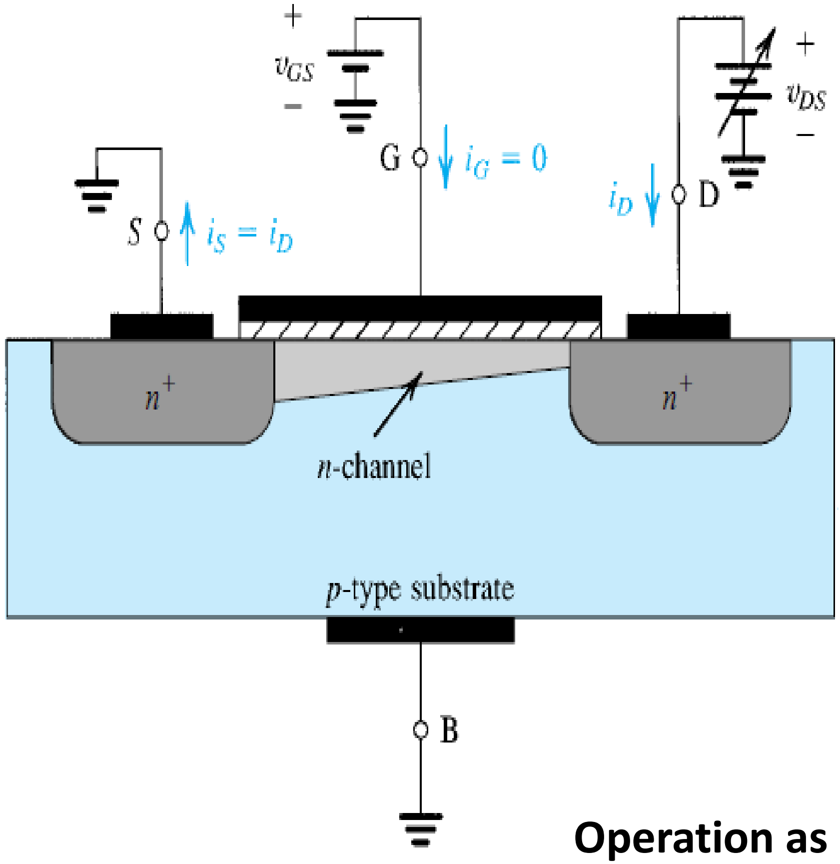
The drain current *iD versus the drain-to-source voltage vDS for an enhancement-type NMOS* transistor operated with *vGS = Vt + VOV*

.

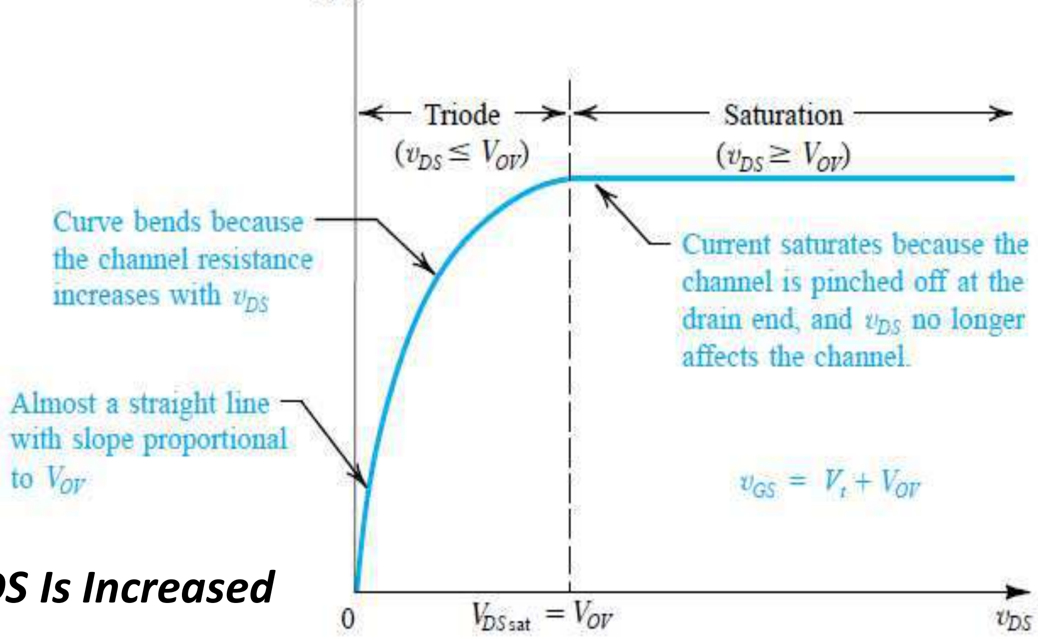
Device Structure and Physical Operation-
Creating a Channel for Current Flow

$$i_D = [k_n(v_{GS} - v_T)]v_{DS}$$

$$i_D = \left[k_n(v_{eff} - \frac{1}{2}v_{DS})\right]v_{DS}$$

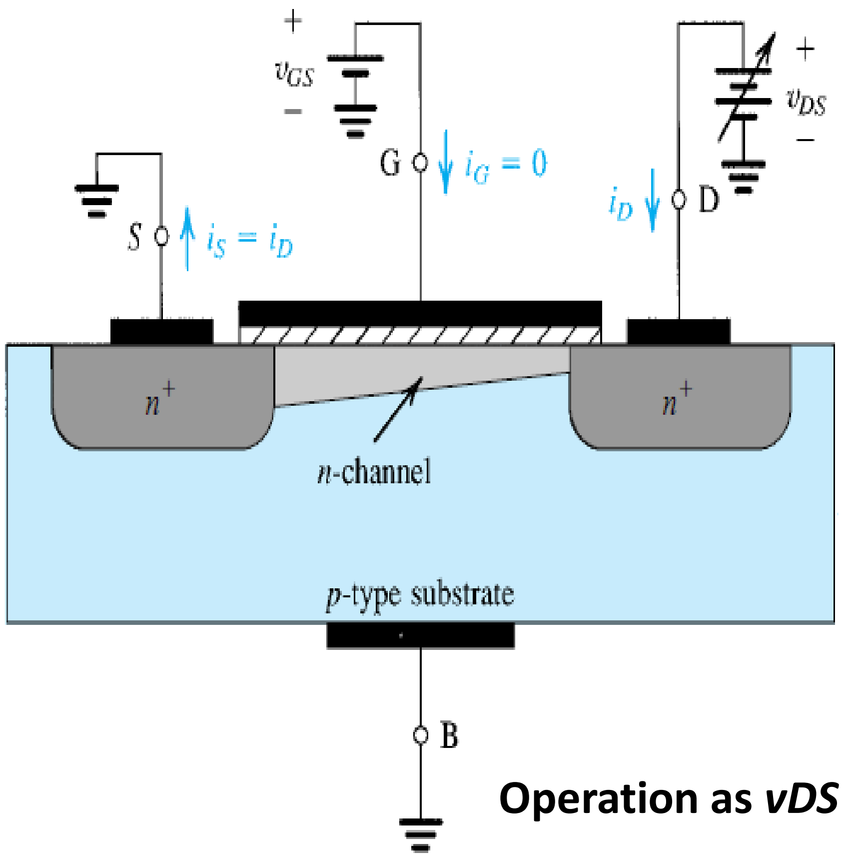


Operation as *vDS Is Increased*

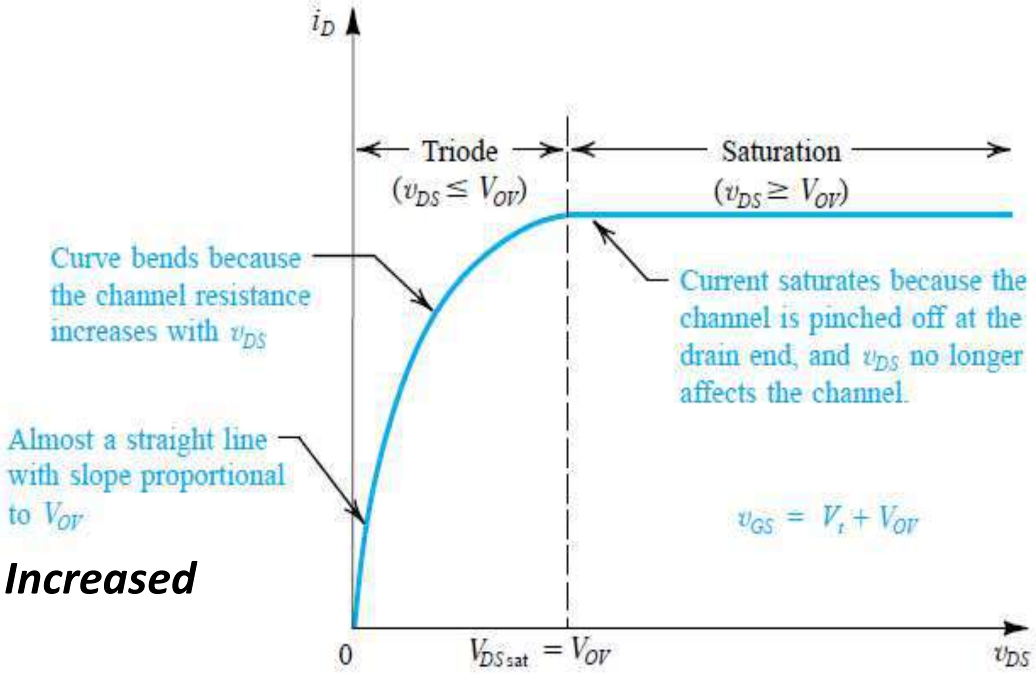


Device Structure and Physical Operation- **Creating a Channel for Current Flow**

$$i_D = \left[k_n(v_{GS} - v_T) - \frac{1}{2}v_{DS})\right]v_{DS}$$

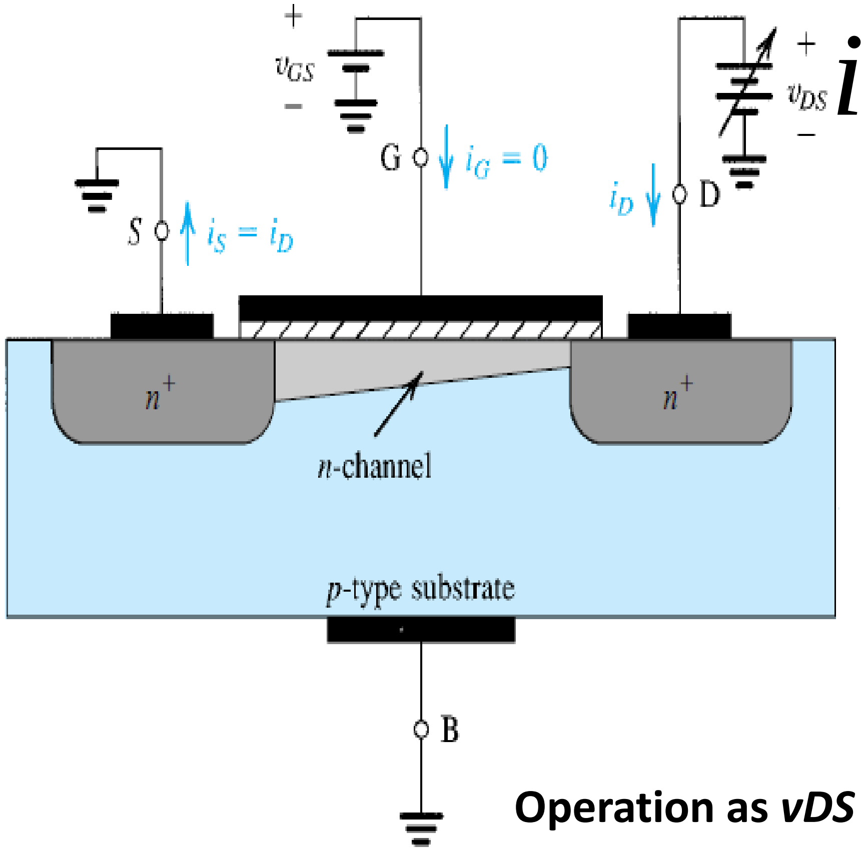


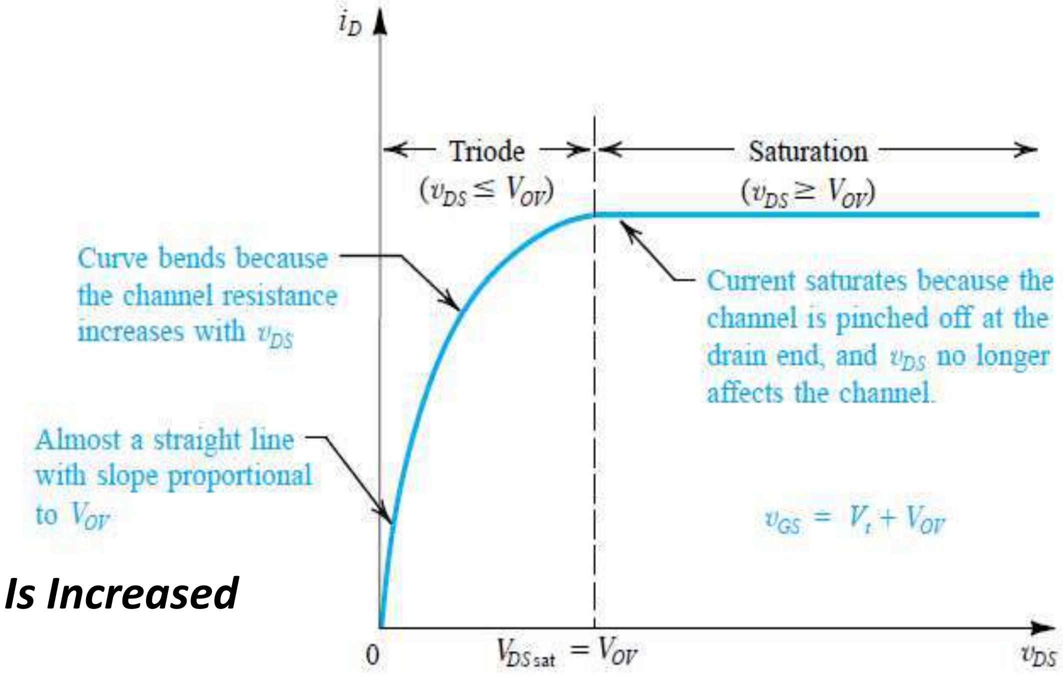
Operation as *vDS Is Increased*



Device Structure and Physical Operation- **Creating a Channel for Current Flow**

$$i_D = \left[k_n (v_{GS} - v_T) v_{DS} - \frac{1}{2} v_{DS}{}^{2}) \right]$$

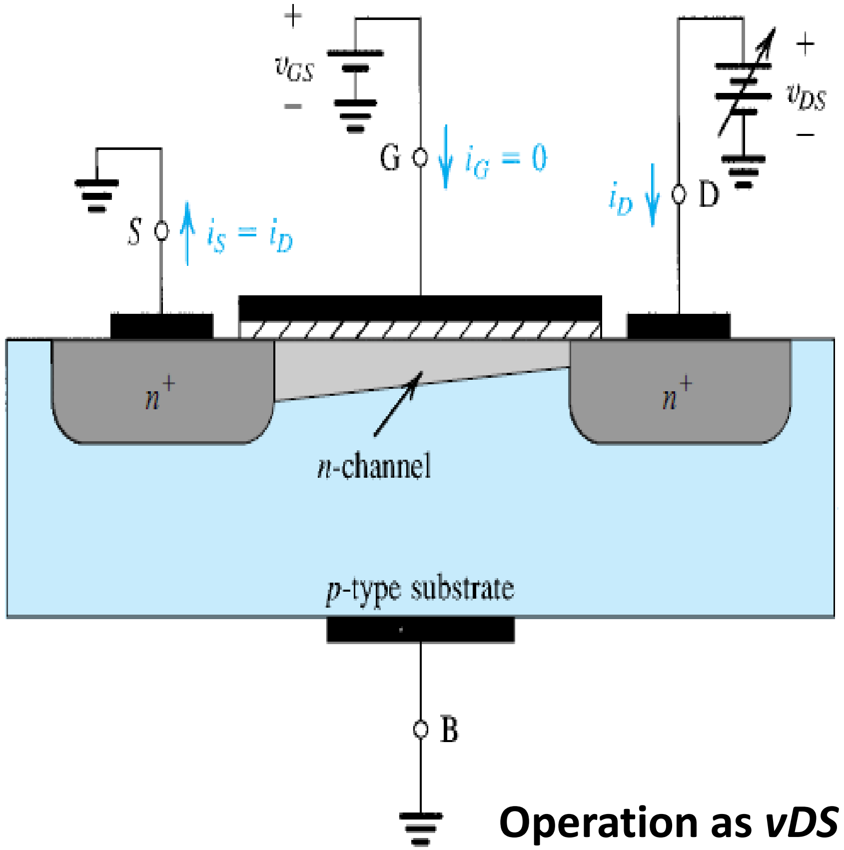




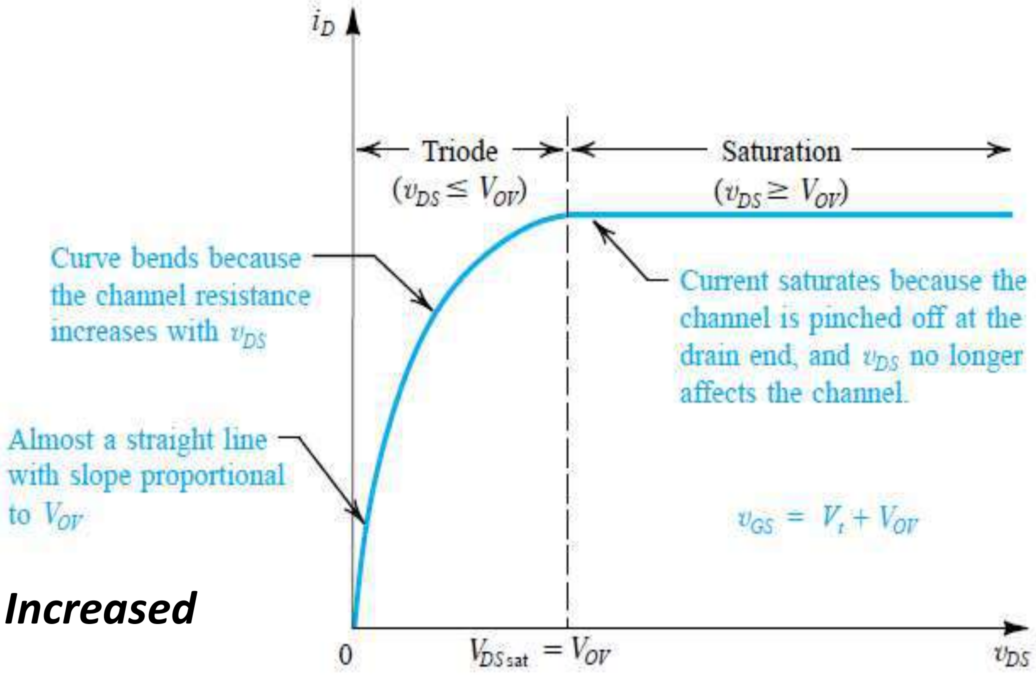
Operation as *vDS Is Increased*

Device Structure and Physical Operation- **Creating a Channel for Current Flow**

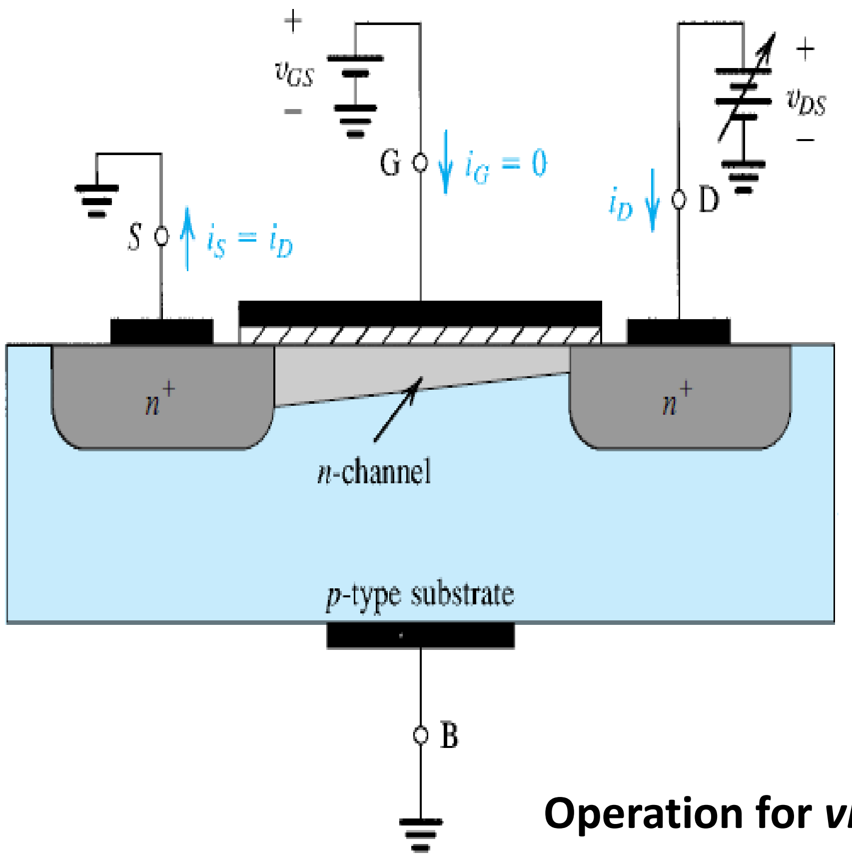
$$i_D = \left[k_n' \left(\frac{W}{L} \right) (v_{GS} - v_T) v_{DS} - \frac{1}{2} v_{DS}^{2}) \right]$$



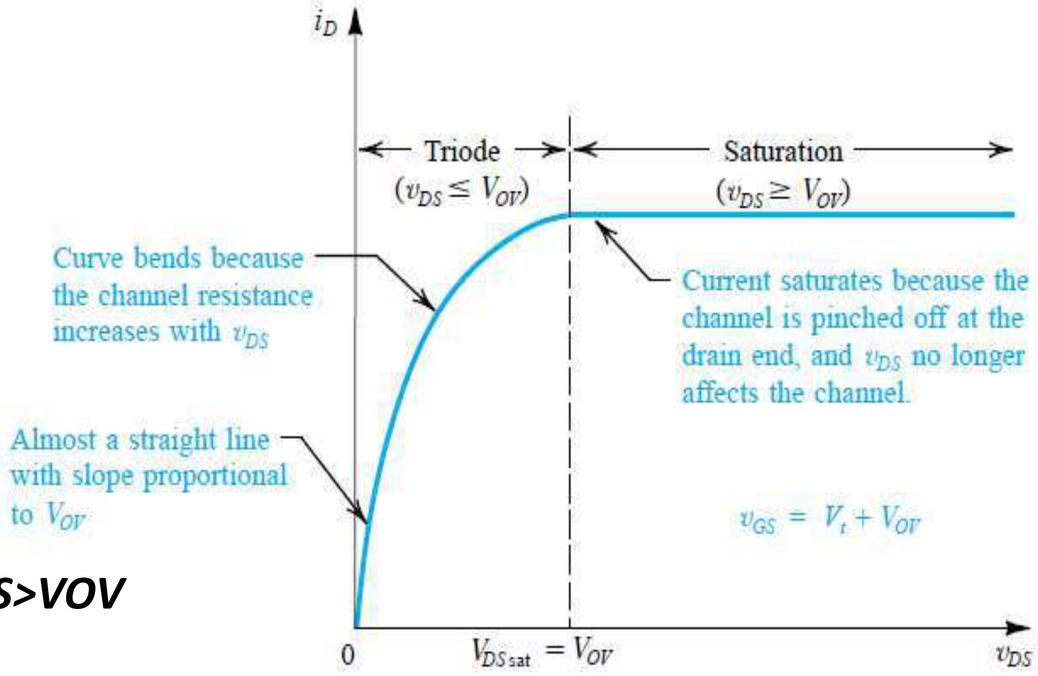
Operation as *vDS Is Increased*



Device Structure and Physical Operation-
Creating a Channel for Current Flow



$$i_D = \frac{1}{2}\left[k_n'\left(\frac{W}{L}\right)(v_{GS} - v_T)^2\right]$$



Operation for *vDS>VOV*

Device Structure and Physical Operation- **Creating a Channel for Current Flow**

$$i_D = 0 \; for \; v_{GS} < v_T$$

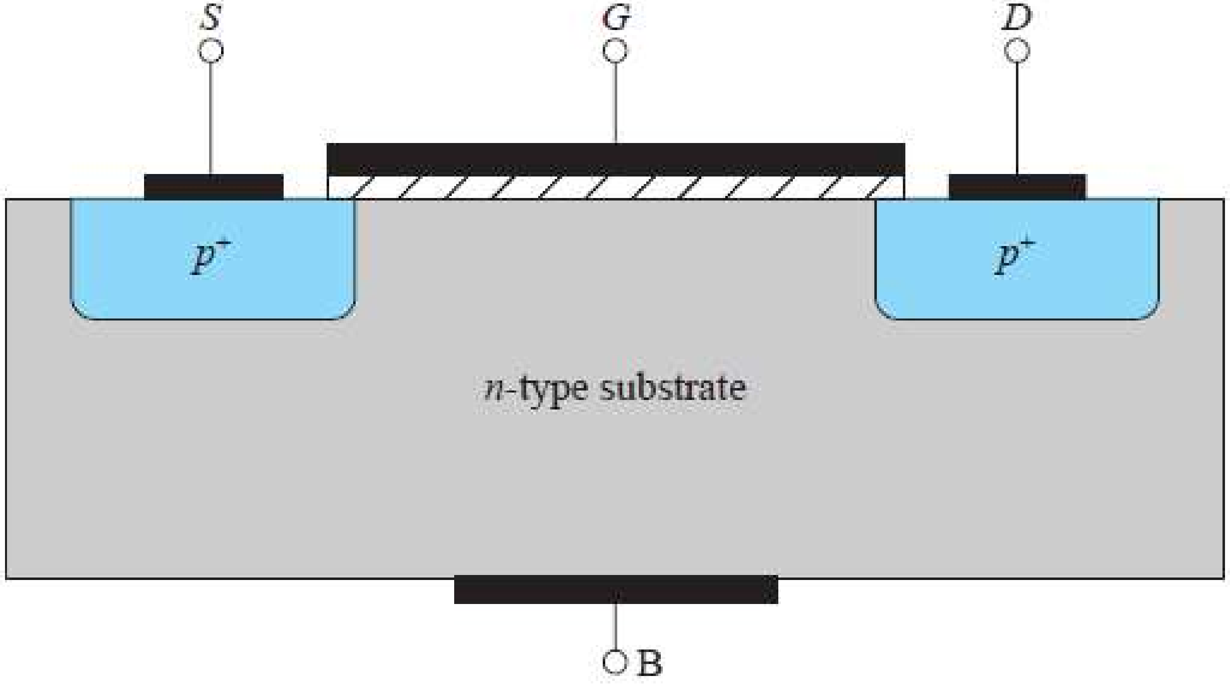
Triode Region

$$i_D = \left[k_n' \left(\frac{W}{L} \right) (v_{GS} - v_T) v_{DS} - \frac{1}{2} v_{ds}{}^2) \right] for \; v_{GS} \geq v_T \; and \; v_{ds} \leq v_{eff}$$

Saturation Region

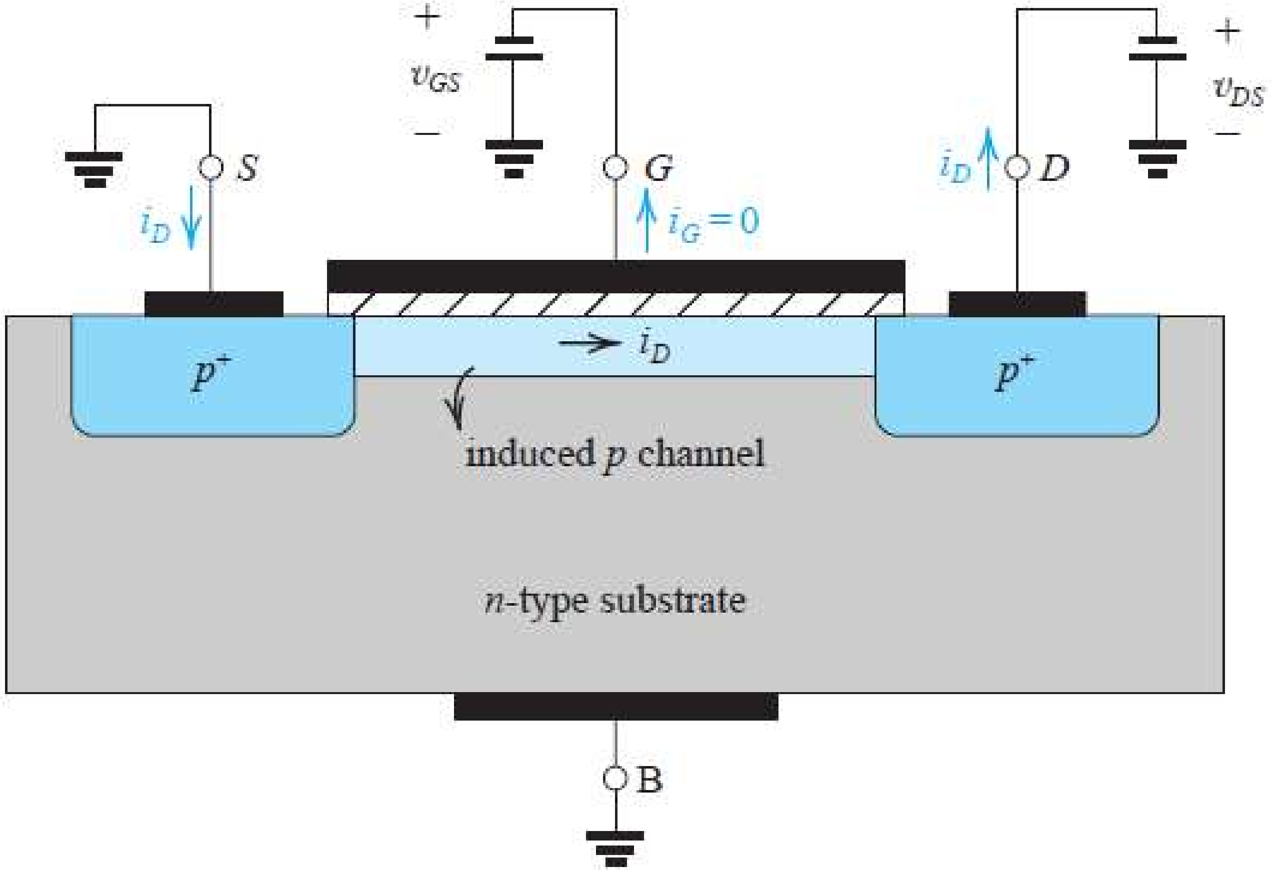
$$i_D = \frac{1}{2} \left[k_n' \left(\frac{W}{L} \right) (v_{GS} - v_T)^2 \right] for \; v_{GS} \geq v_T \; and \; v_{ds} \geq v_{eff}$$

p-Channel MOSFET



(a)

p-Channel MOSFET



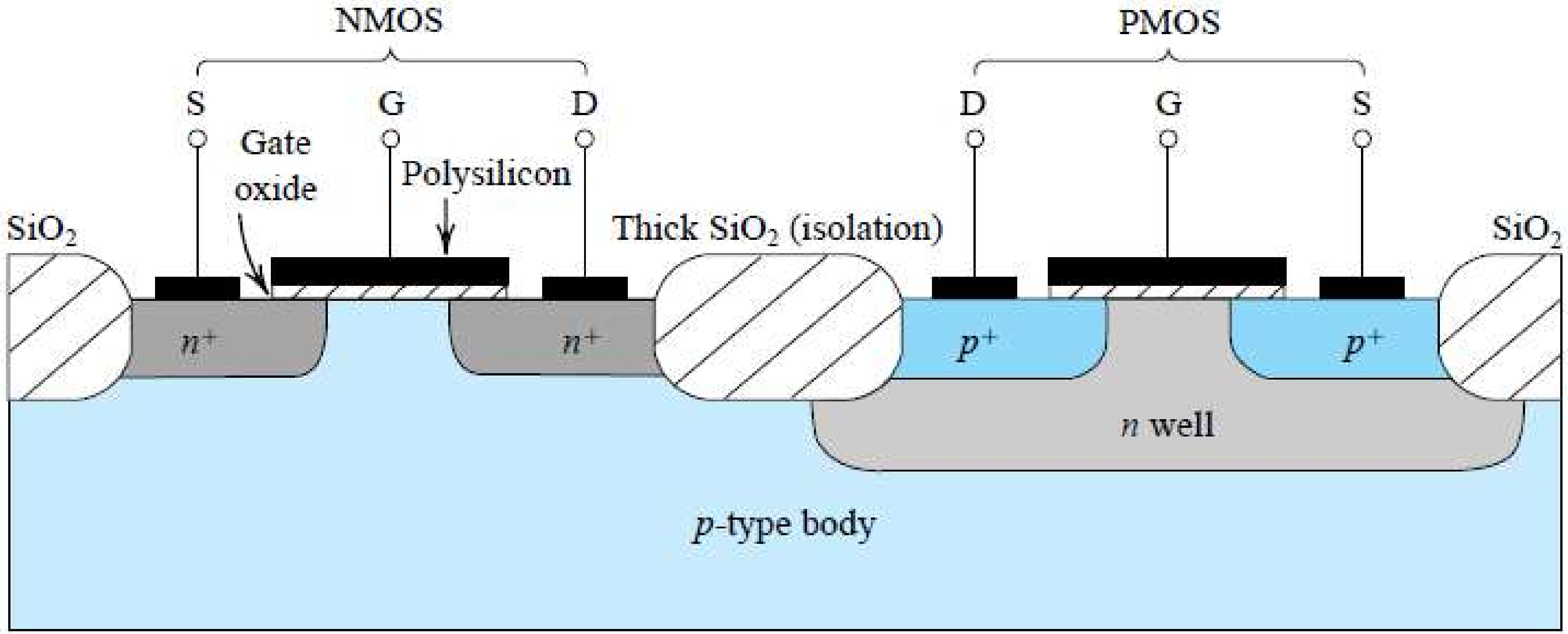
$$v_{GS} \leq V_{tp}$$

$$|v_{GS}| \geq |V_{tp}|$$

$$k_p' = \mu_p C_{ox}$$

$$k_p = k_p'(W/L)$$

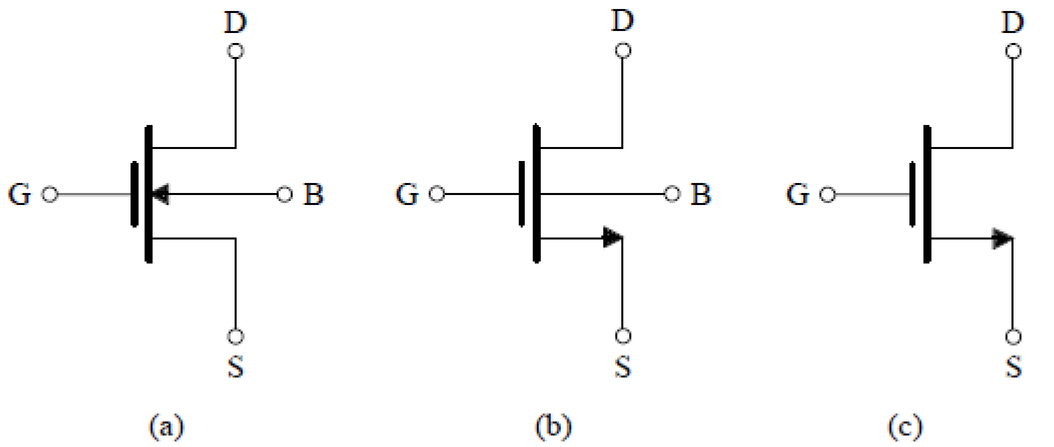
Complementary MOS or CMOS



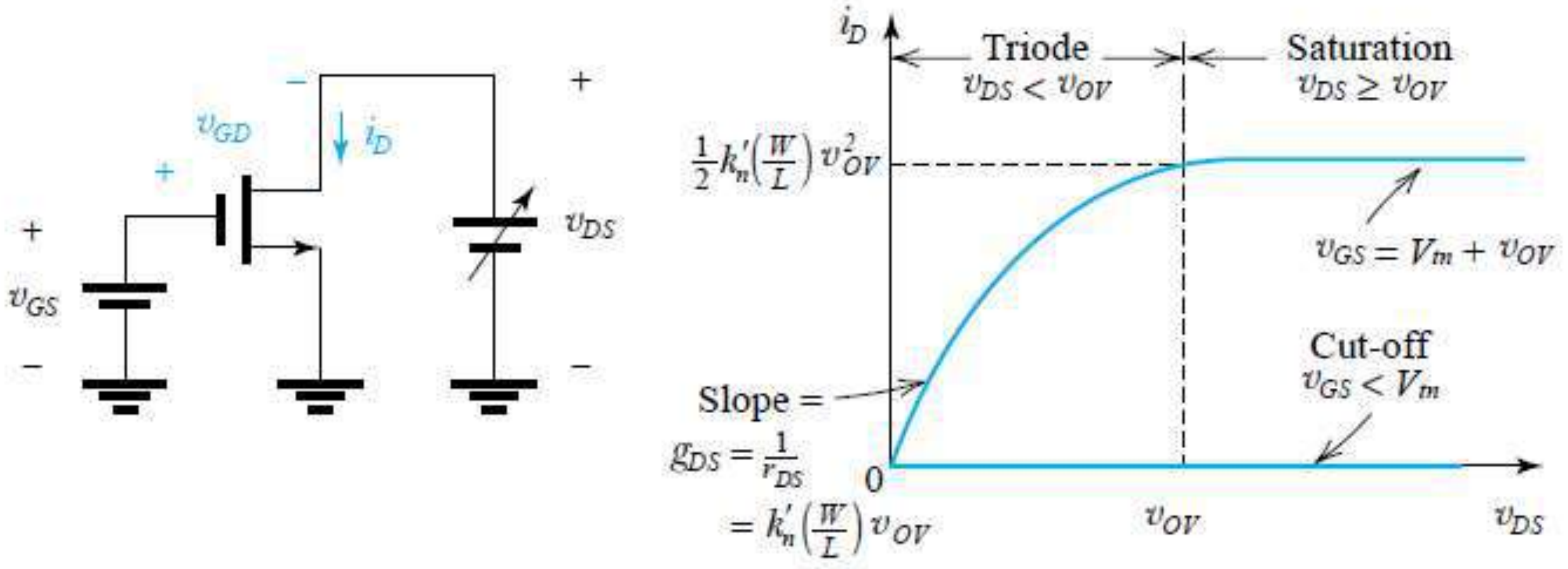
Current–Voltage Characteristics

- ➢iD – vDS Characteristics
- ➢iD – vGS Characteristics
- ➢Finite Output Resistance in Saturation
- ➢Characteristics of the p- Channel MOSFET

❖These characteristics can be measured at dc or at low frequencies and thus are called static characteristics.



Current–Voltage Characteristics



- $v_{GS} < V_{tn}$: no channel; transistor in cut-off; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

Current–Voltage Characteristics

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

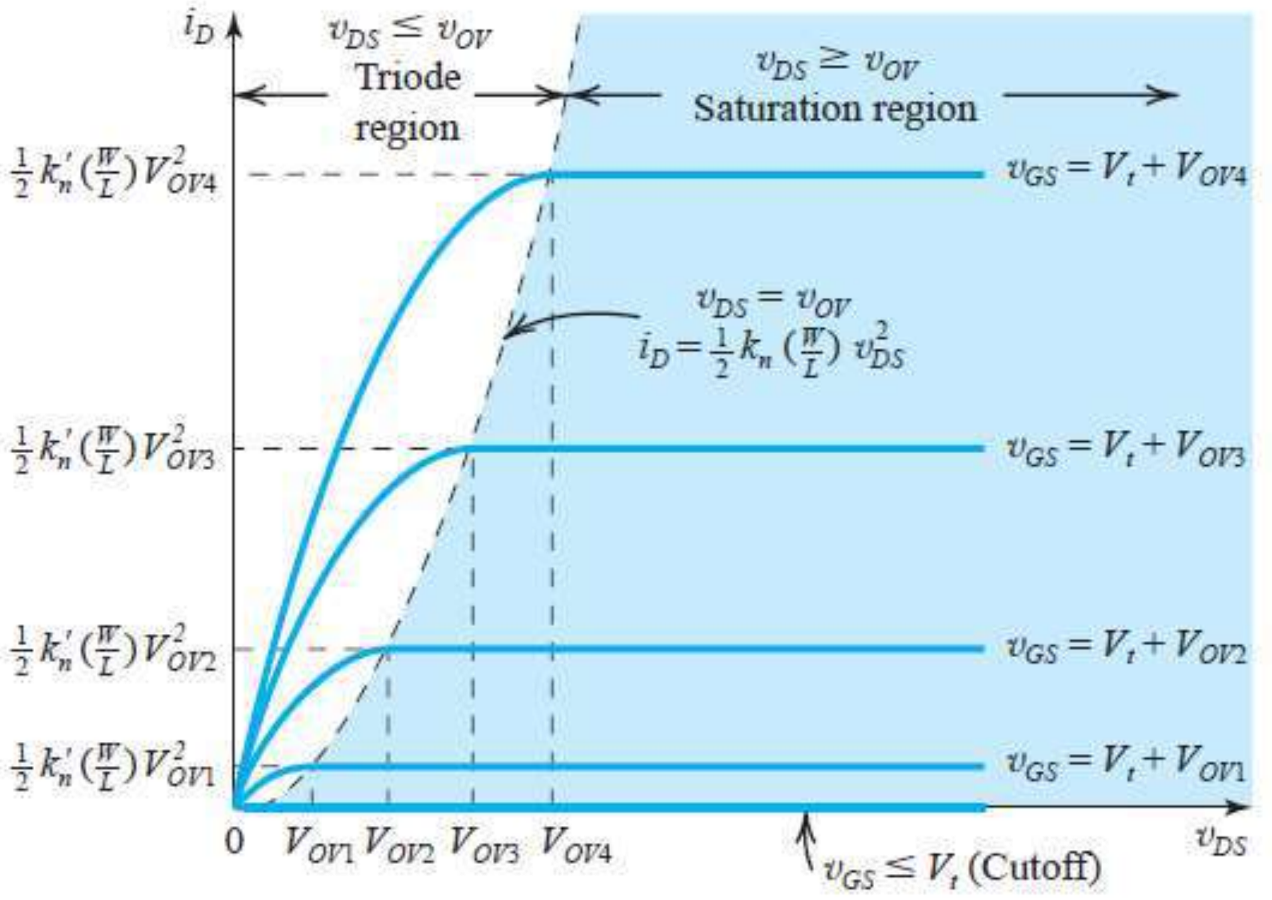
Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

Current–Voltage Characteristics

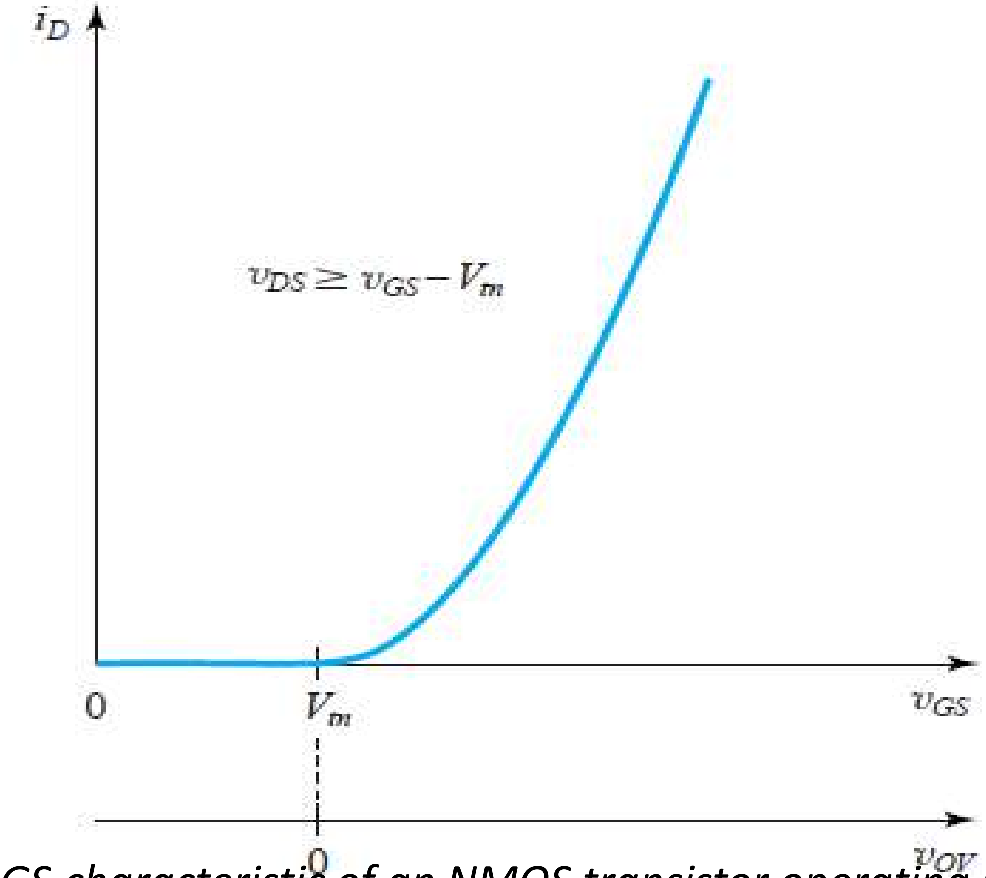


When the MOSFET is used to design an amplifier, it is operated in the saturation region.

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

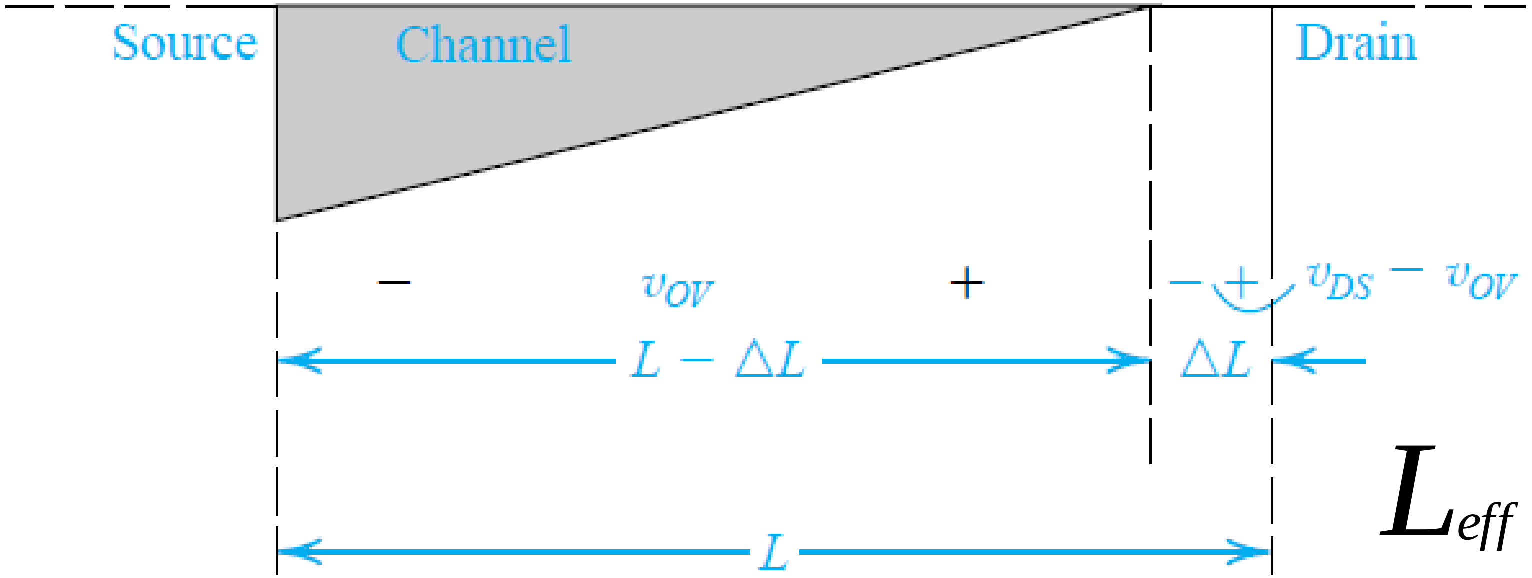
$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

Current–Voltage Characteristics



The *iD–vGS characteristic of an NMOS transistor operating in the saturation region. The iD–vOV* characteristic can be obtained by simply relabelling the horizontal axis; that is, shifting the origin to the point *vGS = Vtn.*

Current–Voltage Characteristics- Finite Output Resistance in Saturation



$$L_{eff} = L - \Delta L$$

Channel-length Modulation

Increasing *vDS beyond vDSsat causes the channel pinch-off point to move slightly away from the* drain, thus reducing the effective channel length (by Δ*L).*

Current–Voltage Characteristics- Finite Output Resistance in Saturation

$$i_D = \frac{1}{\left(1-\frac{\Delta L}{L}\right)} \frac{1}{2}\left[k_n^{'}\left(\frac{W}{L}\right)(v_{GS}-v_T)^2\right]$$

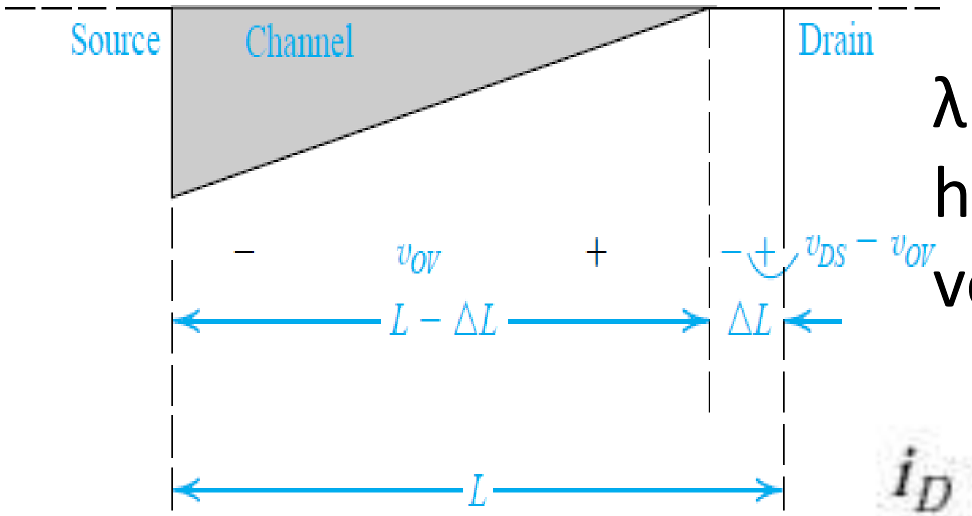
$$L_{eff} = L - \Delta L = 1 - \frac{\Delta L}{L} \approx 1 - \lambda V_{DS}$$

$$i_D = \frac{1}{2}\left[k_n^{'}\left(\frac{W}{L}\right)(v_{GS}-v_T)^2\right](1+\lambda V_{DS})$$

Channel-length Modulation

Increasing *vDS beyond vDSsat causes the channel pinch-off point to move slightly away from the* drain, thus reducing the effective channel length (by Δ*L).*

Current–Voltage Characteristics- Finite Output Resistance in Saturation



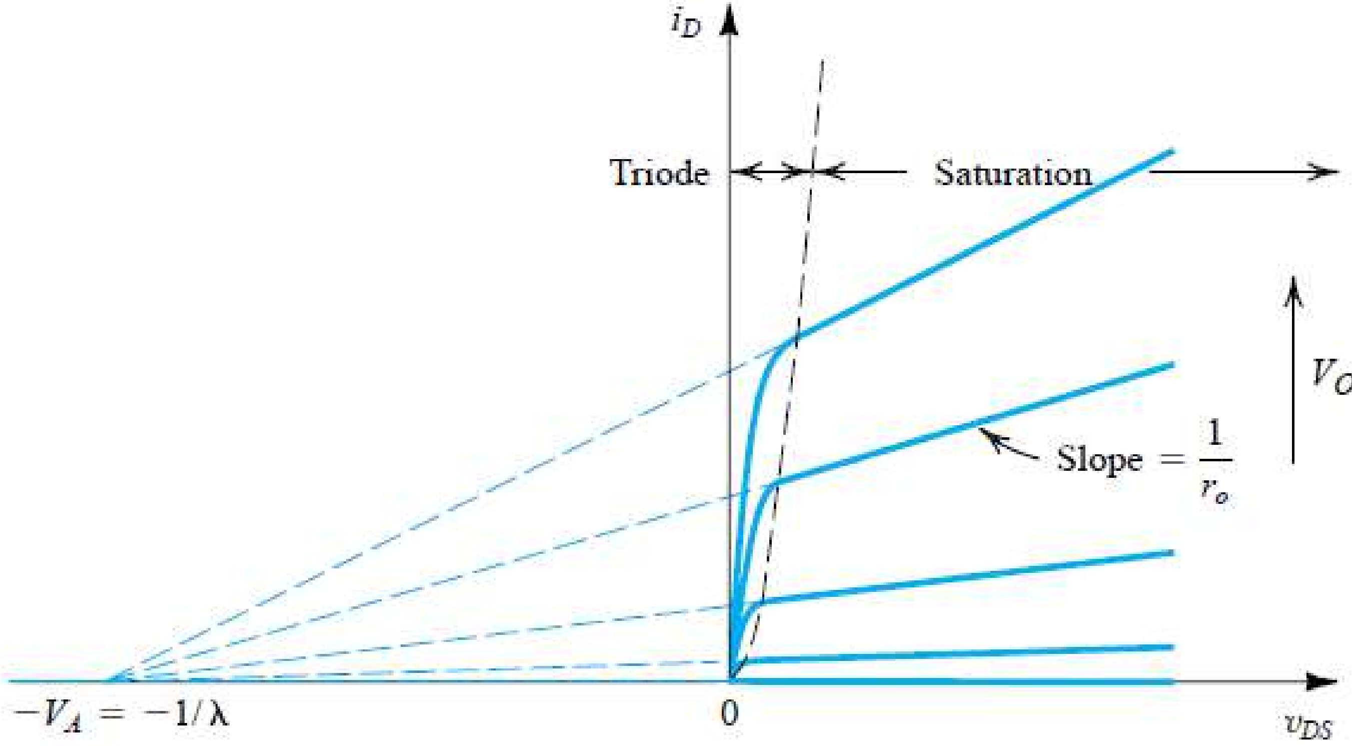
Channel-length Modulation

λ is a device parameter having the units of reciprocal volts

$$i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2 \ (1 + \lambda v_{DS})$$

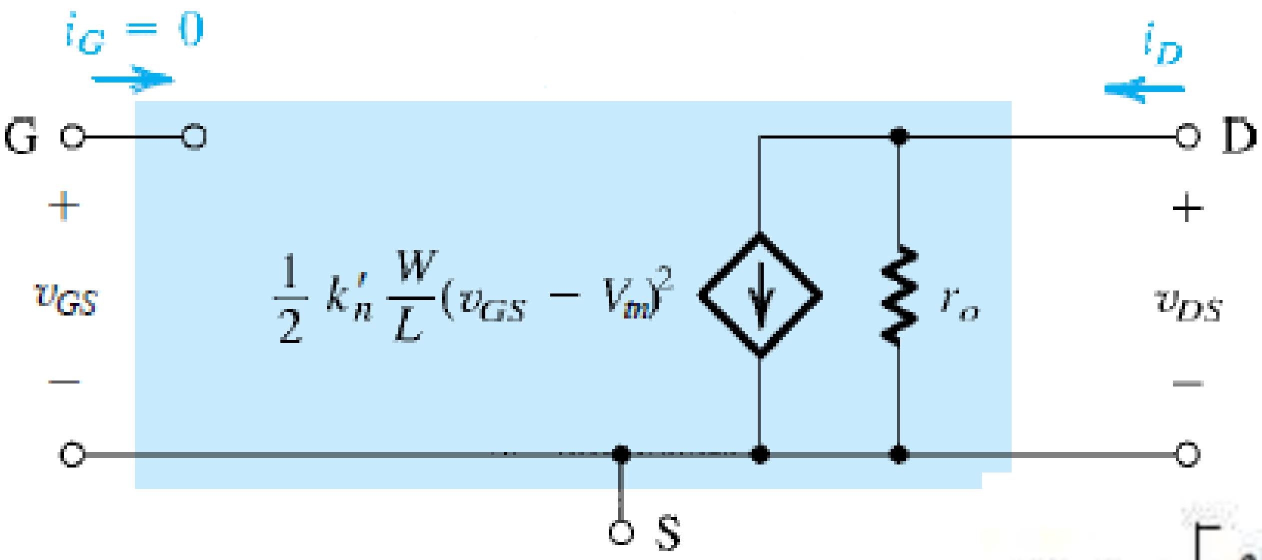
Increasing *vDS beyond vDSsat causes the channel pinch-off point to move slightly away from the* drain, thus reducing the effective channel length (by *ΔL).*

Current–Voltage Characteristics- Finite Output Resistance in Saturation



Effect of *vDS on iD in the saturation region. The MOSFET parameter VA depends on the process* technology and, for a given process, is proportional to the channel length *L.*

Current–Voltage Characteristics- Finite Output Resistance in Saturation

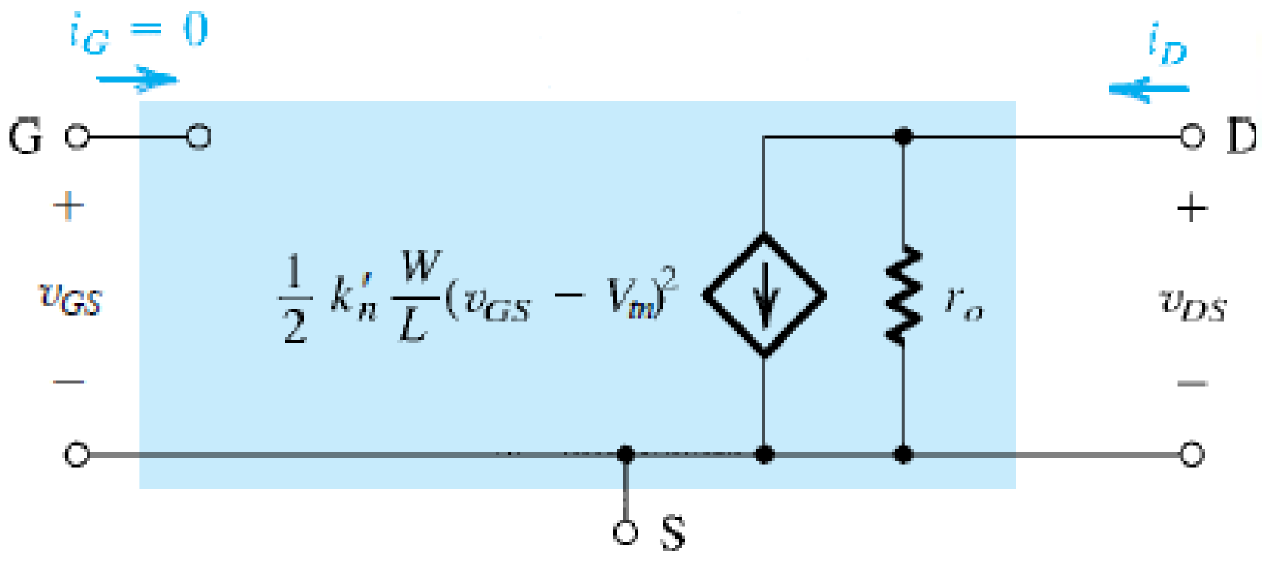


$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}\ \text{constant}}$$

$$r_o = \left[\lambda \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_{tn})^2\right]^{-1}$$

Large-signal equivalent circuit model of the *n-channel MOSFET in saturation, incorporating* the output resistance *ro.*

Current–Voltage Characteristics- Finite Output Resistance in Saturation



$$r_o = \left[\lambda \frac{k'_n}{2} \frac{W}{L} (V_{GS} - V_{tn})^2\right]^{-1}$$

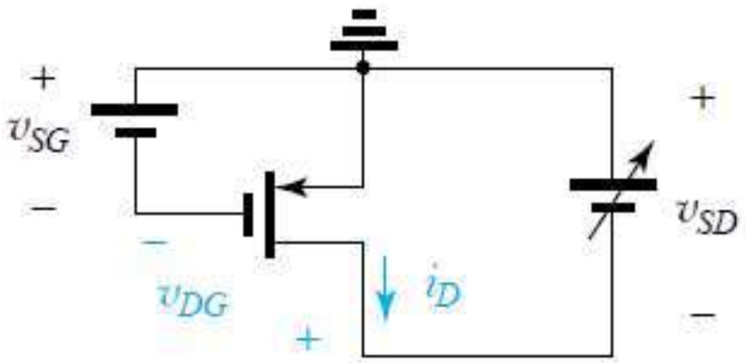
$$r_o = \frac{1}{\lambda I_D}$$

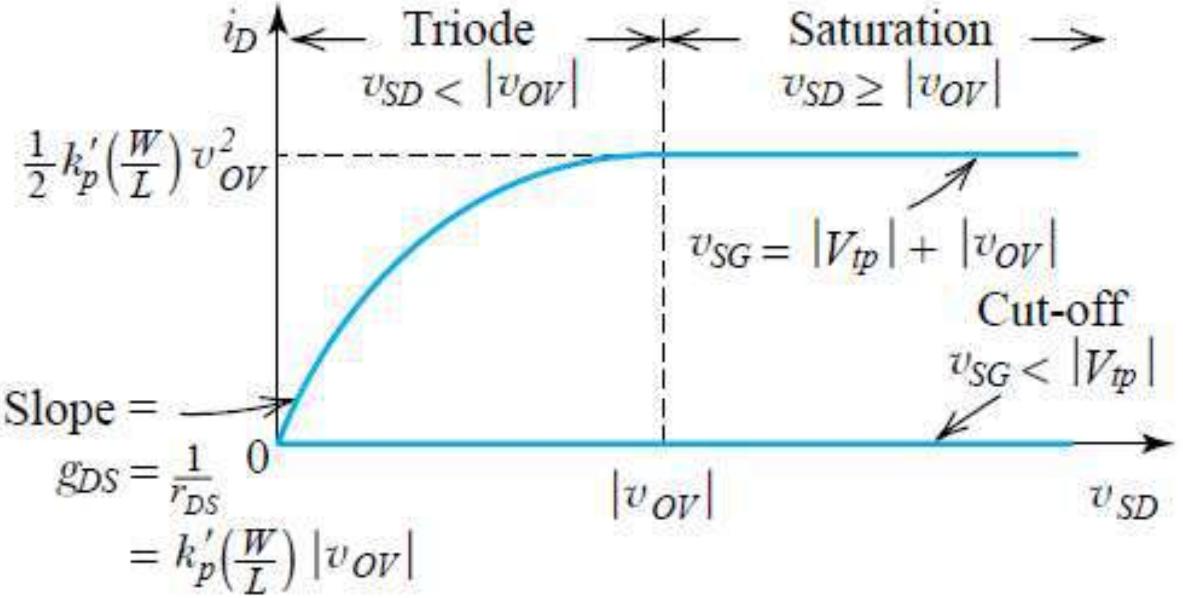
$$r_o = \frac{V_A}{I_D}$$

$$I_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_{tn})^2$$

Large-signal equivalent circuit model of the *n-channel MOSFET in saturation, incorporating* the output resistance *ro.*

Current–Voltage Characteristics- Characteristics of the *p-Channel MOSFET*





$v_{SG} < |V_{tp}|$: no channel; transistor in cut-off; $i_D = 0$

$v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

Current–Voltage Characteristics- Characteristics of the *p-Channel MOSFET*

Triode Region

Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently:

$$v_{SD} < |v_{OV}|$$

Then,

$$i_D = k_p'\left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

or equivalently

$$i_D = k_p'\left(\frac{W}{L}\right)\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{DG} \leqslant |V_{tp}|$$

or equivalently

$$v_{SD} \geqslant |v_{OV}|$$

Then

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)v_{OV}^2$$

MOSFET Circuits at DC

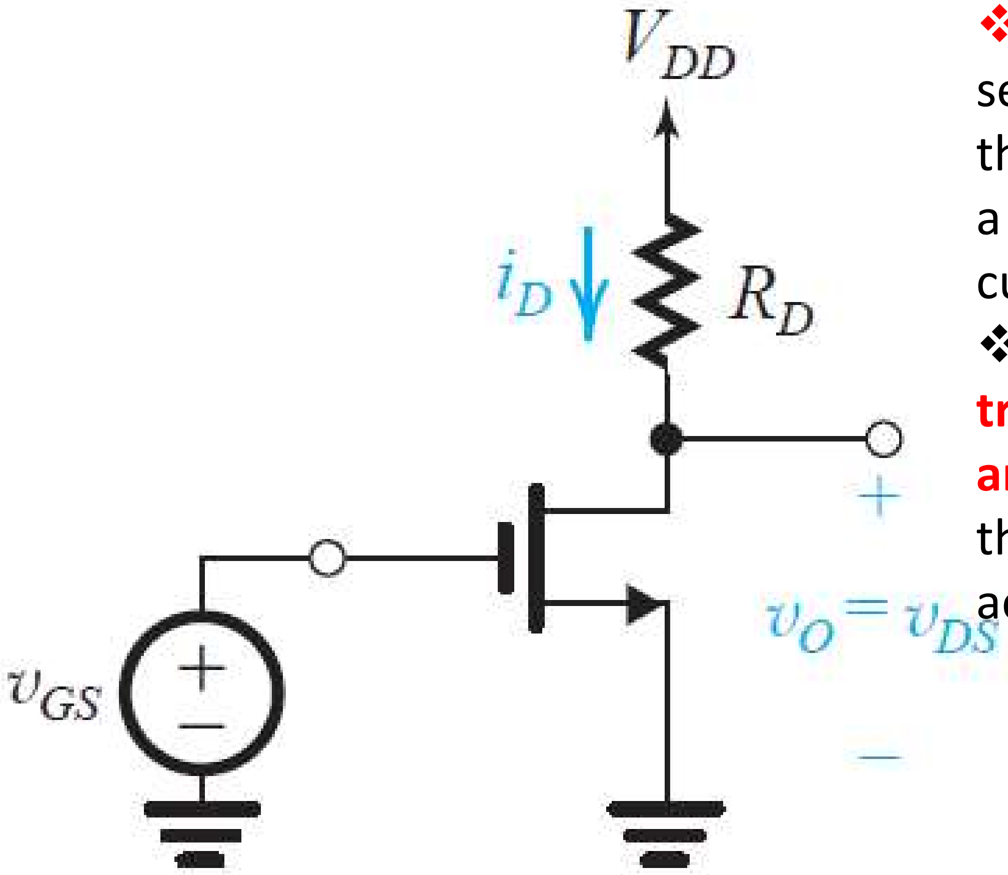
- Consider circuits in which only dc voltages and currents are of concern.
- Design and analysis examples of MOSFET circuits at dc.
- The objective is to instill in the reader a familiarity with the device and the ability to perform MOSFET circuit analysis both rapidly and effectively.
- Generally neglect channel-length modulation,λ=0

$$V_{eff} = V_{GS} - V_{tn}, V_{eff} = V_{SG} - |V_{tp}|$$

Applying the MOSFET in Amplifier Design

- The basis for this important application is that when operated in **saturation**, the MOSFET functions as v**oltage-controlled current source**: The **gate-to-source voltage** controls the **drain current** .
- Although the control relationship is nonlinear (square law)
- we will shortly devise a method for obtaining almost-linear amplification from this fundamentally nonlinear device.
    - ➢ Voltage Amplifier
    - ➢ Voltage Transfer Characteristic (VTC)
    - ➢ **Biasing the BJT to Obtain Linear Amplification**
    - ➢ Small-Signal Voltage Gain
    - ➢ Determining the VTC by Graphical Analysis
    - ➢ Q-POINT

Applying the MOSFET in Amplifier Design-Obtaining a Voltage Amplifier

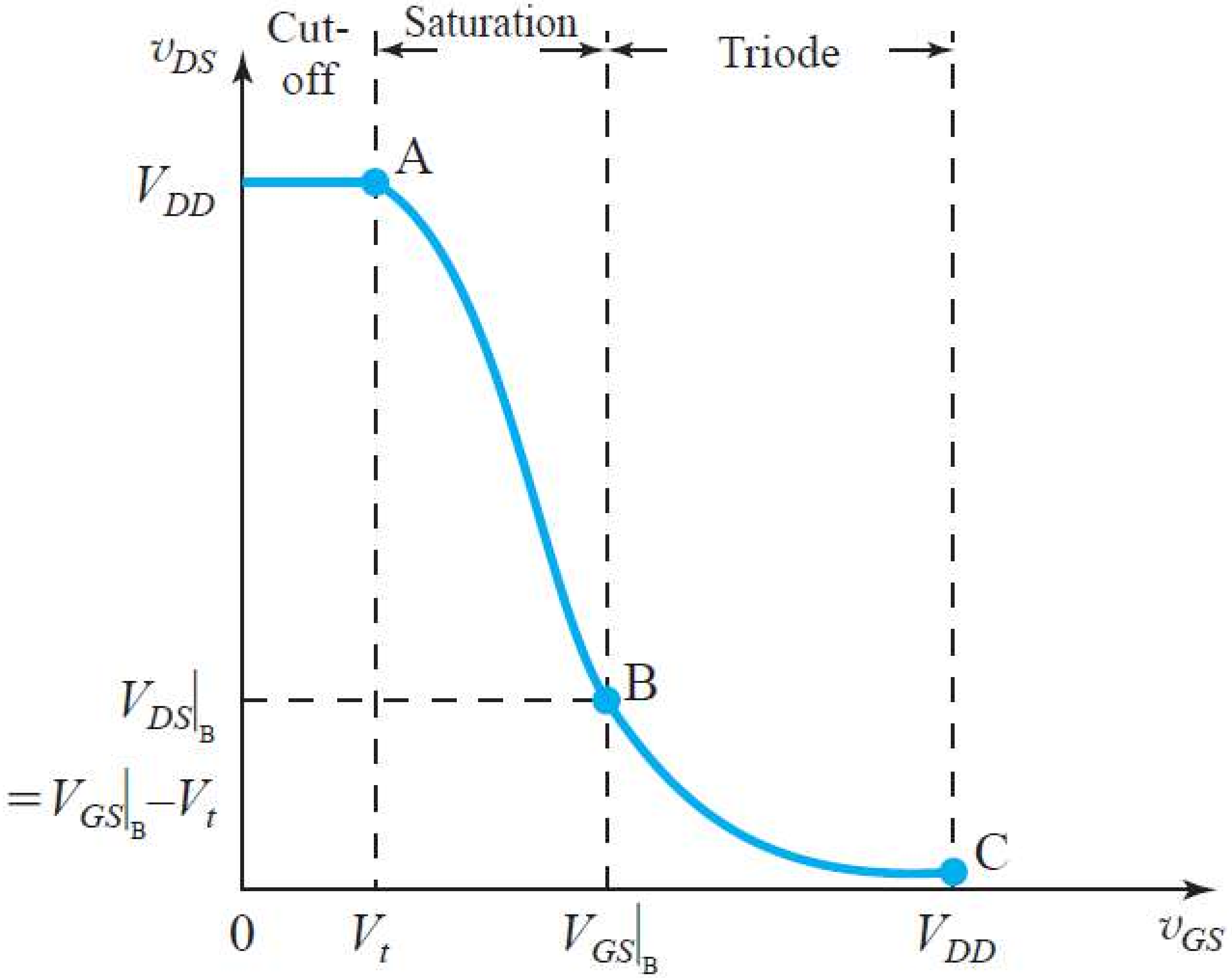


❖**Voltage-controlled current source** can serve as a **transconductance amplifier**, that is, an amplifier whose input signal is a voltage and whose output signal is a current.

❖A simple way to convert a **transconductance amplifier** to a **voltage amplifier** is to pass the **output current** through a **resistor** and take the voltage across the resistor as the output.

$$v_{DS} = V_{DD} - i_D R_D$$

Applying the MOSFET in Amplifier Design- Voltage Transfer Characteristic (VTC)



$$v_{GS} < v_T$$

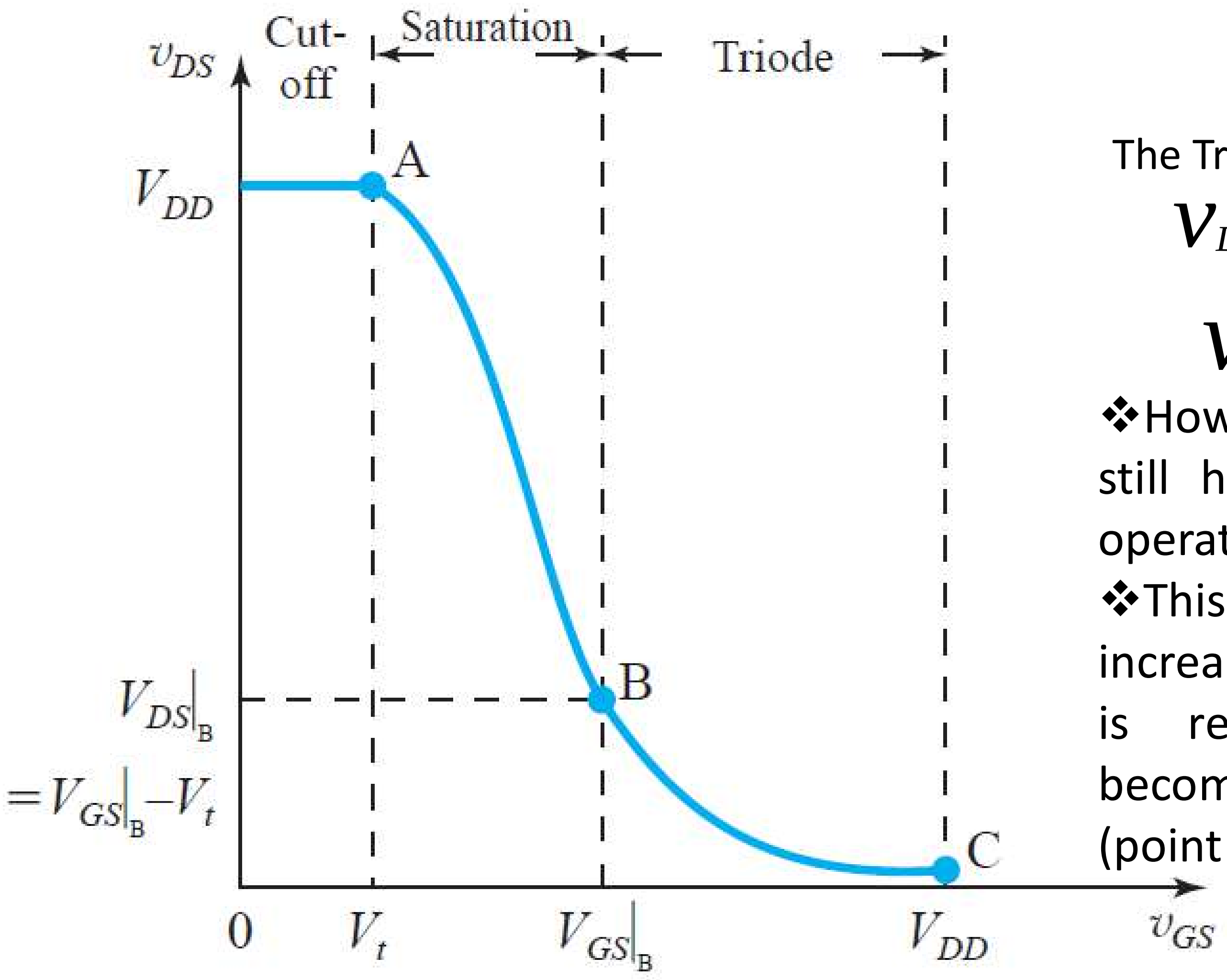
The Transistor is Cut-off

$$i_D = 0,$$

$$v_{DS} = V_{DD} - i_D R_D$$

$$v_{DS} = V_{DD}$$

Applying the MOSFET in Amplifier Design-Voltage Transfer Characteristic (VTC)



$$V_{GS} > V_T$$

The Transistor is Turns ON

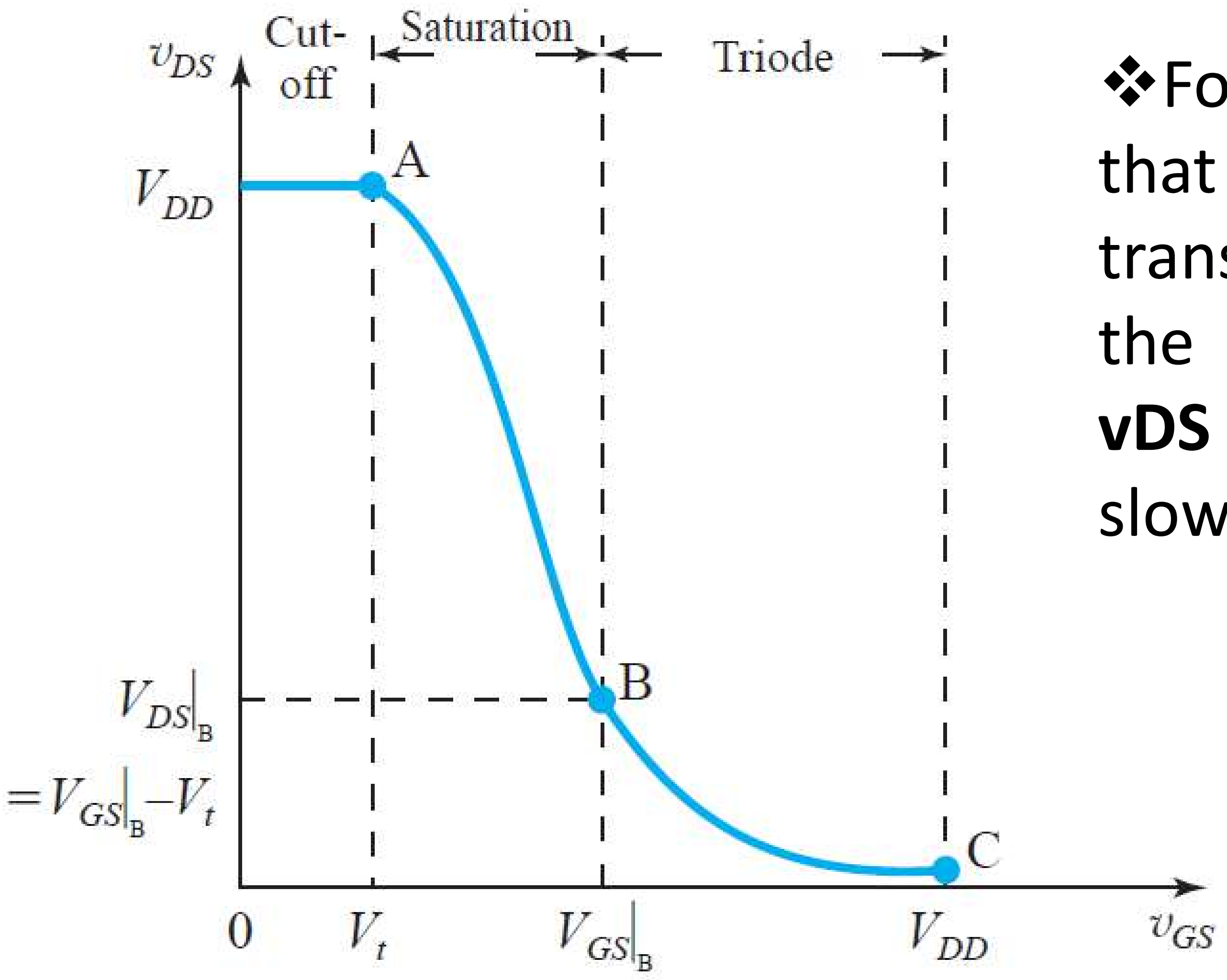
$$v_{DS} = v_{DD} - i_D R_D$$

$$v_{DS} \downarrow Decreases$$

❖However, since initially vDS is still high, the MOSFET will be operating in **saturation**.

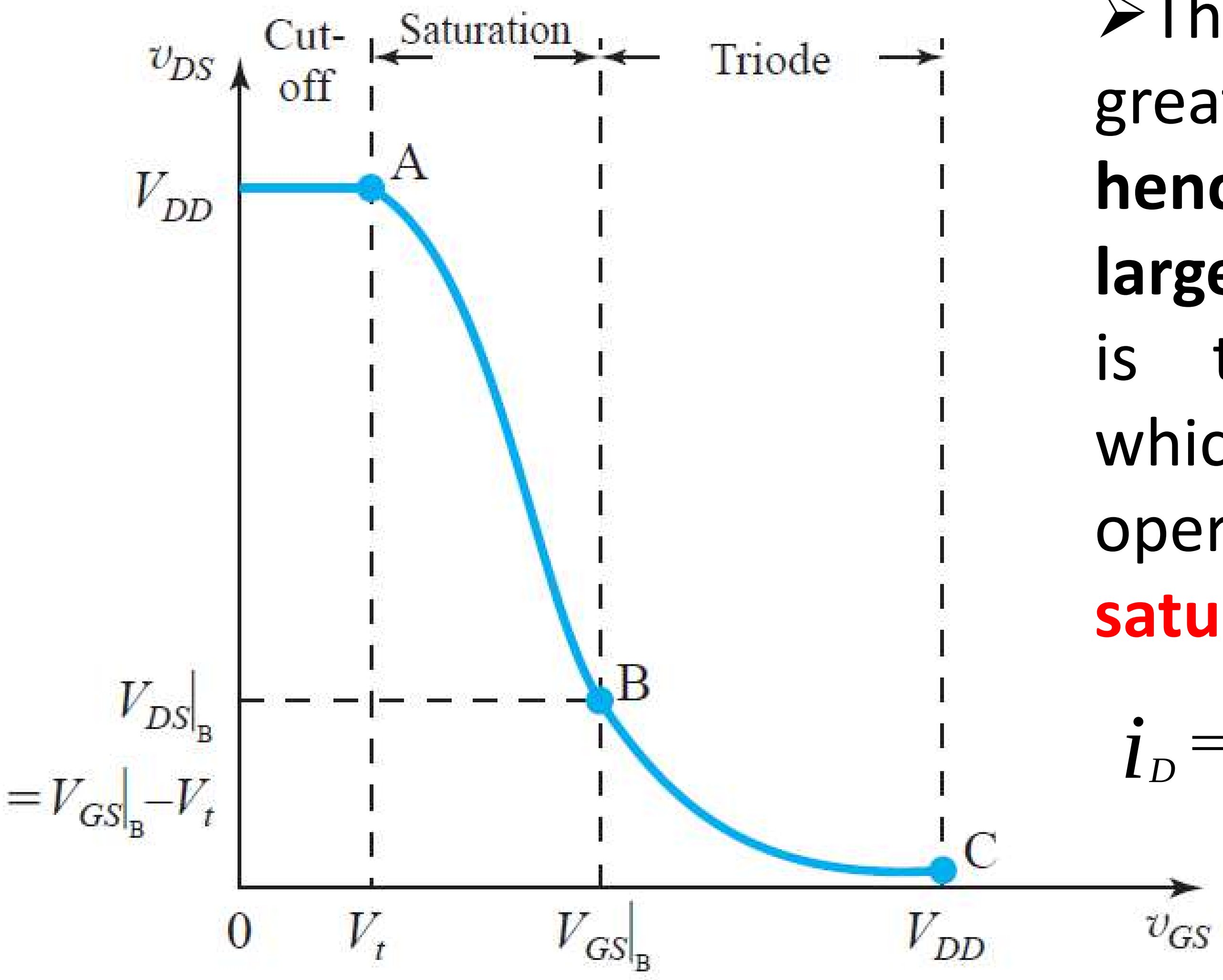
❖This continues as vGS is increased until the value of vGS is reached that results in becoming lower than by volts (point B on the VTC)

Applying the MOSFET in Amplifier Design-Voltage Transfer Characteristic (VTC)



❖For **vGS** greater than that at point B, the transistor operates in the **triode region** and **vDS** decreases more slowly.

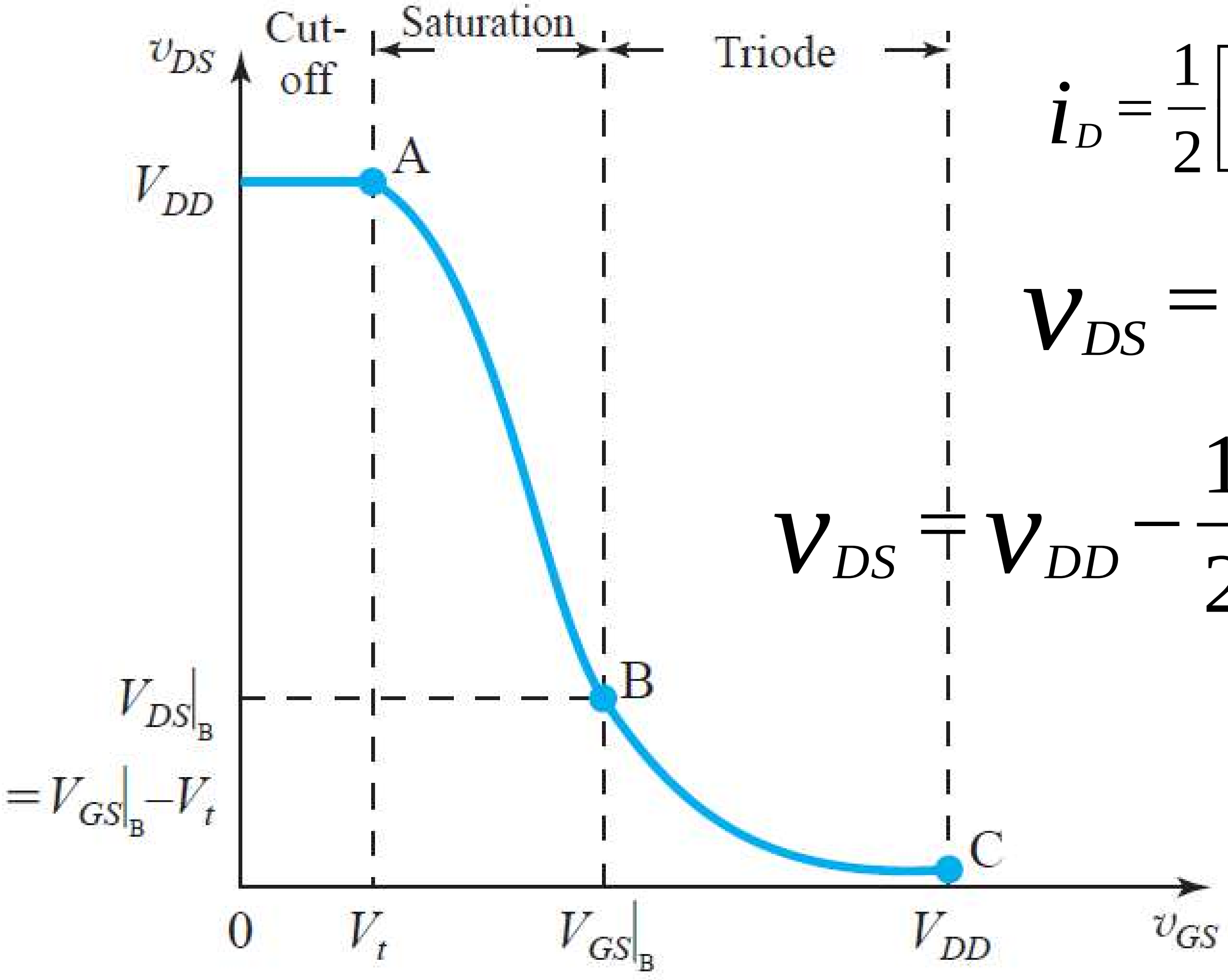
Applying the MOSFET in Amplifier Design-Voltage Transfer Characteristic (VTC)



- The segment of greatest slope **(and hence potentially the largest amplifier gain)** is that labeled AB, which corresponds to operation in the **saturation region**.

$$i_D = \frac{1}{2}\left[k_n (v_{GS} - v_T)^2\right]$$

Applying the MOSFET in Amplifier Design-Voltage Transfer Characteristic (VTC)

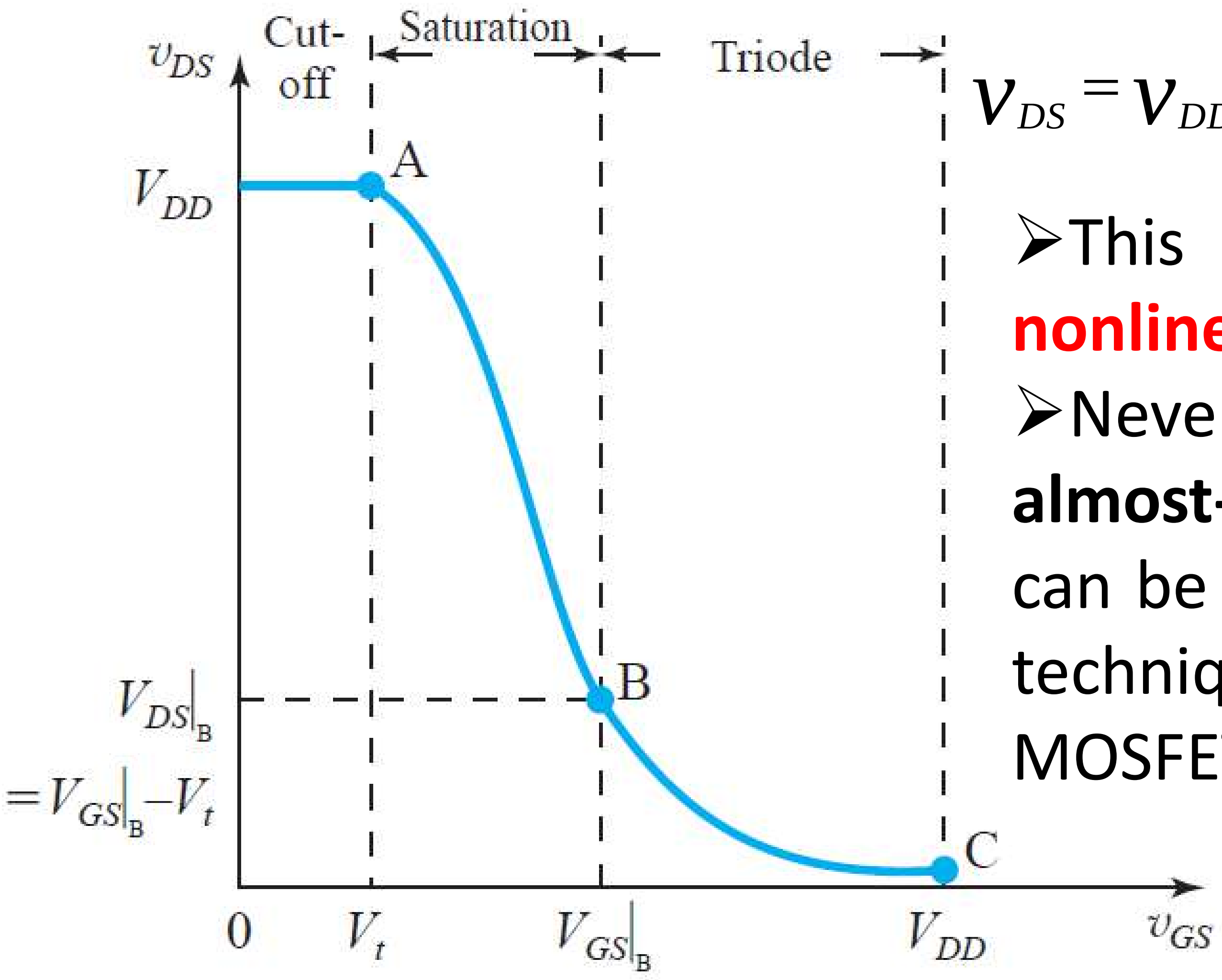


$$i_D = \frac{1}{2}\left[k_n (v_{GS} - v_T)^2\right]$$

$$v_{DS} = v_{DD} - i_D R_D$$

$$v_{DS} = v_{DD} - \frac{1}{2} k_n R_D (v_{GS} - v_T)^2$$

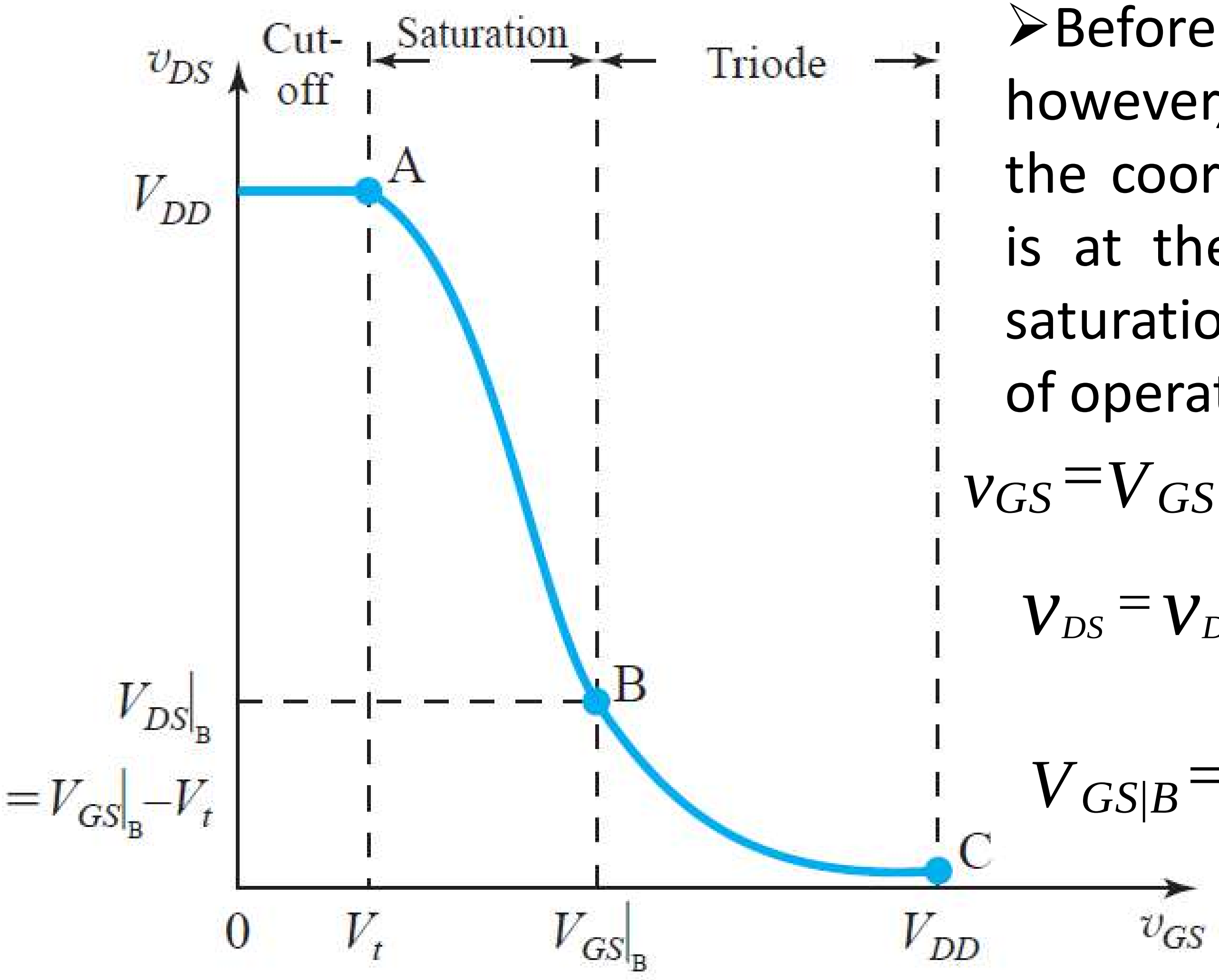
Applying the MOSFET in Amplifier Design- Voltage Transfer Characteristic (VTC)



$$v_{DS} = v_{DD} - \frac{1}{2} k_n R_D (v_{GS} - v_T)^2$$

- This is obviously a **nonlinear relationship.**
- Nevertheless, **linear (or almost-linear) amplification** can be obtained by using the technique of **biasing** the MOSFET.

Applying the MOSFET in Amplifier Design-Voltage Transfer Characteristic (VTC)



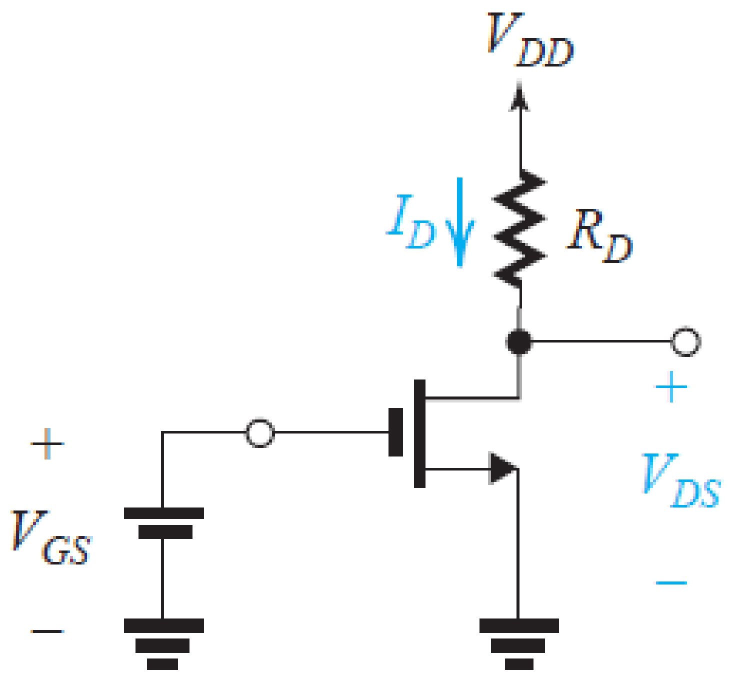
- Before considering biasing, however, it is useful to determine the coordinates of point B, which is at the boundary between the saturation and the triode regions of operation.

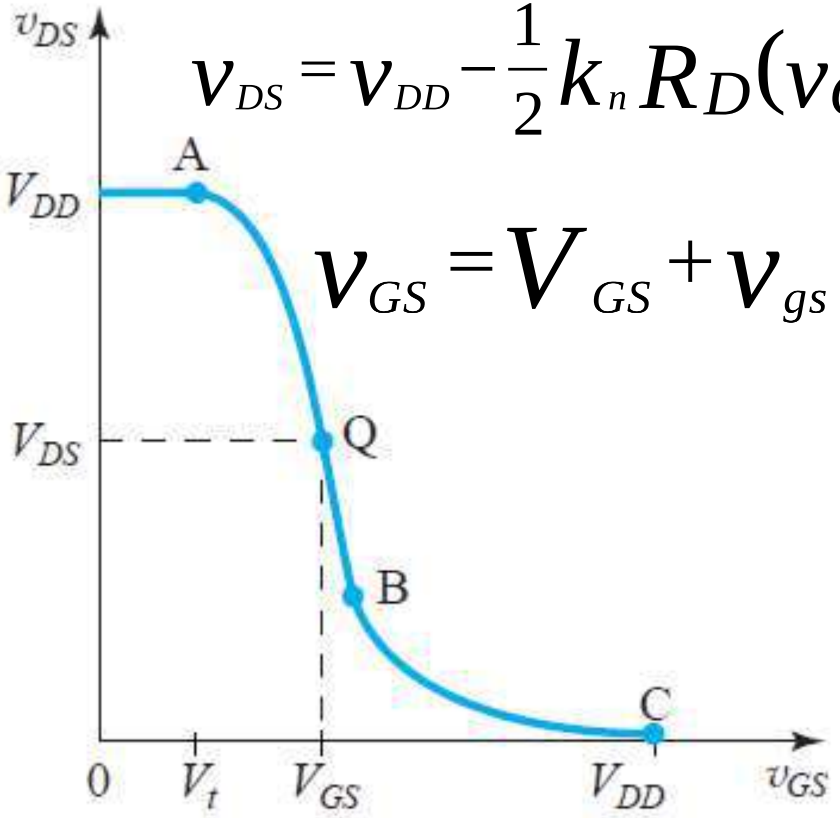
$$v_{GS} = V_{GS|B} \; and \; v_{DS} = V_{DS|B} = V_{GS|B} - V_t$$

$$v_{DS} = v_{DD} - \frac{1}{2} k_n R_D (v_{GS} - v_T)^2$$

$$V_{GS|B} = V_t + \frac{\sqrt{2 k_n R_D V_{DD} + 1} - 1}{k_n R_D}$$

Applying the MOSFET in Amplifier Design- Biasing the MOSFET to Obtain Linear Amplification

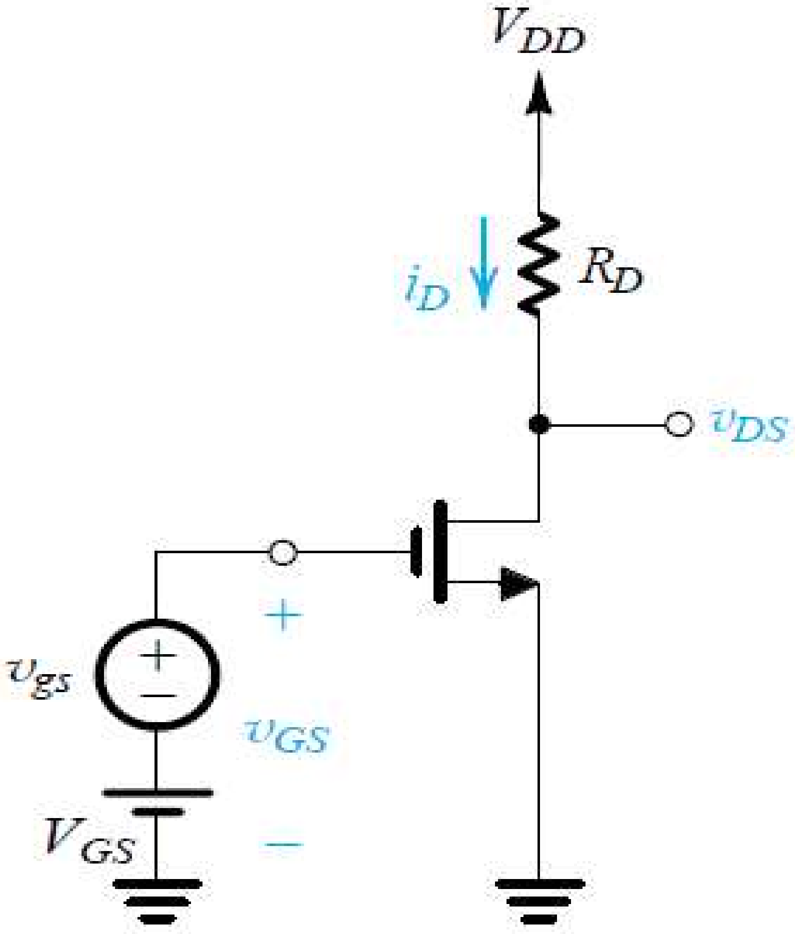




$$v_{DS} = v_{DD} - \frac{1}{2} k_n R_D (v_{GS} - v_T)^2$$

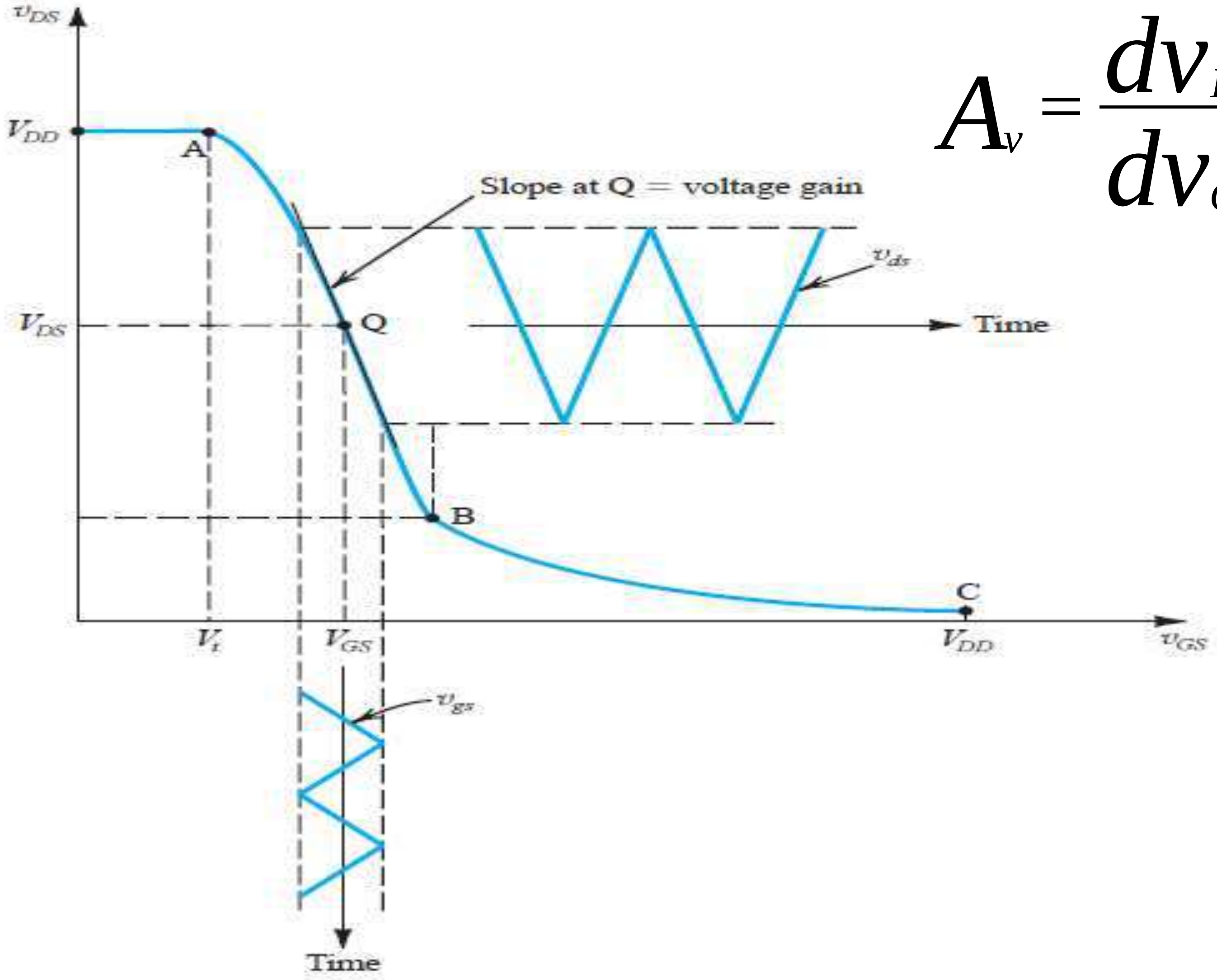
$$v_{GS} = V_{GS} + v_{gs}(t)$$

Applying the MOSFET in Amplifier Design- Biasing the MOSFET to Obtain Linear Amplification



$$v_{GS} = V_{GS} + v_{gs}(t)$$

Applying the MOSFET in Amplifier Design- Biasing the MOSFET to Obtain Linear Amplification



$$A_v = \left.\frac{dv_{DS}}{dv_{GS}}\right|_{=v_{GS}=V_{GS}}$$

Applying the MOSFET in Amplifier Design-Small Signal Voltage Gain

$$A_v = \left.\frac{dv_{DS}}{dv_{GS}}\right|_{=v_{GS}=V_{GS}}$$

$$v_{DS} = v_{DD} - \frac{1}{2}k_n R_D (v_{GS} - v_T)^2$$

$$\frac{d\,v_{DS}}{d\,v_{GS}} = 0 - \frac{1}{2}k_n R_D \cdot 2(v_{GS} - v_T)$$

$$A_v = -k_n R_D (v_{GS} - v_T) = -k_n R_D V_{eff}$$

$$i_D = \frac{1}{2}\left[k_n (V_{eff})^2\right]$$

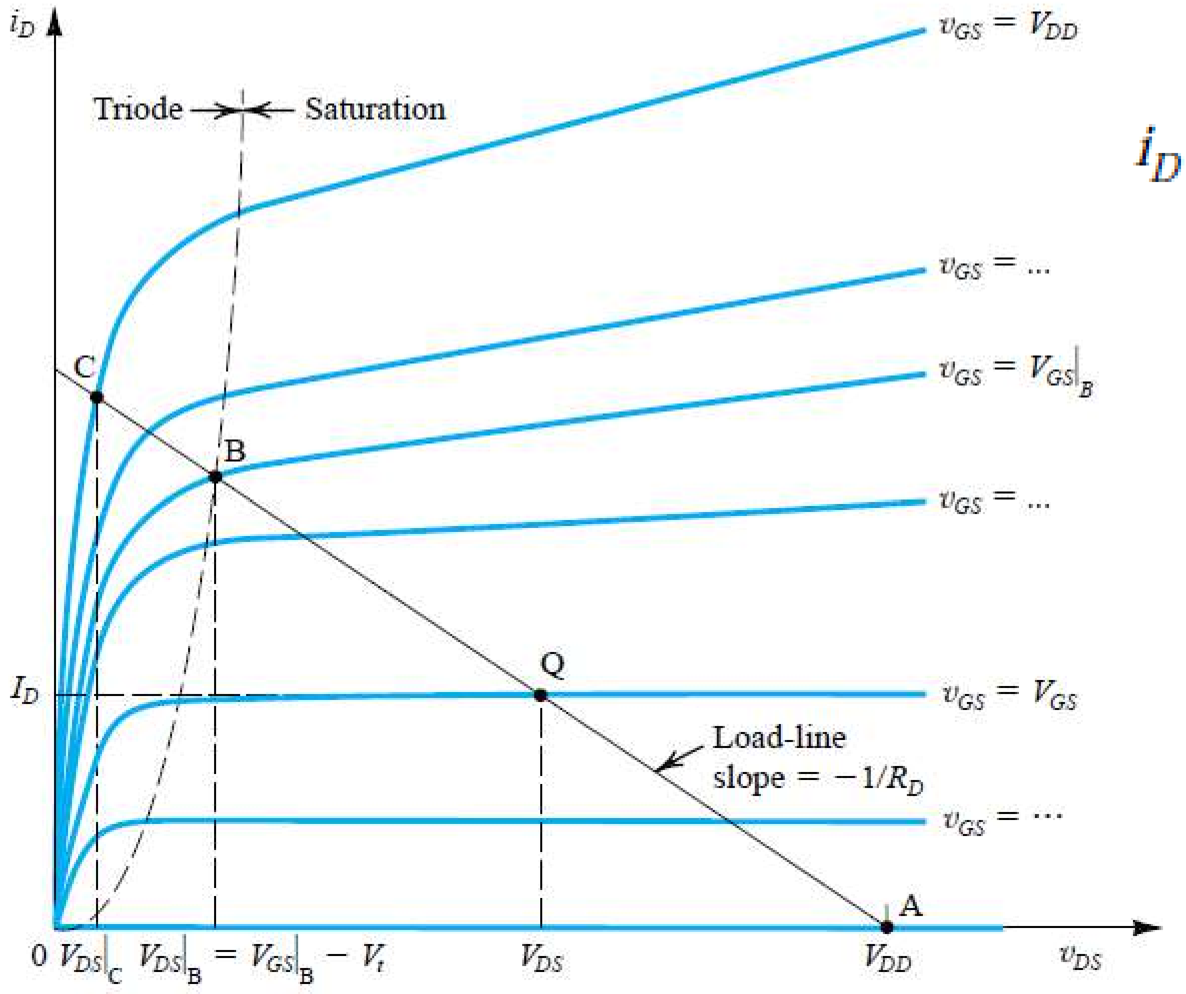
$$k_n = \frac{2 i_D}{(V_{eff})^2}$$

$$A_v = -k_n R_D V_{eff}$$

$$A_v = -\frac{2 i_D}{(V_{eff})^2} R_D V_{eff}$$

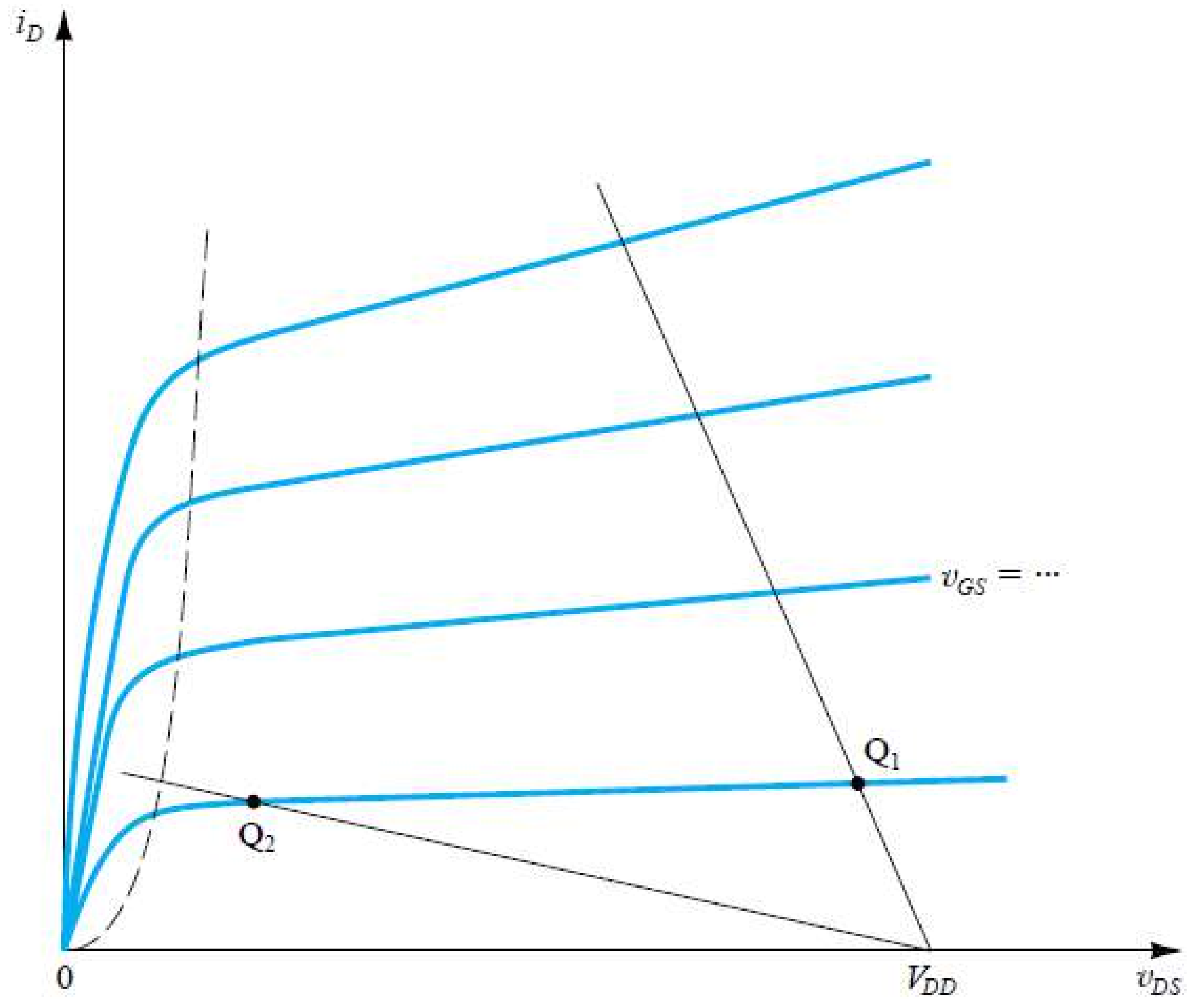
$$A_v = -\frac{i_D R_D}{V_{eff}/2}$$

Applying the MOSFET in Amplifier Design-Determining the VTC by Graphical Analysis



$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS}$$

Applying the MOSFET in Amplifier Design-Locating the Bias Point Q



Unit- 5

- **MOSFET Small Signal Operation Models**
  - The DC Bias
  - Separating the DC Analysis and the Signal Analysis
  - Small Signal Equivalent Circuit Models
  - The Transconductance
  - The T Equivalent Circuit Model
- **Basic MOSFET Amplifier Configurations**
  - Three Basic Configurations
  - Characterizing Amplifiers
  - Common Source (CS) Amplifier without and with Source Resistance
  - Common Gate (CG) Amplifier
  - Source Follower
  - The Amplifier Frequency Response
- **Biasing in MOSFET Amplifier Circuits**
  - Biasing by Fixing VGS with and without Source Resistance
  - Biasing using Drain to Gate Feedback Resistor
  - Biasing using Constant Current Source
- **Common Source Amplifier using MOSFETs**
  - Small Signal Analysis and Design
  - Body Effect
- **Problem Solving.**