



VEMU INSTITUTE OF TECHNOLOGY

P.Kothakota, Chittoor District -517112

**Two Day Workshop
on " Digital System
Design with PLD's and
FPGA"**

20.10.2017

to

21-10-2017

(Under MOU Activity)

ABOUT VEMU IT

VEMU Institute of Technology is one of the well known and finest technical institutions in Chittoor District, A.P. Beginning its quality inputs in 2008, it has attained ISO 2015:9001 certification for quality management within a short span of time. It is located on Tirupati - Chittoor highway on a beautiful 16 acre campus.

A diverse, talented community united by a passion for learning and quest for more, VEMU challenges its students to make a difference on its campus, in the region, and in the companies where ever they join. With unmatched results in every sphere of Education, its commitment to be the best has grown to transform its departments into centre of Excellence.

Topics to be covered:

- FSM's timing problems
- Introduction to VHDL for synthesis (Back-end design)
- Programming of complex PLD's(Hands-on-experience)
- Introduction to Xilinx virtex-II Architecture
- Programming FPGA using Xilinx tools (Hands-on-experience)
- Case study
- FPGA Design

Resource Person:

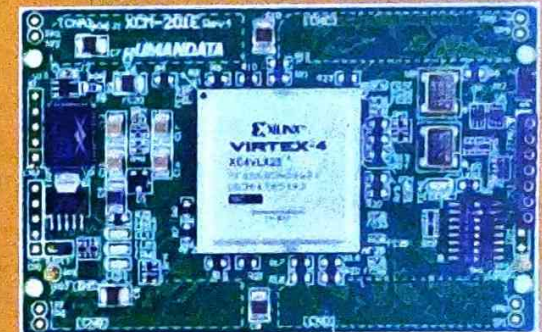
Mr.A.Munikrishna,
Technical Engineer,
takeoff edu group,
Tirupati.

TWO DAY WORKSHOP

On

**“Digital System Design
with PLD’s and FPGA”
(“VIRTEX-17”)**

20th& 21st OCT 2017



Organized by

**Department of Electronics
and Communication
Engineering,
(As a part of MOU)**



**VEMU Institute of
Technology,
P.Kothakota, Near Pakala,
Chittoor District,
Andhra Pradesh-517112.**

on
"Digital System Design
with PLD's and FPGA"
(VIRTEX-17)

Registration Form

Full Name: _____

Gender: Male/female

Designation: _____

Organization: _____

Address: _____

Mobile No: _____

Date: _____

Declaration: the information provided is true to best of my knowledge if selected I agree to abide by the rules and regulation I agree to abide by the rules and regulation of the Course and attend the course for entire duration

Place: _____

Date: _____

Signature of participant

About Department of ECE

The department offers undergraduate programme in Electronics and Communication Engineering. The Department has highly qualified, experienced and competent faculty members in the areas of Digital Image Processing, Applied Electronics, Digital Electronics, Microwave Communication, and VLSI & Embedded Systems. The department maintains several equipped laboratories for basic and advanced Electronics and Communications. The department has a separate Computer Center with Core2 Duo systems equipped with software applications and suites such as MATLAB, XILINX ISE and Multi-Sim packages. The department has a number of facilities with a substantial collection of teaching tools, instruments, equipment and computers for conducting experiments in different domains of Electronics and Communications Engineering.

Chiefpatron

Prof.Dr. K.Chandrasekhar Naidu, Chairman

Patron

Dr.KVNVN RAO, Principal

Convener

Prof.L.Ramamurthy, Prof&HOD/ECE

Co-ordinator

H.CHANDRASEKHAR,
Assoc.Professor /ECE
Department of ECE,
Vemu Institute of Technology,
P.Kothakota-517112,

Eligibility:

This Workshop is open to faculty members of AICTE approved Engineering colleges, Research Scholars working in various fields of Electronics and Communication Engineering, persons from Industry, R & D organizations and PG scholars who have a genuine interest in the field Embedded systems

Registration:

- No registration fee/-
- The number of seats for the Workshop is limited to 30 and selection is based on first come first serve basis

Accommodation

- boarding and lodging will be provided for outstation participants on payment basis

Location Map

Vemu Institute of Technology is located midway between Tirupathi and Chittoor on the Highway. There are direct trains / buses to Tirupathi or Chittoor from important cities like Hyderabad, Bangalore and Chennai. It is 4 hours journey by road from Bangalore, 3 hours from Chennai, 1 hour from Tirupathi and 30 minutes from Chittoor

Route Map to Vemu Institute of Technology





VEM INSTITUTE OF TECHNOLOGY :: P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

(Approved by AICTE, New Delhi & Affiliated to JNTUA, Anantapuramu)

Department of Electronics & Communication Engineering

Workshop Schedule

Title : "Digital System Design with PLD's & FPGA"(VIRTEX-17)

Date:20/10/2017& 21/10/2017

Resource Person: Mr.A.Munikrishna, Technical Engineer, Takeoff edu group, Tirupati

| | | Session 1 | | | Session 2 | | |
|-----------------|--|--------------------------------------|---|--|--|--------------------------------------|--|
| Timings Date | 10:00 to 11:15 (Topic) | T E A B R E A K | 11:30 to 1:00 (Topic) | L U N C H B R E A K | 1:50 to 3:00 (Topic) | T E A B R E A K | 3:15 to 4:00 (Topic) |
| 20/10/2018 | Registration/inaugural session/Introduction to Digital System Design | | Design: Hierarchy, (FSM), case study, FSM timing issues. | | VHDL for Synthesis. | | Programming of complex PLD'S (hands-on-experience) |
| 21/10/2018 | Introduction to Xilinx Virtex-II (Architecture) | | Programming FPGA's. Constraint Editor, Static Timing Analysis. Using Xilinx tools (hands-on-experience) | | Case Study/ Debugging FPGA Design, Chipscope Pro | | Valedictory |


CO-CONVENOR


CONVENOR
DEPARTMENT OF ECE
VEMU INSTITUTE OF TECHNOLOGY
P. KOTHAKOTA - 517 112



VEMU INSTITUTE OF TECHNOLOGY

P.KOTHAKOTA, TIRUPATHI-CHITTOOR ROAD, CHITTOOR, AP-517112

DEPT OF ELECTRONICS & COMMUNICATION ENGINEERING

Two days workshop on "Digital System Design With PLD'S and FPGA".
Attendance

| S.No. | Name of the Participant | 20/10/2017 | | 21/10/2017 | |
|-------|-------------------------|------------|----|------------|----|
| | | FN | AN | FN | AN |
| 1. | M Manasa | | | | |
| 2. | K Selva Kumar swamy | | | | |
| 3. | M D Bismil joffry | | | | |
| 4. | Shanti M | | | | |
| 5. | Vidhya A | | | | |
| 6. | D Sree Lakshmi | | | | |
| 7. | Sirish Grandi | | | | |
| 8. | S k Shogutha | | | | |
| 9. | S K Shabana | | | | |
| 10. | G Sindhu Bhargavi | | | | |
| 11. | Ch Leela Mohan | | | | |
| 12. | Gunasekhar D | | | | |
| 13. | Tulasiram M | | | | |
| 14. | M Mahesh | | | | |
| 15. | Sai Krishna J | | | | |
| 16. | P H Chandra Mouli | | | | |
| 17. | R Rani | | | | |
| 18. | D Reena | | | | |

CO-ORDINATOR

HEAD
DEPARTMENT OF ELECTRONICS
CONVENOR
VEMU INSTITUTE OF TECHNOLOGY
P. KOTHAKOTA - 517 112



VEMU INSTITUTE OF TECHNOLOGY

P.Kotha Kota, Pakala

A Report on

“Digital system design with PLD’s & FPGA”

As a part of MOU a Two day workshop on “Digital system design with PLD’s & FPGA” was conducted by department of ECE in collaboration with “take off edu group“ Tirupati. on 20th & 21st Oct 2017.

The Inaugural function of this workshop was held on 20-10-2017, Prof.L.Ramamurthy HOD (E.C.E) Presided over the function and given a small note on ECE department in VEMUIT. Prof.L.Ramamurthy introduced resource person Mr.A.Munikrishna Technical engineer, takeoff edu group Tirupati to the audience. Around 20 faculties from surrounding college registered for the workshop.

The main objective of the workshop is to provide hands on experience to the faculty on PLD’s and FPGA kits. Mr.L.Ramamurthy handed the session around 10:35am to the resource person, started his session by brief introduction about takeoff edu group and the assistance provided by takeoff edu group for students and staff and number of workshop/FDP/project kits organized through takeoffedu group in surrounding colleges. Resource person started with introduction to digital system design. After a small tea break resource person started session with FSM timing issues and its problems

After a lunch break resource person started session with lab session of VHDL synthesis using Xilinx tools and hands on experience on complex PLD’s.

Day-2 of workshop started with introduction to Xilinx Virtex-II kit and architecture and hand on experience on Xilinx Virtex-II kit. Afternoon session resource person mainly focused on Timing analysis using xilinx tools and a case study on Virtex-II kit. Finally workshop came to an end with a brief valedictory session which is followed by feedback from the participants and a formal vote of thanks.



VEMU INSTITUTE OF TECHNOLOGY

P.Kotha Kota, Pakala

 **VEMU INSTITUTE OF TECHNOLOGY**
P.Kothakota, Chittoor-Tirupathi highway, Chittoor, 517112, Andhra Pradesh

Two day workshop

ON
"Digital system design with PLD's and FPGA"
("VIRTEX-17")

Organized by
Department of Electronics and Communication Engineering
Venue: E.C.E Seminar Hall/E-CAD Lab,
Date: 20 & 21 Oct 2017

Principal **CONVENER** **CO-ORDINATOR**
D.K.VN VN Rao Prof. Srinivasa Rao N. GRANDRASETHAR



Faculty-In charge

HOD

HEAD

DEPARTMENT OF ECE
VEMU INSTITUTE OF TECHNOLOGY
P. KOTHAKOTA - 517 112



VEMU INSTITUTE OF TECHNOLOGY take edu

Tirupati-Chittoor Highway road, P.Kothakota, Chittoor-517112

(A Division of Young Minds Technology Solutions Pvt.Ltd)

Certificate of Participation

This is to certify that Dr./Prof./Mr./Ms./Mrs. P.H. CHANDRA MOULI of VEMU IT Participated in Two Day workshop on "Digital Systems Design with PLD's & FPGA" held during 20th to 21th October 2017 Organized by Dept. of Electronics and Communication Engineering in association with Takeoff edu Group, Tirupati at Vemu Institute of Technology, P.Kothakota, Chittoor.


Co-ordinator


PRINCIPAL
VEMU INSTITUTE OF TECHNOLOGY,
P. KOTHAKOTA - 517 112


HOD-ECE



VEMU INSTITUTE OF TECHNOLOGY

Tirupati-Chittoor Highway road, P.Kothakota, Chittoor-517112

take edu

(A Division of Young Minds Technology Solutions Pvt. Ltd.)

Certificate of Participation

This is to certify that Dr./Prof./Mr./Ms./Mrs. [✓] R.RANI of VEMU IT Participated in Two Day workshop on "Digital Systems Design with PLD's & FPGA" held during 20th to 21th October 2017 Organized by Dept. of Electronics and Communication Engineering in association with Takeoff edu Group, Tirupati at Vemu Institute of Technology, P.Kothakota, Chittoor.


Co-ordinator


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P. KOTHAKOTA - 517 112


HOD-ECE