



VEMU INSTITUTE OF TECHNOLOGY::P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

(Approved by AICTE, New Delhi & Permanently Affiliated to JNTUA

Accredited by NAAC, Recognised under 2(F) &12(B)of UGC Act 1956

An ISO 9001:2015 certified Institute)

Department of Electronics & Communication Engineering

A Seminar

ON

**“Latest Version of AV-Artix-7 FPGA
Kit Interfaces Using Xilinx”**

By


Mr. K. Ramesh Naidu,

Apply Volt,

Vijayawada.

Date: 03.01.2020

TARGETTED STUDENTS: IV ECE


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Department of Electronics & Communication Engineering

VIT/VEMU/ECE/S-01/2019-20 /SEM-II

Date: 02-01-2020

Circular

It is hereby informed to IV ECE Students that there is a Seminar on "Latest version of AV-Artix-7FPGA kit interfaces using Xilinx" on 03.01.2020 by Mr. K. Ramesh naidu, Apply Volt, Vijayawada. Hence all the students are instructed to attend the Seminar without fail.

Venue: ECE Seminar Hall

Time: 10.00AM

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HOD

HEAD
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Copy To: The Principal Desk,

The Staff In-charge,

Circulate among all class rooms.

IV - A - *[Signature]*
IV - B - *[Signature]*

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Report-On
Latest version of AV-Artix-7FPGA kit interfaces using Xilinx

(Seminar Date: 03.01.2020)

A Seminar on “**Latest version of AV-Artix-7FPGA kit interfaces using Xilinx**” was conducted by the Department of Electronics and Communication Engineering on 3rd January 2020.


This program was organized by Mr. K. Ramesh Naidu, Apply Volt, Vijayawada with the co-ordination of Mrs. K. Jayasree, Associate Professor, ECE Department and Dr. S. Muni Rathnam, Head of the ECE department.

The expert explained Latest version of AV-Artix-7FPGA kit interfaces using Xilinx advantages features and applications by showing the kit.

The FPGA KC705 Evaluation Kit includes all the basic components of hardware, design tools, IP, and pre-verified reference designs including a targeted design enabling high-performance serial connectivity and advanced memory interfacing. The included pre-verified reference designs and industry-standard FPGA Mezzanine Connectors (FMC) allow scaling and customization with daughter cards.

Features & Benefits: Optimized for quickly prototyping high performance serial transceiver applications using Kintex-7 FPGAs, Hardware, design tools, IP, and pre-verified reference designs, Demonstrates an end to end PCIe configured with 4 lanes at a 5 Gb/s link rate or 8 lanes at a 2.5 Gb/s link rate, Advanced memory interface with 1GB Memory, Enabling serial connectivity, Supports embedded processing with Micro Blaze, soft 32bit RISC, Develop networking applications with 10-100-1000 Mbps Ethernet, Implement Video display applications with HDMI out, Expand I/O with the FPGA Mezzanine Card (FMC) interface.

The resource person concluded the seminar successfully by enhancing confidence levels of each and every student and which is beneficial to the students. The total program is successfully completed with the cooperation of each and every faculty member of the department and student participants.


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Head of the Department

(Signature)
(Dr. S. Muni Rathnam)

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