

ANALOG ELECTRONIC CIRCUITS LAB MANUAL



Department of Electronics & Communication Engineering

VEMU INSTITUTE OF TECHNOLOGY::P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

(Approved by AICTE, New Delhi & Affiliated to JNTUA, Anantapuramu)

ANALOG ELECTRONIC CIRCUITS LAB MANUAL



Name: _____

H.T.No: _____

Year/Semester: _____

Department of Electronics & Communication Engineering

VEMU INSTITUTE OF TECHNOLOGY::P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

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VEMU Institute of Technology
Dept. of Electronics and Communication Engineering

Vision of the institute

To be one of the premier institutes for professional education producing dynamic and vibrant force of technocrats with competent skills, innovative ideas and leadership qualities to serve the society with ethical and benevolent approach.

Mission of the institute

Mission_1: To create a learning environment with state-of-the art infrastructure, well equipped laboratories, research facilities and qualified senior faculty to impart high quality technical education.

Mission_2: To facilitate the learners to inculcate competent research skills and innovative ideas by Industry-Institute Interaction.

Mission_3: To develop hard work, honesty, leadership qualities and sense of direction in learners by providing value based education.

Vision of the department

To develop as a center of excellence in the Electronics and Communication Engineering field and produce graduates with Technical Skills, Competency, Quality, and Professional Ethics to meet the challenges of the Industry and evolving Society.

Mission of the department

Mission_1: To enrich Technical Skills of students through Effective Teaching and Learning practices to exchange ideas and dissemination of knowledge.

Mission_2: To enable students to develop skill sets through adequate facilities, training on core and multidisciplinary technologies and Competency Enhancement Programs.

Mission_3: To provide training, instill creative thinking and research attitude to the students through Industry-Institute Interaction along with Professional Ethics and values.

Programme Educational Objectives (PEOs)

PEO 1: To prepare the graduates to be able to plan, analyze and provide innovative ideas to investigate complex engineering problems of industry in the field of Electronics and Communication Engineering using contemporary design and simulation tools.

PEO-2: To provide students with solid fundamentals in core and multidisciplinary domain for successful implementation of engineering products and also to pursue higher studies.

PEO-3: To inculcate learners with professional and ethical attitude, effective communication skills, teamwork skills, and an ability to relate engineering issues to broader social context at work place

Programme Outcomes(Pos)

| | |
|-------|--|
| PO_1 | Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems. |
| PO_2 | Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences. |
| PO_3 | Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations. |
| PO_4 | Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions. |
| PO_5 | Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations. |
| PO_6 | The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice. |
| PO_7 | Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development. |
| PO_8 | Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice. |
| PO_9 | Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings. |
| PO_10 | Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions. |
| PO_11 | Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments. |
| PO_12 | Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change. |

Programme Specific Outcome(PSOs)

| | |
|-------|---|
| PSO_1 | Higher Education : Qualify in competitive examination for pursuing higher education by applying the fundamental concepts of Electronics and Communication Engineering domains such as Analog & Digital Electronics, Signal Processing, Communication & Networking, Embedded Systems, VLSI Design and Control systems etc., |
| PSO_2 | Employment: Get employed in allied industries through their proficiency in program specific domain knowledge, Specialized software packages and Computer programming or became an entrepreneur. |

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

II B.Tech. II-Sem (EEE)

(20A04404P) ANALOG ELECTRONIC CIRCUITS LAB

COURSE OUTCOMES(CO_s)

| CO No. | Description | Blooms Level |
|---------------|---|--------------|
| C229.1 | Analyze various amplifier circuits. | 03 |
| C229.2 | Design OPAMP based analog circuits. | 02 |
| C229.3 | Understand working of logic gates. | 02 |
| C229.4 | Design and implement Combinational and Sequential logic circuits. | 02 |

PART A:

LIST OF EXPERIMENTS:

1. Design and simulate two stage RC coupled amplifier for given specifications. Determine Gain and Bandwidth from its frequency response curve.
2. Design and simulate Darlington amplifier. Determine Gain and Bandwidth from its frequency response curve.
3. Design and simulate voltage series feedback amplifier for the given specifications. Determine the effect of feedback on the frequency response of a voltage series feedback amplifier.
4. Design RC Phase shift oscillator/Wien bridge oscillator and square wave generator for the given specifications. Determine the frequency of oscillation.
5. Analyze a Class B complementary symmetry power amplifier and observe the waveforms with and without cross-over distortion. Determine maximum output power and efficiency.
6. Design inverting and non inverting amplifiers for the given specifications using OP-AMP and verify the same experimentally.
7. Design practical differentiator and integrator circuits using OP-AMP for the given specifications and verify the same practically.
8. Design a second order low pass and high pass active filters using OP-AMP using the given specifications. Verify them practically.
9. Design an astable multi-vibrator circuit for the given specifications using 555 timer. Observe ON & OFF states of transistor in an astable multi-vibrator. Plot output waveforms.
10. Design an Monostable multi-vibrator circuit for the given specifications using 555 timer. Plot output waveform.

PART B:
LIST OF EXPERIMENTS:

1. To study basic gates (AND, OR, NOT) and verify their truth tables.
2. Realization of Boolean Expressions using Gates
3. Design a 3 – bit Adder / Subtractor
4. Design and realization a 4 – bit gray to Binary and Binary to Gray Converter
5. Design and construct basic flip-flops R-S,J-K,J-K Master slave flip-flops using gates and verify their truth tables
6. Design and implementation of Mod-N synchronous counter using J-K flip-flops.
7. Design and implementation of i) Ring counter and ii) Johnson counter using 43 bit shift register
8. Design and realization of 8x1 MUX using 2x1 MUX

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Dept. of Electronics and Communication Engineering
(20A04404P) ANALOG ELECTRONIC CIRCUITS LAB



II B.Tech-II SEM(EEE)

LIST OF EXPERIMENTS TO BE CONDUCTED

PART-A:

SOFTWARE EXPERIMENTS

1. Two Stage RC Coupled Amplifier.
2. Darlington Pair Amplifier.
3. Voltage-Series Feedback Amplifier.
4. RC Phase Shift/Wien Bridge Oscillator.
5. Design Inverting and non inverting amplifiers using OP-AMP.
6. Design differentiator and Integrator Circuits using OP-AMP.

HARDWARE EXPERIMENTS

1. Two Stage RC Coupled Amplifier.
2. Darlington Pair Amplifier.
3. Voltage-Series Feedback Amplifier.
4. RC Phase Shift/Wien Bridge Oscillator.
5. Design Inverting and non inverting amplifiers using OP-AMP.
6. Design differentiator and Integrator Circuits using OP-AMP.

PART-B:

1. Study Basic gates (AND, OR, NOT).
2. Design a Full Adder.
3. Design basic flip-flops R-S,J-K, J-K master slave flip-flops using gates.
4. Design 8X1 MUX using 2X1 MUX.

ADDITIONAL EXPERIMENTS:

1. Hartley oscillator.
2. Decade counter IC7490.

CONTENTS

| S.NO. | NAME OF THE EXPERIMENT | PAGE NO |
|-------------------------------|---|---------|
| PART-A | | |
| SOFTWARE EXPERIMENT | | |
| 1 | TWO STAGE RC COUPLED AMPLIFIER. | |
| 2 | DARLINGTON PAIR AMPLIFIER. | |
| 3 | VOLTAGE-SERIES FEEDBACK AMPLIFIER. | |
| 4 | RC PHASE SHIFT/WIEN BRIDGE OSCILLATOR. | |
| 5 | DESIGN INVERTING AND NON INVERTING AMPLIFIERS USING OP-AMP. | |
| 6 | DESIGN DIFFERENTIATOR AND INTEGRATOR CIRCUITS USING OP-AMP. | |
| HARDWARE EXPERIMENTS | | |
| 1 | TWO STAGE RC COUPLED AMPLIFIER. | |
| 2 | DARLINGTON PAIR AMPLIFIER. | |
| 3 | VOLTAGE-SERIES FEEDBACK AMPLIFIER. | |
| 4 | RC PHASE SHIFT/WIEN BRIDGE OSCILLATOR. | |
| 5 | DESIGN INVERTING AND NON INVERTING AMPLIFIERS USING OP-AMP. | |
| 6 | DESIGN DIFFERENTIATOR AND INTEGRATOR CIRCUITS USING OP-AMP. | |
| PART-B | | |
| 1 | STUDY BASIC GATES (AND, OR, NOT). | |
| 2 | DESIGN A FULL ADDER. | |
| 3 | DESIGN BASIC FLIP-FLOPS R-S,J-K, J-K MASTER SLAVE FLIP-FLOPS USING GATES. | |
| 4 | DESIGN 8X1 MUX USING 2X1 MUX. | |
| ADDITIONAL EXPERIMENTS | | |
| 1 | HARTLEY OSCILLATOR | |
| 2 | DECADE COUNTER IC7490. | |

DOS & DONTs IN LABORATORY

DO's

1. Students should be punctual and regular to the laboratory.
2. Students should come to the lab in-time with proper dress code.
3. Students should maintain discipline all the time and obey the instructions.
4. Students should carry observation and record completed in all aspects.
5. Students should be at their concerned experiment table, unnecessary moment is restricted.
6. Students should follow the indent procedure to receive and deposit the components from lab technician.
7. While doing the experiments any failure/malfunction must be reported to the faculty.
8. Students should check the connections of circuit properly before switch ON the power supply.
9. Students should verify the reading with the help of the lab instructor after completion of experiment.
10. Students must ensure that all switches are in the lab OFF position, all the connections are removed.
11. At the end of practical class the apparatus should be returned to the lab technician and take back the indent slip.
12. After completing your lab session SHUTDOWN the systems, TURNOFF the power switches and arrange the chairs properly.
13. Each experiment should be written in the record note book only after getting signature from the lab in charge in the observation notebook.

DON'Ts

1. Don't eat and drink in the laboratory.
2. Don't touch electric wires.
3. Don't turn ON the circuit unless it is completed.
4. Avoid making loose connections.
5. Don't leave the lab without permission.
6. Don't bring mobiles into laboratory.
7. Do not open any irrelevant sites on computer.
8. Don't use a flash drive on computers.

SCHEME OF EVALUATION

| S.No | Program | Date | Marks Awarded | | | | Total 30(M) |
|-------------------------------|--|------|-----------------|---------------|--------------|---------------|----------------|
| | | | Record (10M) | Obs. (10M) | Viva (5M) | Attd. (5M) | |
| 1 | Two Stage RC Coupled Amplifier. | | | | | | |
| 2 | Darlington Pair Amplifier. | | | | | | |
| 3 | Voltage-Series Feedback Amplifier. | | | | | | |
| 4 | Rc Phase Shift Oscillator. | | | | | | |
| 5 | Design Inverting And Non Inverting Amplifiers Using Op-Amp. | | | | | | |
| 6 | Design Differentiator And Integrator Circuits Using Op-Amp. | | | | | | |
| 7 | Study Basic Gates (And, Or, Not). | | | | | | |
| 8 | Design A Full Adder. | | | | | | |
| 9 | Design Basic Flip-Flops R-S, J-K, J-K Master Slave Flip-Flops Using Gates. | | | | | | |
| 10 | Design 8x1 Mux Using 2x1 Mux. | | | | | | |
| ADDITIONAL EXPERIMENTS | | | | | | | |
| 1 | Hartley Oscillator | | | | | | |
| 2 | Decade counter IC7490 | | | | | | |

Signature of Lab In-charge

PART -A

SIMULATION EXPERIMENTS

CIRCUIT DIAGRAM:

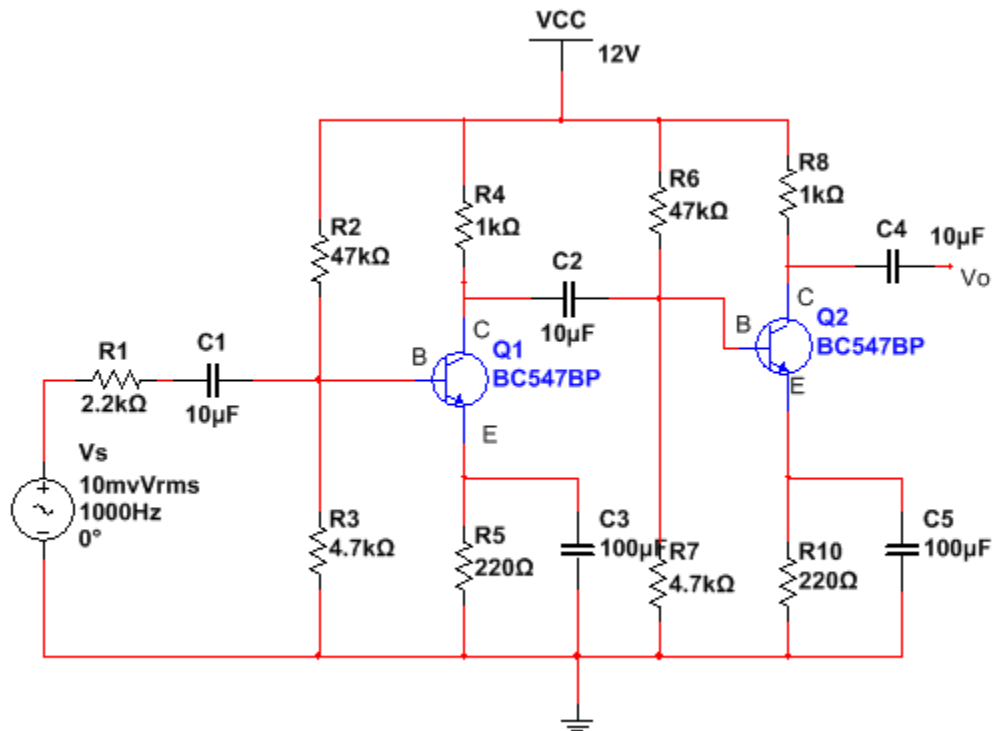
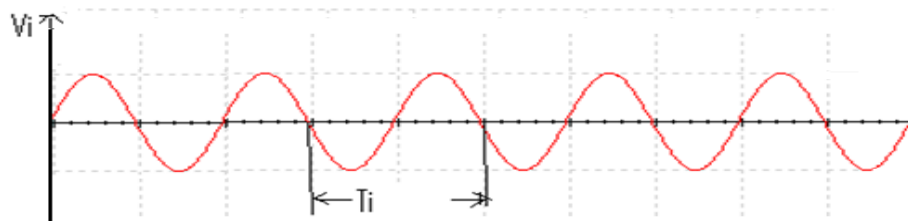


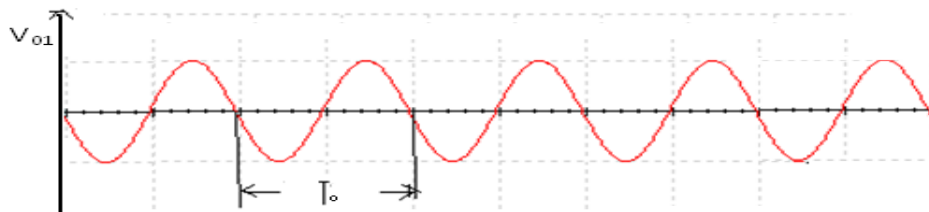
Fig: Two Stage RC Coupled Amplifier.

MODELGRAPH:-

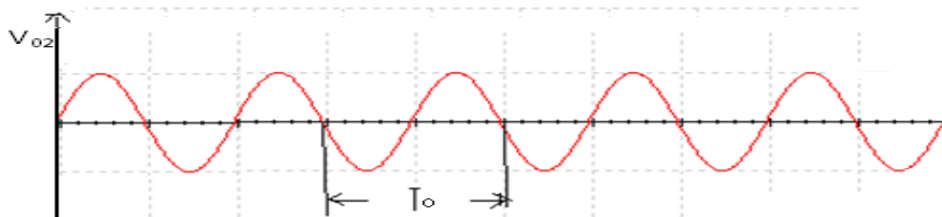
INPUT WAVEFORM:



FIRST STAGE OUTPUT:



SECOND STAGE OUTPUT:



Exp:**Date:**

TWO STAGE RC COUPLED AMPLIFIER

AIM: To design and simulate RC coupled amplifier using Multisim software and determine bandwidth.

SOFTWARE REQUIRED: NI Multisim software 14.1 version.

HARDWARE REQUIRED: Personal Computer

OPERATION:

When input AC. signal is applied to the base of the transistor of the 1st stage of RC coupled amplifier, from the function generator, it is then amplified across the output of the 1st stage. This amplified voltage is applied to the base of next stage of the amplifier, through the coupling capacitor. The signal is further amplified and reappears across the output of the second stage.

Thus the successive stages amplify the signal and the overall gain is raised to the desired level. Much higher gain can be obtained by connecting a number of amplifier stages in succession. Resistance-capacitance (RC) coupling in amplifiers are most widely used to connect the output of first stage to the input (base) of the second stage and so on. This type of coupling is most popular because it is cheap and provides a constant amplification over a wide range of frequencies.

PROCEDURE:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar.
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications.
4. Simulate the circuit.
5. Observe the response from oscilloscope and obtain the magnitude plot.
6. Extract the output voltage from the magnitude plot and determine voltage gain in dB.
7. Plot the frequency response and determine bandwidth.

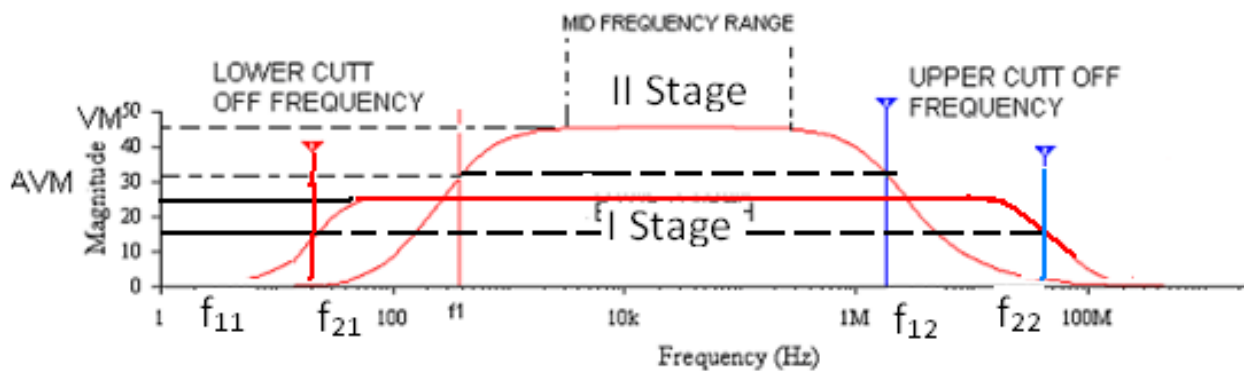
$$BW = f_2 - f_1.$$

TABULAR COLUMN: $V_i=20mV$

| S.NO | FREQUENCY(Hz) | OUTPUT VOLTAGE (V) | | GAIN (V_o/V_i) | | GAIN IN dB $A_v=20 \log_{10} (V_o/V_i)$ | |
|------|---------------|--------------------|----------|--------------------|----------|--|----------|
| | | V_{01} | V_{02} | A_{v1} | A_{v2} | A_{v1} | A_{v2} |
| | | | | | | | |
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MODEL WAVE FORMS:

MAGNITUDE PLOT:

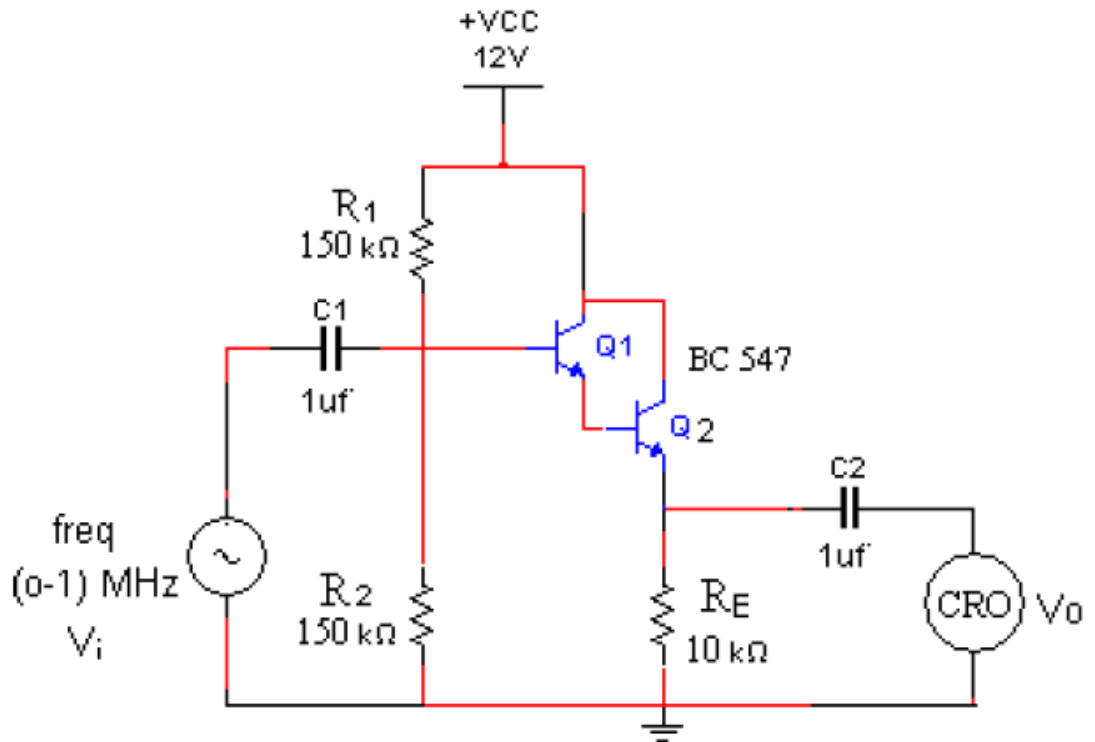


RESULT:**CONCLUSION:**
.**VIVA QUESTIONS:**

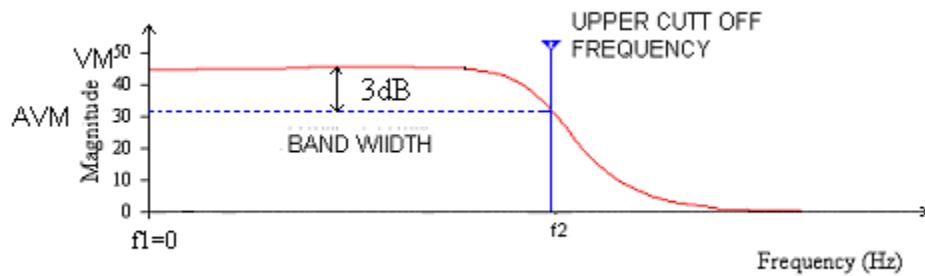
1. What is the type of capacitors are used in RC coupled amplifier?
2. Why CE configuration is used in amplifiers?
3. If voltage gain of each stage is 10, then calculate the total gain.
4. What is the effect of capacitors C_b , C_e , C_c , on frequency response of two stage RC coupled amplifier?
5. What type of Coupling is used in above circuit?

CIRCUIT DAIGRAM:

Darlington Amplifier



MODEL WAVE FORM:



Darlington Pair

Exp:**Date:****DARLINGTON PAIR****AIM:** To design and simulate Darlington pair and determine bandwidth.**SOFTWARE REQUIRED:** NI Multisim software 14.1 version.**HARDWARE REQUIRED:** Personal Computer.**OPERATION:**

A Darlington transistor pair comprises of a couple of bipolar transistors that are coupled in order to deliver a very high-current gain from a low-base current.

It is cascading of common collector-common collector. In this circuit, the emitter of the input transistor is connected to the base terminal of the output transistor.

Therefore, the current that is amplified by the first transistor is again amplified by the second transistor.

The current gain of single stage cc amplifier is high, so by using darlington pair we can get high current gain.

PROCEDURE:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications.
4. Simulate the circuit.
5. Observe the response from oscilloscope.
6. Calculate the efficiency and compare it with theoretical value.
7. Plot the graph for simulated output.

TABULAR COLUMN: $V_i=1.5V$

| S.NO | FREQUENCY(Hz) | OUTPUT VOLTAGE (V) | GAIN (V_0/V_s) | GAIN IN dB $A_v=20 \log_{10} (V_0/V_s)$ |
|------|---------------|--------------------|--------------------|--|
| | | | | |

RESULT:**CONCLUSION:****VIVA QUESTIONS:**

1. What is a Darlington pair?
2. What is the advantage of Darlington configuration?
3. Give few applications of Darlington amplifier
4. Why does amplifier gain reduce at high frequencies?
5. State the types of distortions in amplifier.

CIRCUIT DAIGRAM:

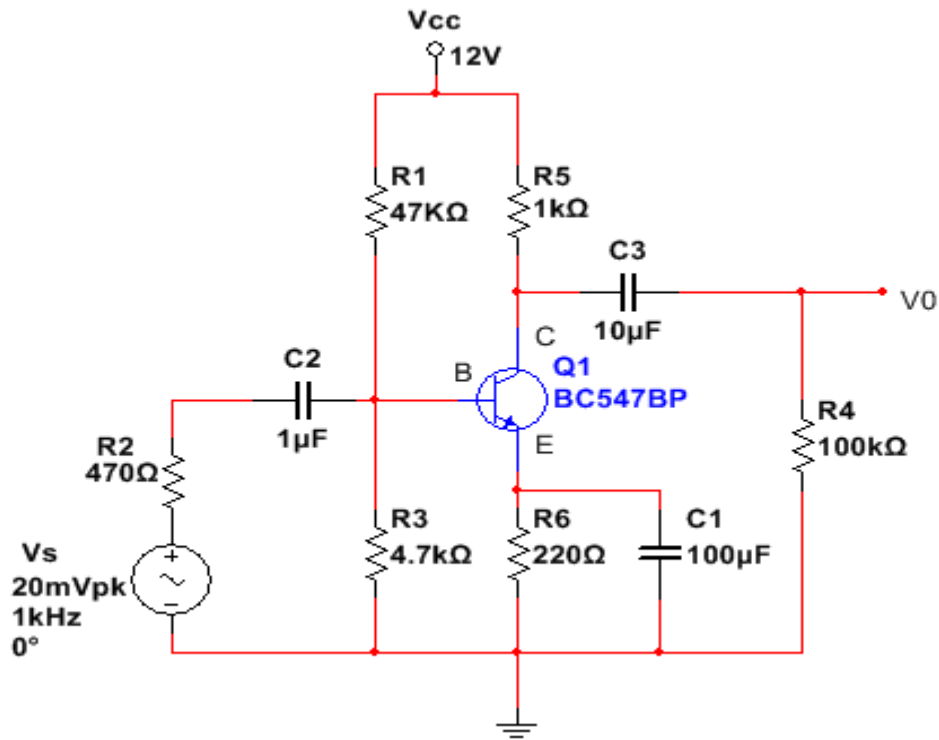
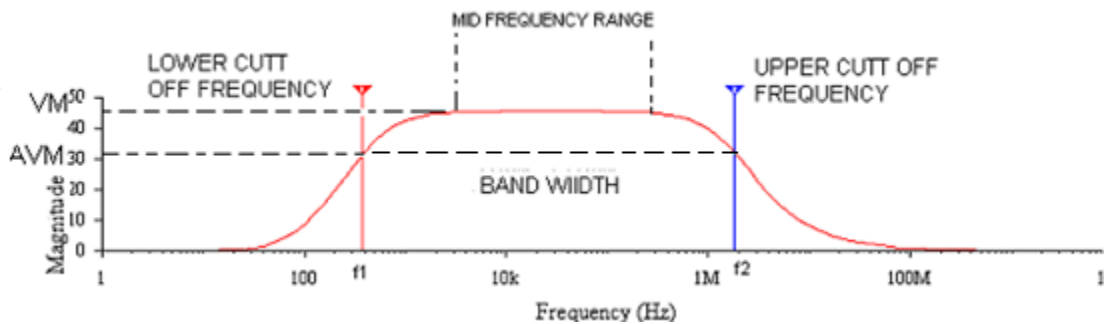


Fig: Voltage Series Feedback Amplifier.

MODEL WAVEFORMS:

MAGNITUDE PLOT



Exp:**Date:****VOLTAGE SERIES FEEDBACK AMPLIFIER**

AIM: To design and simulate the voltage series feedback amplifier using Multisim software and determine bandwidth.

SOFTWARE REQUIRED: NI Multisim software 14.1 version.

HARDWARE REQUIRED: Personal Computer.

OPERATION:

The fraction of output voltage is applied in series with input voltage through feedback circuit. Feedback circuit shunt the output but in series with input. So the output impedance is decreased while input impedance is increased. The input & output impedance of an ideal voltage series feedback amplifier is infinite & zero respectively. The resistor R_E is used to provide necessary biasing for the amplifier with voltage series feedback gain of the amplifier decreases.

PROCEDURE:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications.
4. Simulate the circuit.
5. Observe the response from oscilloscope and obtain the magnitude plot.
6. Extract the output voltage from the magnitude plot and determine voltage gain in dB.
7. Plot the frequency response and determine bandwidth.

$$BW = f_2 - f_1.$$

RESULT:**CONCLUSIONS:****VIVA QUESTIONS:**

1. Why CE Configuration is preferred over other configurations in amplifiers?
2. What is meant by feed back?
3. Define Stability?
4. What are the types of feed backs?
5. What are the advantages of negative feedback in amplifiers?

CIRCUIT DIAGRAM:

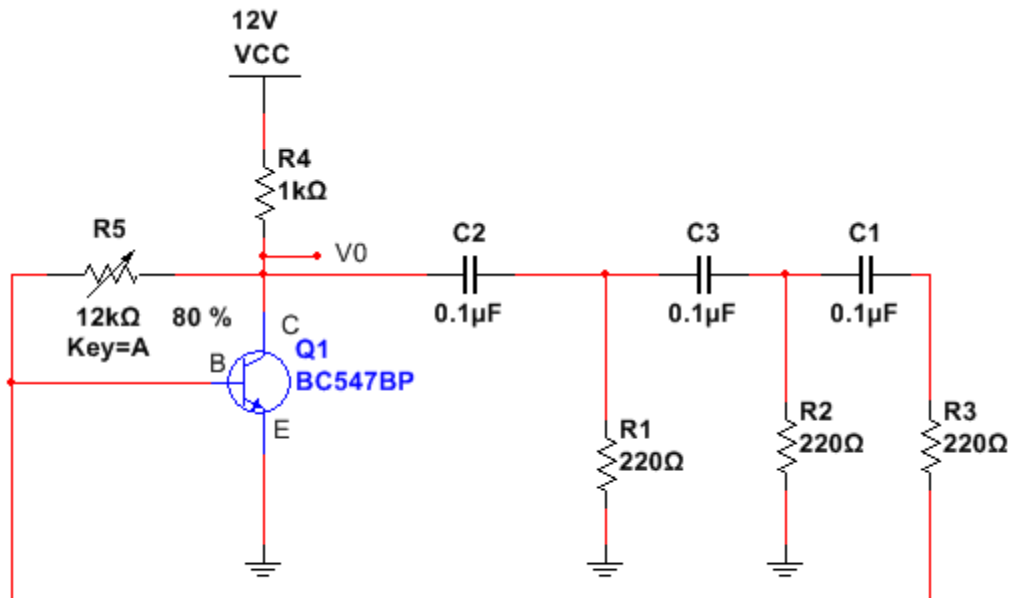
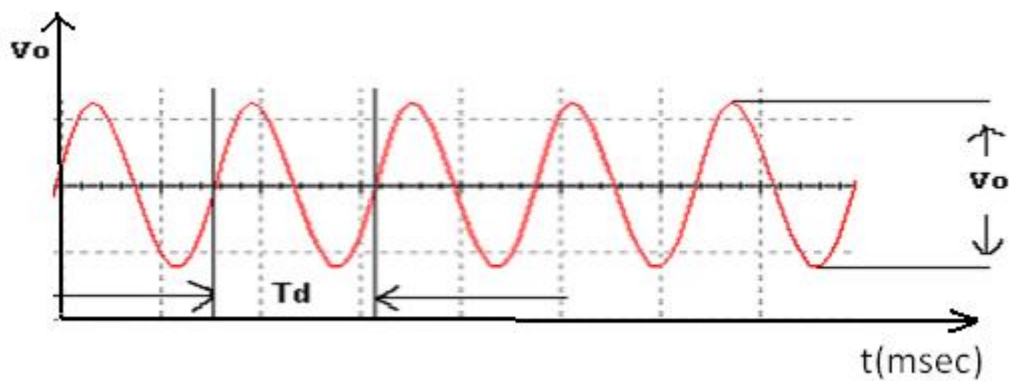


Fig: RC Phase Shift Oscillator

MODELWAVE FORMS:

OUT PUT WAVE FORM :



Exp:

Date:

RC PHASE SHIFT OSCILLATOR

AIM: To design and simulate RC phase shift oscillator using Multisim software and verify practical frequency with theoretical frequency.

SOFTWARE REQUIRED: NI Multisim software 14.1 version.

HARDWARE REQUIRED: Personal Computer

OPERATION:

When the circuit is switched on, current through R3 starts increasing because of biasing. This charging current induces voltage across R2 through C3.

The voltage across R2 leads the voltage across R3 by 60°. Since three R-C sections are provided, therefore, the phase shift circuit produces a total phase shift of $60 \times 3 = 180^\circ$.

A further phase shift of 180° is produced due to the transistor properties. So a total shift of 360 degrees is produced.

Therefore a fraction of the output fed to the input is in phase with it.

The frequency of the transistor RC phase shift oscillator can be expressed by the equation:

$$F = \frac{1}{2\pi RC \sqrt{2N}}$$

Where F is the frequency, R is the resistance, C is the capacitance and N is the number of RC phase shift stages.

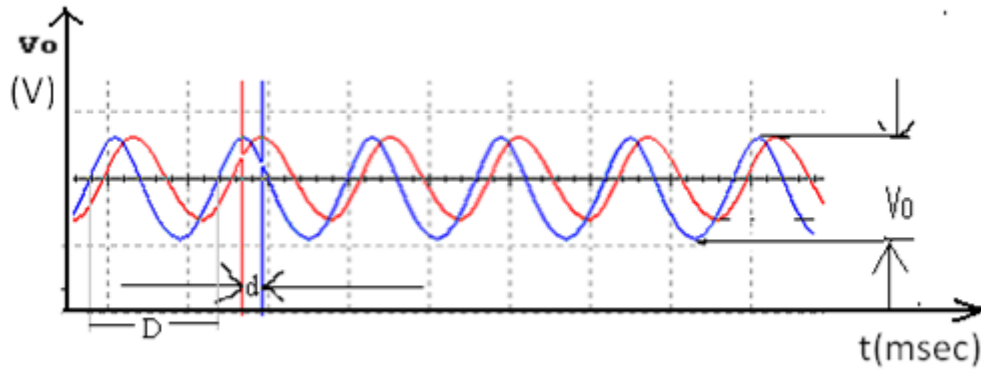
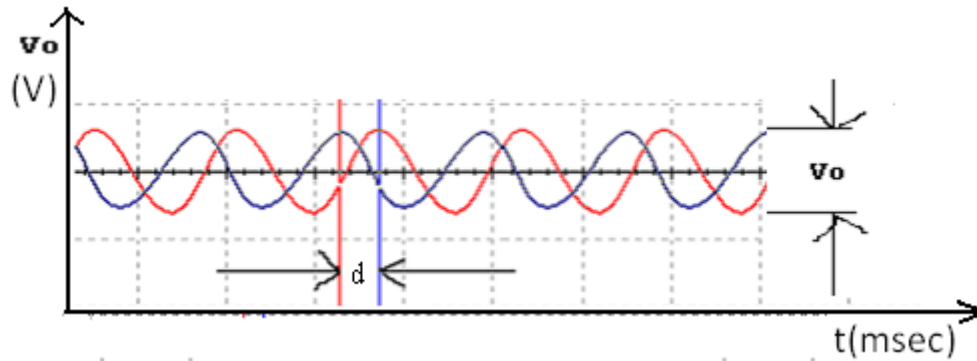
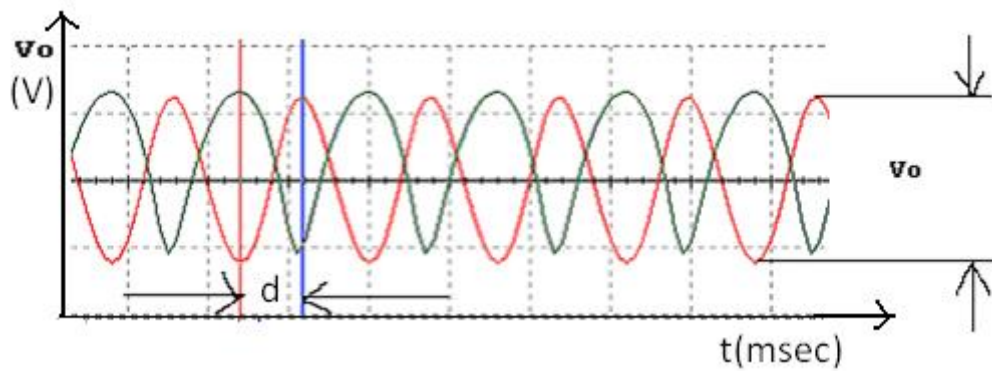
The RC phase shift oscillator can be made variable by making the resistors or capacitors variable. The common approach is to leave the resistors untouched the three capacitors are replaced by a triple gang variable capacitor.

PROCEDURE:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications.
4. Simulate the circuit.
5. Observe and plot the wave form from oscilloscope.
6. Tabulate the frequencies for different combinations of R and C and compare with the theoretical value

$$f = \frac{1}{2\pi RC \sqrt{6+4K}}$$

Where $K = R_3/R$, $R = R_1 = R_2$

MODELWAVE FORMS:OUTPUT WAVEFORM: $\theta = 60^\circ$ OUTPUT WAVEFORM: $\theta = 120^\circ$ OUTPUT WAVEFORM : $\theta = 180^\circ$ **CALCULATIONS:**

RESULT:**CONCLUSION:****VIVA QUESTIONS:**

- 1 What is an Oscillator? Classify the various types of Oscillators?
- 2 What are the constituent parts of an Oscillator?
- 3 What phase angle introduced by ideal and practical RC section for oscillation?
- 4 What is the main difference between an Oscillator and an Amplifier?
- 5 Why three RC networks are necessary for a phase-shift oscillator.

CIRCUIT DIAGRAM:

Inverting Amplifier:

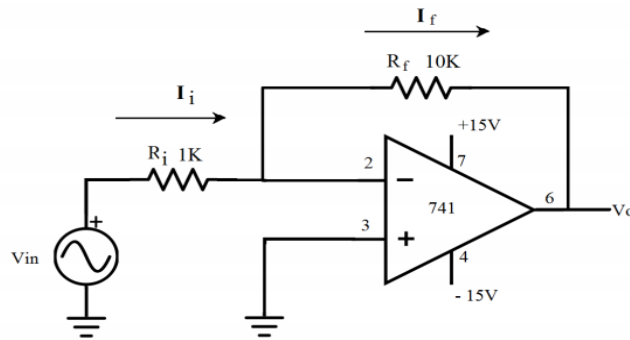


Figure: 1

Non-Inverting Amplifier:

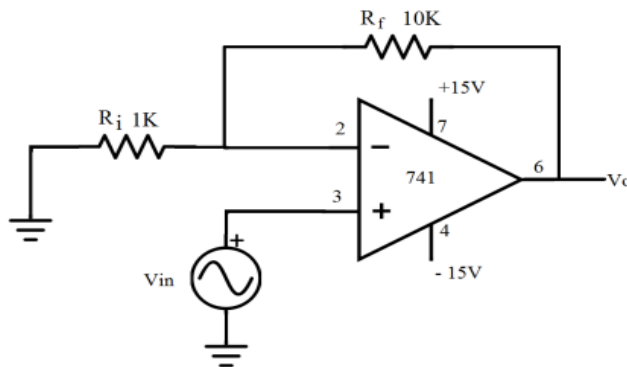
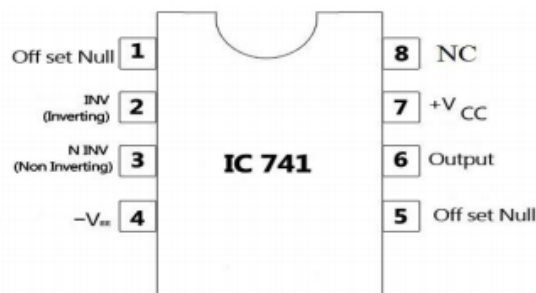


Figure: 2

741 pin diagram



Exp:**Date:**

INVERTING AND NON-INVERTING AMPLIFIERS

AIM: To simulate the following amplifiers using 741 OP-AMP with Multisim software.

- a) An inverting amplifier
- b) A non-inverting amplifier

SOFTWARE REQUIRED: NI Multisim software 14.1 version.

HARDWARE REQUIRED: Personal Computer

OPERATION:

A unity gain amplifier is an electronic amplifier circuit that doesn't amplify. the output voltage in a unity gain amplifier is same as the input voltage.

This means that the op-amp does not provide any amplification to the signal. an op-amp circuit is a Circuit with a very high input impedance. When a circuit has very high input impedance very little current is drawn from circuit.

$$I=V/R$$

Thus the greater the resistance, the less current is drawn from a power source.

PROCEDURE:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar.
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications.
4. Simulate the circuit.
5. Connections are given as per the circuit diagram.
6. + Vcc and - Vcc supply is given to the power supply terminal of the Op-Amp IC.
7. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the non - inverting input terminal of the Op-Amp.
8. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

TABULAR COLUMN:

Inverting Amplifier:

| S. No | Input signal | | | Output signal | | | GAIN=Vo/Vi |
|-------|----------------|------------------|---------------|----------------|------------------|----------------|------------|
| | Amplitude (Vi) | Time period (ms) | Frequency Hz) | Amplitude (Vo) | Time period (ms) | Frequency (Hz) | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

Non-Inverting Amplifier:

| S. No | Input signal | | | Output signal | | | GAIN=Vo/Vi |
|-------|----------------|------------------|---------------|----------------|------------------|----------------|------------|
| | Amplitude (Vi) | Time period (ms) | Frequency Hz) | Amplitude (Vo) | Time period (ms) | Frequency (Hz) | |
| | | | | | | | |
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| | | | | | | | |

MODEL WAVEFORMS:

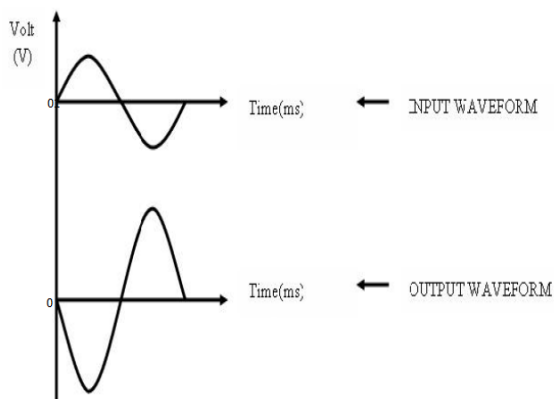


Fig: Inverting Amplifier

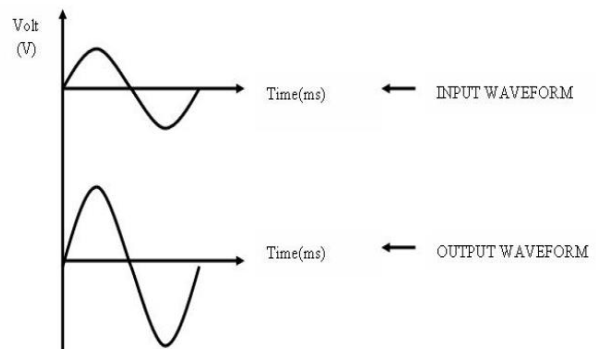
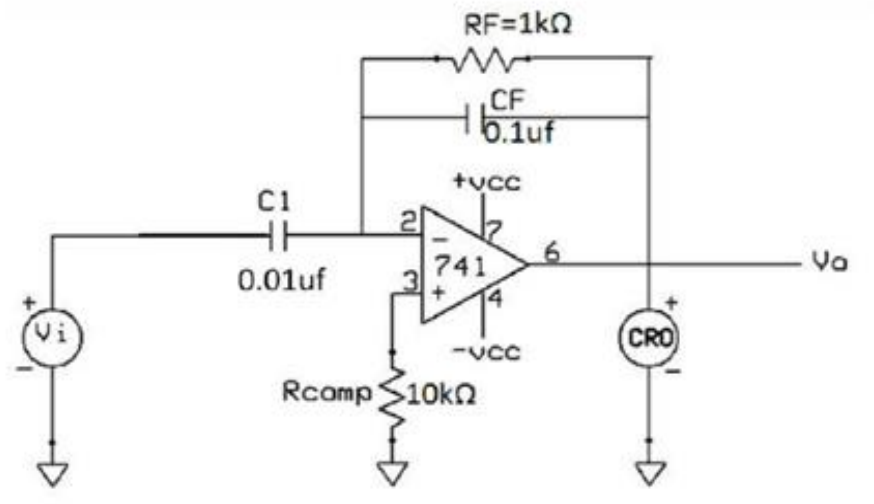
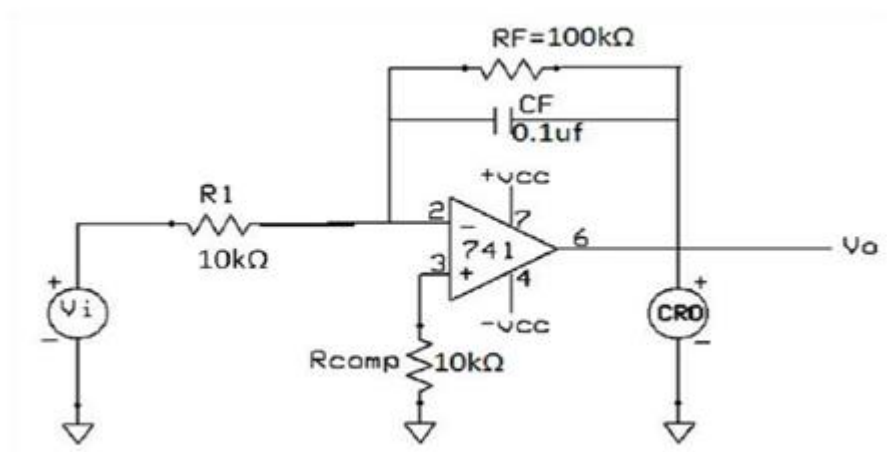


Fig: Non Inverting Amplifier

CIRCUIT DIAGRAM:**DIFFERENTIATOR****INTEGRATOR:**

Exp:**Date:**

INTEGRATOR AND DIFFERENTIATOR

AIM: To design and simulate the characteristics of integrator and differentiator using OP AMP.

SOFTWARE REQUIRED: NI Multisim software 14.1 version.

HARDWARE REQUIRED: Personal Computer

OPERATION:

INTEGRATOR:

As its name implies, the op-amp integrator is an operational amplifier circuit that performs the mathematical representation of integration. That is, we can cause the output v_o to respond to changes in the input voltage over time as the op-amp integrator produces an output voltage which is proportional to the integral of the input voltage.

The formulae for determining the output voltage for integrator is $v_o/dt = -V_{in}/Rc$

Where c = output voltage at start time.

Another application would be to integrate a signal representing water flow, producing a signal representing total quantity of water that has passed by the flow meter.

DIFFERENTIATOR:

One of the simplest of the Op amp circuits that contain a capacitor is the differentiating amplifier or differentiator. As the name suggests, the circuit performs the mathematical operation of differentiation, i.e., the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1 .

The output voltage V_O is equal to R/C_1 times the negative instantaneous rate of change of the input voltage V_{in} with time. Since the differentiator performs the reverse of the integrator's function, a cosine wave input will produce a sine wave output or a triangular input will produce a square wave output.

PROCEDURE:

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component toolbar
2. Using component tool bar place all the components on the circuit window and wire the circuit.
3. Connect the circuit diagram as per the given Specifications.
4. Simulate the circuit.
5. + Vcc and - Vcc supply is given to the power supply terminal of the Op-Amp IC.

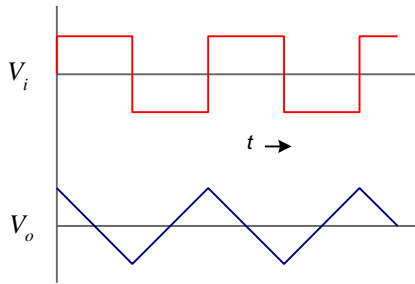
MODEL WAVEFORMS:

Fig 3. Integrator output

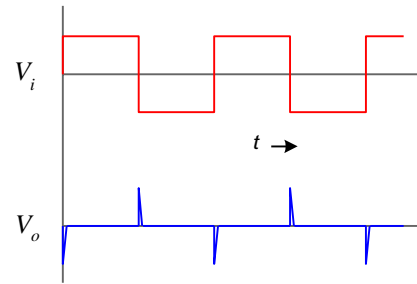


Fig 4. Differentiator output

TABULAR COLUMN:**INTEGRATOR:**

| Sl. No | | Input | Output |
|--------|--|-------|--------|
| 1. | Amplitude (No. of div x Volts per div) | | |
| 2. | Time period (No. of div x Time per div) | | |

DIFFERENTIATOR:

| Sl. No | | Input | Output |
|--------|--|-------|--------|
| 1. | Amplitude (No. of div x Volts per div) | | |
| 2. | Time period (No. of div x Time per div) | | |

6. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. Why an integrator cannot be using low pass rc circuit?
2. What is ic741?
3. Why op-amp is called 741?
4. Why resistor is shunted across feedback capacitor in the practical integrator?
5. What is the symbol of op-amp?

PART -A

HARDWARE EXPERIMENTS

CIRCUIT DIAGRAM:

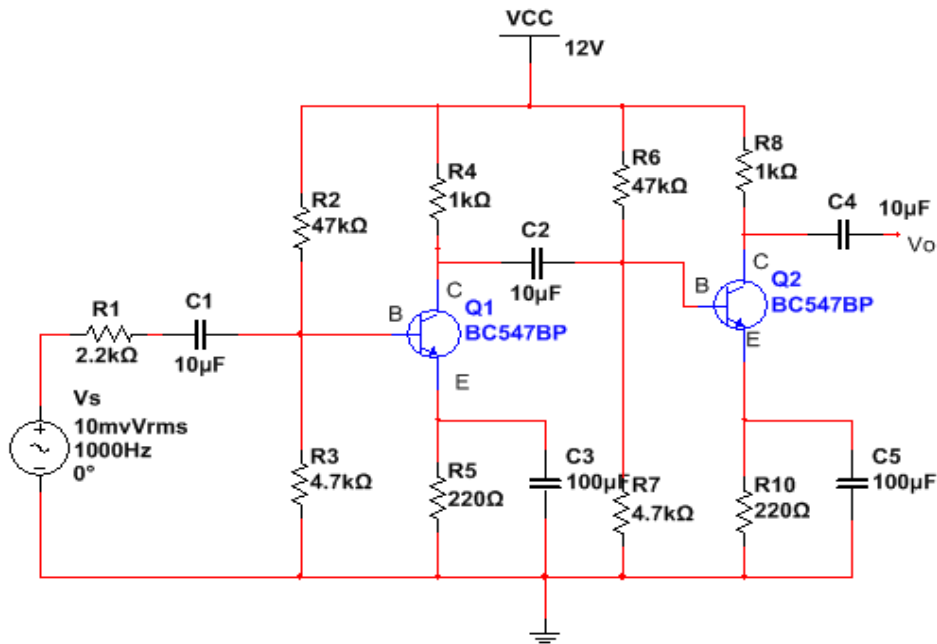
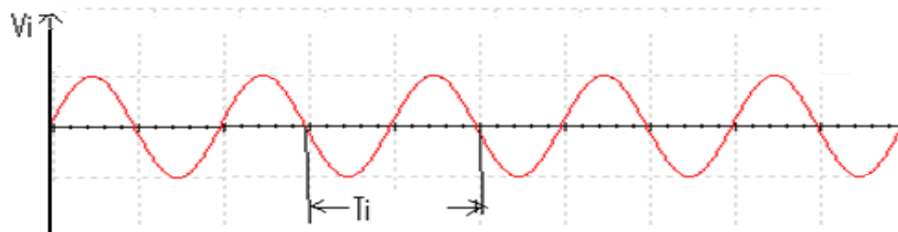


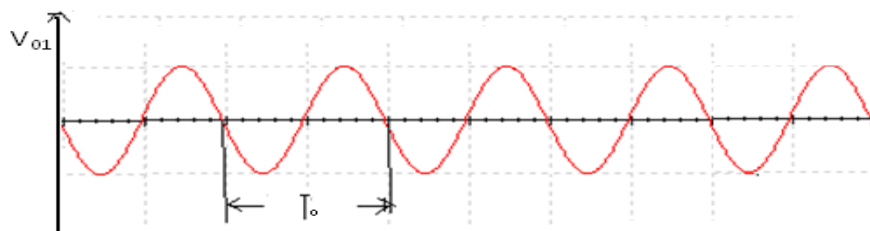
Fig: Two Stage RC Coupled Amplifier

MODELGRAPH:-

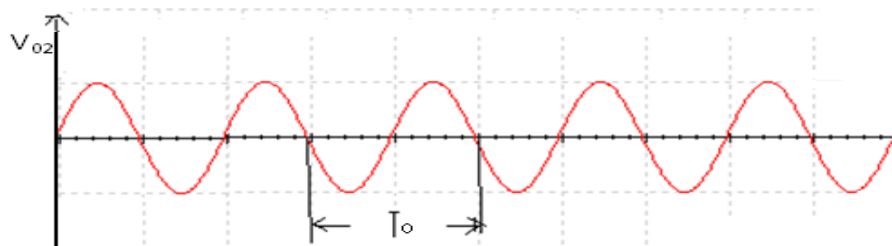
INPUT WAVE FORM:



FIRST STAGE OUTPUT:



SECOND STAGE OUTPUT:



Exp:

Date:

TWO STAGE RC COUPLED AMPLIFIER**AIM:** To design and verify two stages RC coupled amplifier and determine bandwidth.**APPARATUS:**

| S.NO | APPARATUS | RANGE | QUANTITY |
|------|--------------------|-------------|----------|
| 1 | Transistor | BC547 | 2 |
| 2 | Resistors | 47k | 2 |
| | | 1k | 2 |
| | | 4.7k | 2 |
| | | 2.2k | 1 |
| 3 | Capacitors | 220 | 2 |
| | | 10 μ F | 3 |
| | | 100 μ F | 2 |
| 4 | RPS | 0-30V | 1 |
| 5 | Function Generator | 0-3MHz | 1 |
| 6 | CRO | 30MHz | 1 |
| 7 | Bread board | - | 1 |
| 8 | Connecting wires | - | REQUIRED |

OPERATION:

When input AC. signal is applied to the base of the transistor of the 1st stage of RC coupled amplifier, from the function generator, it is then amplified across the output of the 1st stage. This amplified voltage is applied to the base of next stage of the amplifier, through the coupling capacitor. Count where it is further amplified and reappears across the output of the second stage.

Thus the successive stages amplify the signal and the overall gain is raised to the desired level. Much higher gain can be obtained by connecting a number of amplifier stages in succession. Resistance-capacitance (RC) coupling in amplifiers are most widely used to connect the output of first stage to the input (base) of the second stage and so on. This type of coupling is most popular because it is cheap and provides a constant amplification over a wide range of frequencies.

PROCEDURE:

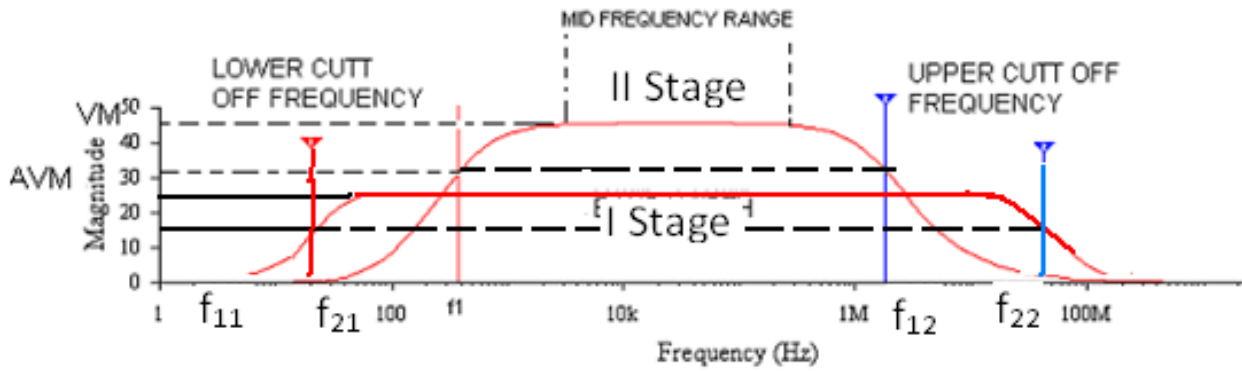
1. Connect the circuit as shown in circuit diagram.
2. Apply the source voltage of 20mV peak-to-peak at 1 KHz frequency using Function Generator and note down input voltage.
3. Measure the Output Voltage V_o (p-p) for various frequency values.
4. The voltage gain can be calculated by using the expression: $A_v = (V_o/V_i)$
5. All the readings are tabulated and voltage gain in dB is calculated by Using The expression $A_v = 20 \log_{10} (V_o/V_i)$
6. A graph is drawn by taking frequency on x-axis and gain in dB on y-axis On Semi-log graph.

The Band Width of the amplifier is calculated from the graph Using the expression,

$$\text{Bandwidth, BW} = f_2 - f_1,$$

$$\text{Gain Bandwidth product} = 3\text{-dB midband gain} \times \text{Bandwidth}$$

FREQUENCY RESPONSE:



TABULAR COLUMN: $V_s=20\text{mv}$

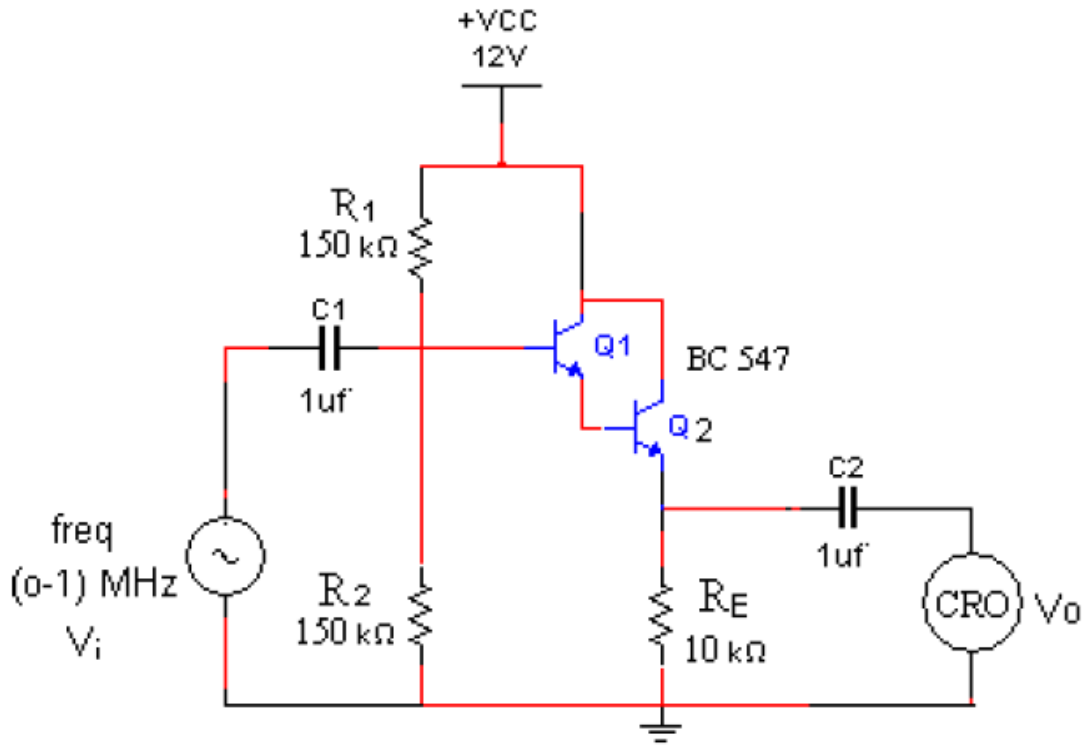
| S.NO | FREQUENCY(Hz) | OUTPUT VOLTAGE (V_o) | | GAIN (V_o/V_i) | | GAIN IN dB $A_v=20 \log_{10} (V_o/V_i)$ | |
|------|---------------|--------------------------|----------|--------------------|----------|--|----------|
| | | V_{o1} | V_{o2} | A_{v1} | A_{v2} | A_{v1} | A_{v2} |
| | | | | | | | |

RESULT:**CONCLUSION:****VIVA QUESTIONS:**

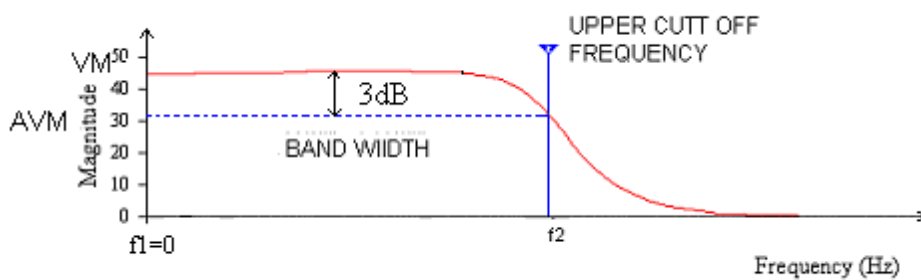
1. What are the advantages and disadvantages of multi-stage amplifiers?
2. Why gain falls at HF and LF?
3. Why the gain remains constant at MF?
4. Explain the function of emitter bypass capacitor, CE?
5. How the band width will effect as more number of stages are cascaded?

CIRCUIT DIAGRAM:

Darlington Amplifier



MODEL WAVE FORM:



Darlington Pair

Exp:**Date:****DARLINGTON PAIR****AIM:** To obtain the frequency response of Darlington pair and determine bandwidth.**APPARATUS:**

| S.NO | APPARATUS | RANGE | QUANTITY |
|------|--------------------|-------------------------------|----------|
| 1 | Transistor | BC 547 | 2 |
| 2 | Resistors | 100K Ω 10K Ω | 2 1 |
| 3 | Capacitor | 1 μ F | 2 |
| 4 | Function Generator | 0-30MHz | 1 |
| 5 | RPS | 0-30V | 1 |
| 6 | CRO | 30MHz | 1 |
| 7 | Bread Board | - | 1 |
| 8 | Connecting Wires | - | REQUIRED |

OPERATION:

A Darlington transistor pair comprises of a couple of bipolar transistors that are coupled in order to deliver a very high-current gain from a low-base current.

It is cascading of common collector-common collector. In this circuit, the emitter of the input transistor is connected to the base terminal of the output transistor.

Therefore, the current that is amplified by the first transistor is again amplified by the second transistor.

The current gain of single stage cc amplifier is high,so by using darlington pair we can get high current gain.

PROCEDURE:

1. Design the circuit for given specifications and connect the circuit.
2. Apply input signal to the circuit of 1.5V_{p-p}, 1 KHz sine wave from the function generator with DC offset ON.
3. Tabulate amplitude of output signal with change in frequency with steps from 10Hz to 1MHz and determine gain using $A_v = V_o/V_s$.
4. Calculate voltage gain in dB using $A_v = 20 \log_{10}(V_o/V_s)$.
5. Plot the frequency response on semi-log graph using the values of amplitude in dB vs frequency in Hz.
6. Calculate the bandwidth using $BW = f_2 - f_1$.

PRECUATIONS:

1. DC offset should be ON, to avoid clipping.

TABULAR COLUMN: $V_i=1.5V$

| S.NO | FREQUENCY(Hz) | OUTPUT VOLTAGE (V) | GAIN (V_0/V_s) | GAIN IN dB $A_v=20 \log_{10} (V_0/V_s)$ |
|------|---------------|--------------------|--------------------|--|
| | | | | |

RESULT:**CONCLUSION:****VIVA QUESTIONS:**

1. What is a Darlington pair?
2. What is the advantage of Darlington configuration?
3. Give few applications of Darlington amplifier
4. Why does amplifier gain reduce at high frequencies?
5. State the types of distortions in amplifier.

CIRCUIT DIAGRAM:

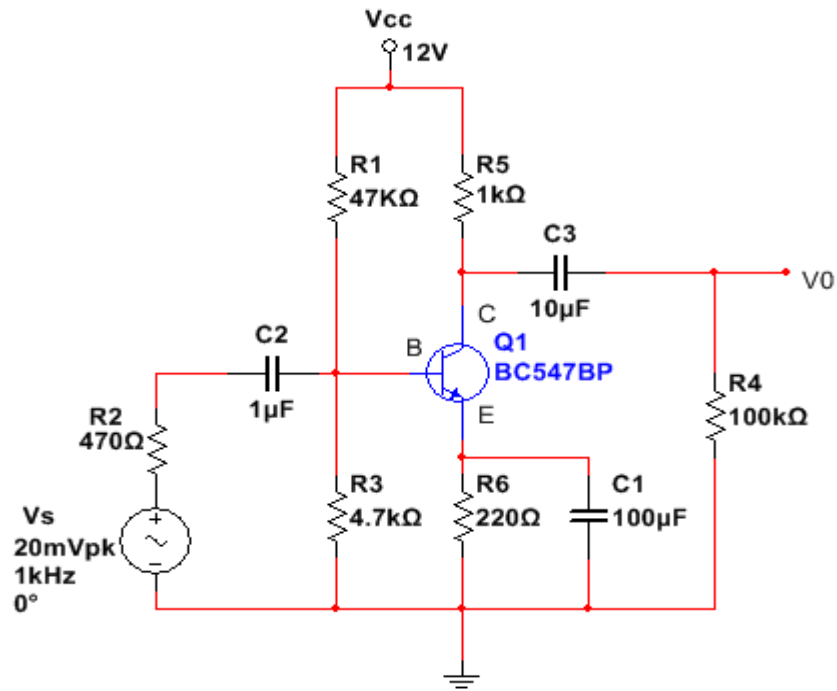
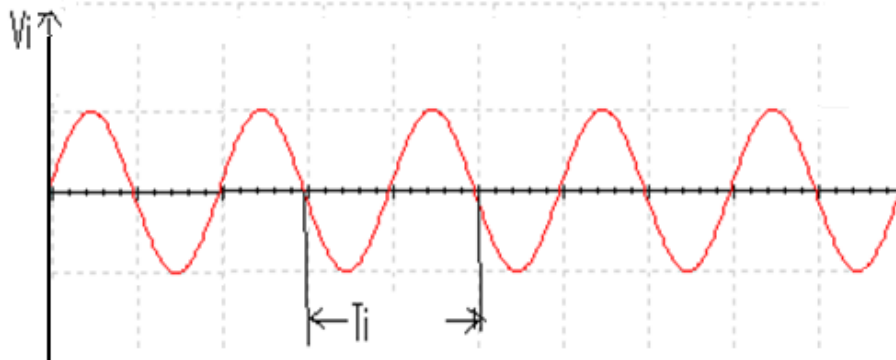
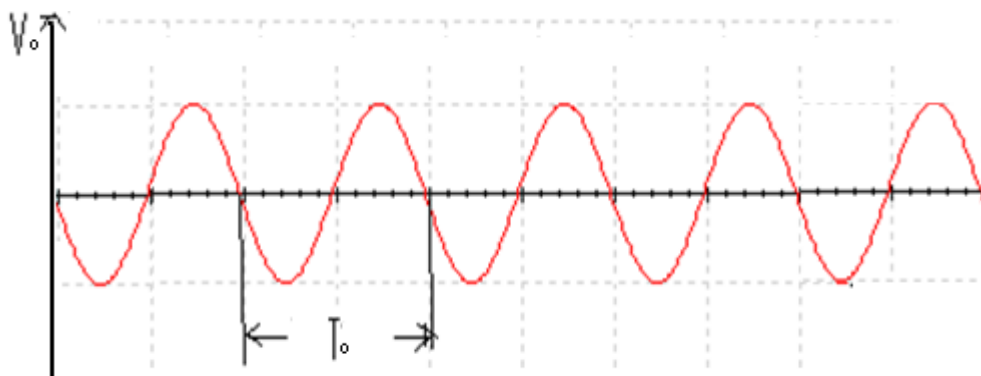


Fig: Voltage series feedback Amplifier

INPUT WAVE FORM:



OUTPUT WAVE FORM:



Exp:

Date:

VOLTAGE SERIES FEEDBACK AMPLIFIER

AIM: To find the gain and bandwidth of the Voltage Series feedback amplifier with & without feedback

APPARATUS:

| S.NO | APPARATUS | RANGE | QUANTITY |
|------|---------------------|--------|----------|
| 1 | Transistor(BC547BP) | - | 1 |
| 2 | Resistors | 470Ω | 1 |
| | | 47kΩ | 1 |
| | | 100KΩ | 1 |
| | | 220Ω | 1 |
| | | 1KΩ | 1 |
| | | 4.7KΩ | 1 |
| 3 | Capacitors | 1μF | 1 |
| | | 10μF | 1 |
| | | 100μF | 1 |
| 4 | RPS | 0-30V | 1 |
| 5 | Function Generator | 0-3MHz | 1 |
| 6 | CRO | 30MHz | 1 |
| 7 | Bread board | - | 1 |
| 8 | Connecting wires | - | Required |

OPERATION:

The fraction of output voltage is applied in series with input voltage through feedback circuit. Feedback circuit shunt the output but in series with input. So the output impedance is decreased while input impedance is increased. The input & output impedance of an ideal voltage series feedback amplifier is infinite & zero respectively. The resistor R_E is used to provide necessary biasing for the amplifier with voltage series feedback gain of the amplifier decreases

PROCEDURE:

1. Connect the circuit as shown in circuit diagram.
2. Apply the source voltage of 20mV peak-to-peak at 1 KHz frequency using Function Generator and note down input voltage.
3. Measure the Output Voltage V_o (p-p) for various frequency values.
4. The voltage gain can be calculated by using the expression: $A_v = (V_o/V_i)$
5. All the readings are tabulated and voltage gain in dB is calculated by Using The expression $A_v = 20 \log_{10} (V_o/V_i)$
6. A graph is drawn by taking frequency on x-axis and gain in dB on y-axis On Semi-log graph. The Band Width of the amplifier is calculated from the graph Using the expression,

RESULT:**CONCLUSION:****VIVA QUESTIONS:**

1. What do you understand by feedback in amplifiers?
2. Explain the terms feedback factor and open loop gain?
3. What are the types of feedback?
4. Explain the basic concept of feedback?
5. Compare the negative feedback and positive feedback?

CIRCUIT DIAGRAM:

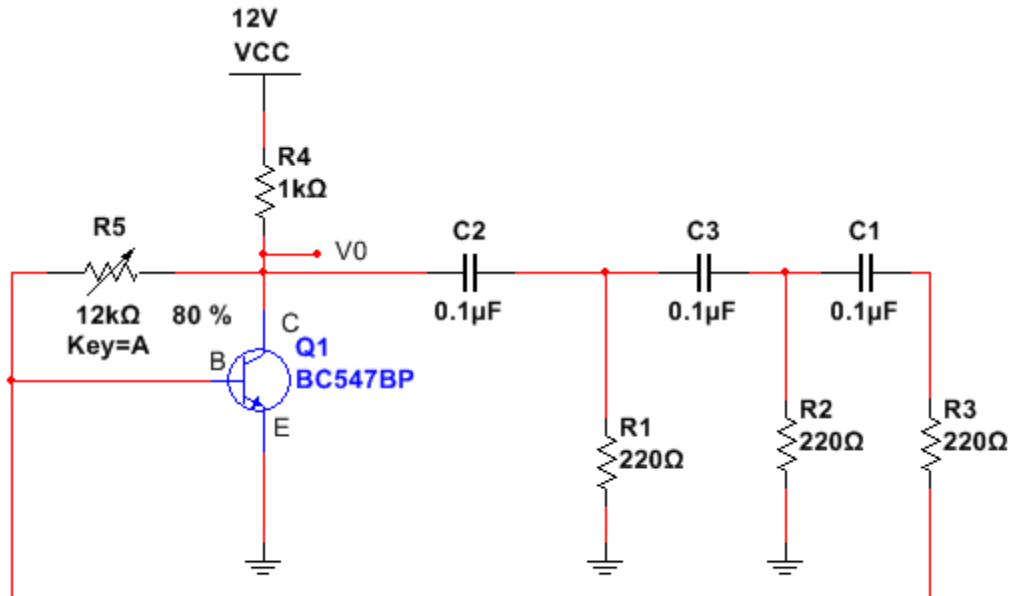
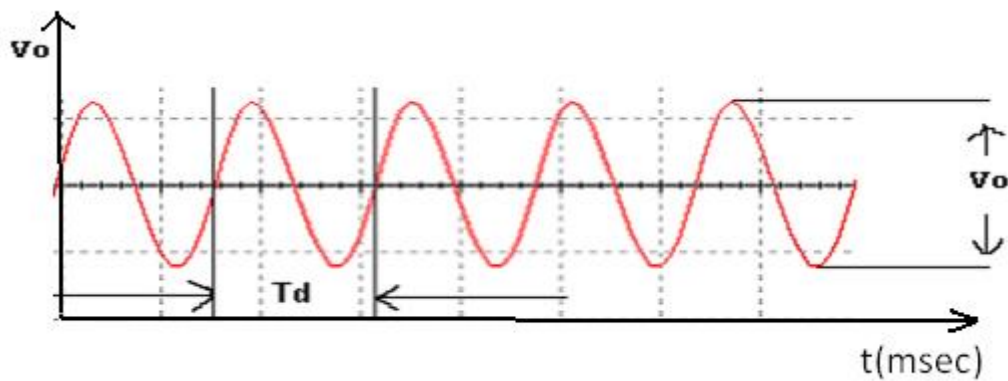


Fig: RC Phase shift Oscillator

MODELWAVE FORMS:

OUT PUT WAVE FORM :



Exp:

Date:

RC PHASE SHIFT OSCILLATOR

AIM: To design a RC phase shift oscillator and verify practical frequency with theoretical Frequency.

APPARATUS:

| S.NO | APPARATUS | RANGE | QUANTITY |
|------|---------------------|-------------|----------|
| 1 | TRANSISTOR(BC547BP) | - | 2 |
| 2 | Resistors | 220Ω 1KΩ | 3 1 |
| 3 | Capacitors | 0.1μF | 3 1 |
| 4 | DIB | 12kΩ | 1 |
| 5 | DCB | - | |
| 6 | RPS | 0-30V | 1 |
| 7 | CRO | 30MHz | 1 |
| 8 | Bread Board | - | 1 |
| 9 | Connecting Wires | - | Required |

OPERATION:

When the circuit is switched on, current through R3 starts increasing because of biasing. This charging current induces voltage across R2 through C3.

The voltage across R2 leads the voltage across R3 by 60°. since three R-C sections are provided, therefore, the phase shift circuit produces a total phase shift of $60 \times 3 = 180^\circ$.

A further phase shift of 180° is produced due to the transistor properties. So a total shift of 360° degrees is produced.

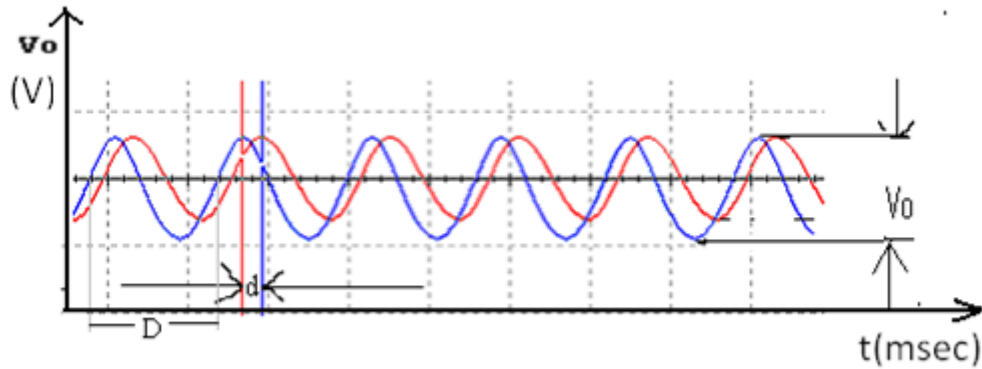
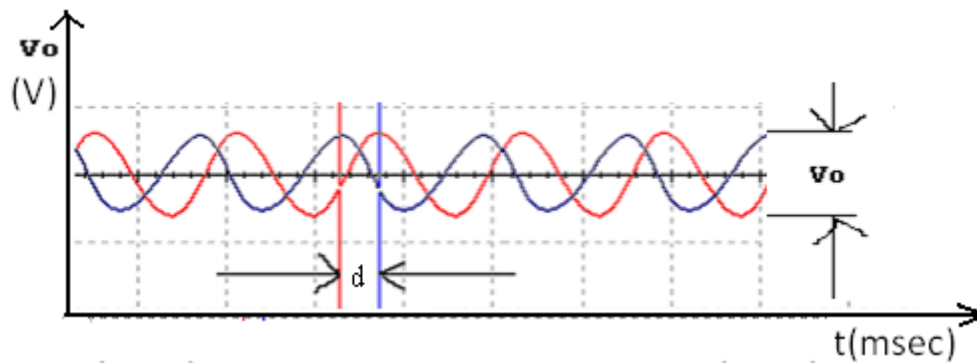
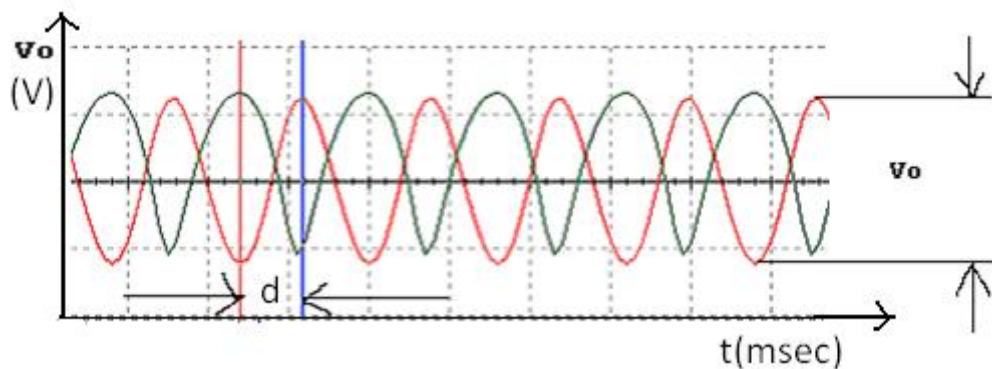
Therefore a fraction of the output fed to the input is in phase with it.

The frequency of the transistor RC phase shift oscillator can be expressed by the equation:

$$F = \frac{1}{2\pi RC\sqrt{2N}}$$

Where F is the frequency, R is the resistance, C is the capacitance and N is the number of RC phase shift stages.

The RC phase shift oscillator can be made variable by making the resistors or capacitors variable. The common approach is to leave the resistors untouched the three capacitors are replaced by a triple gang variable capacitor.

MODEL WAVE FORMS:**OUTPUT WAVEFORM: $\theta = 60^\circ$** **OUTPUT WAVEFORM: $\theta = 120^\circ$** **OUTPUT WAVEFORM : $\theta = 180^\circ$** **CALCULATIONS:**

PROCEDURE:

1. Connect the circuit diagram as shown in the figure
2. Set $V_{CC} = 12V$
3. Keep the capacitance of the decade capacitance box to $0.1\mu F$, and measure the generated output signal amplitude and frequency from CRO.
4. Vary the Inductance in steps and note down frequency and amplitude at each.
5. Plot the graph from CRO and verify the practical frequency with theoretical frequency.

RESULT:**CONCLUSION:****VIVA QUESTIONS:**

1. What is the necessity of cascading?
2. What is 3dB bandwidth?
3. Why RC coupling is preferred in audio range?
4. Which type of coupling is preferred and why?
5. Explain various types of Capacitors?

CIRCUIT DIAGRAM:

Inverting Amplifier:

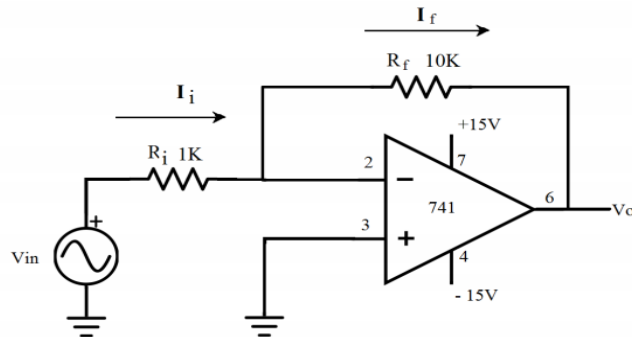


Figure: 1

Non-Inverting Amplifier:

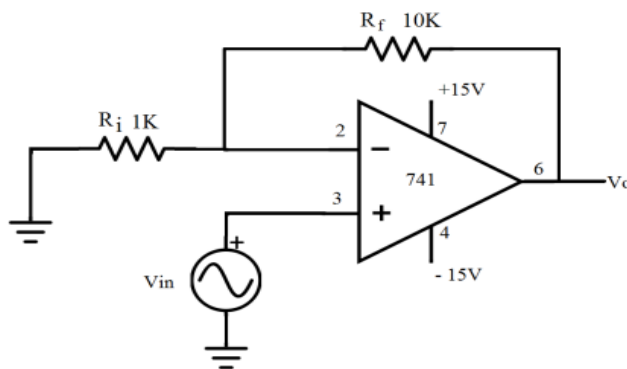
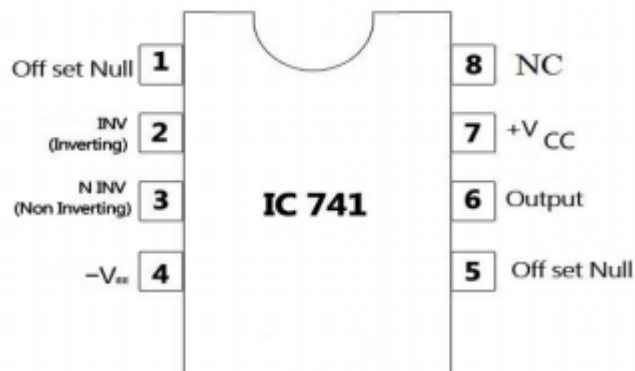


Figure: 2

741 pin diagram



Exp:**Date:****INVERTING AND NON-INVERTING AMPLIFIERS****AIM:** To study and design the following amplifiers using 741 OP-AMP

- a. An inverting amplifier
- b. A non-inverting amplifier

APPARATUS:

| S.NO | Equipment/Component name | Specifications/Value | QUANTITY |
|------|--------------------------|--------------------------------|----------|
| 1 | Resistor | 1k Ω , 10k Ω | 1 |
| 2 | IC | 741 | 1 |
| 3 | Fixed Power supply | (+/- 15)V | 1 |
| 4 | Function Generator | (0 – 3MHz), 20V _{p-p} | 1 |
| 5 | Cathode Ray Oscilloscope | 20MHz | 1 |
| 6 | Connecting wires | | - |

OPERATION:

A unity gain amplifier is an electronic amplifier circuit that doesn't amplify. the output voltage in a unity gain amplifier is same as the input voltage.

This means that the op-amp does not provide any amplification to the signal. an op-amp circuit is a Circuit with a very high input impedance. When a circuit has very high input impedance very little current is drawn from circuit.

$$I=V/R$$

Thus the greater the resistance, the less current is drawn from a power source.

PROCEDURE:**Inverting Amplifier**

1. Connect the circuit as shown in figure: 1.
2. Apply a Sine wave of 5V_{P-P} at 1 KHz frequency at the inverting terminal.
3. Study the effect of slew rate.
4. Observe the output waveform
5. Plot the waveform on a graph.

TABULAR COLUMN:

Inverting Amplifier:

| S. No | Input signal | | | Output signal | | | GAIN=Vo/Vi |
|-------|----------------|------------------|----------------|----------------|------------------|----------------|------------|
| | Amplitude (Vi) | Time period (ms) | Frequency (Hz) | Amplitude (Vo) | Time period (ms) | Frequency (Hz) | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

Non-Inverting Amplifier:

| S. No | Input signal | | | Output signal | | | GAIN=Vo/Vi |
|-------|----------------|------------------|----------------|----------------|------------------|----------------|------------|
| | Amplitude (Vi) | Time period (ms) | Frequency (Hz) | Amplitude (Vo) | Time period (ms) | Frequency (Hz) | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

MODEL WAVEFORMS:

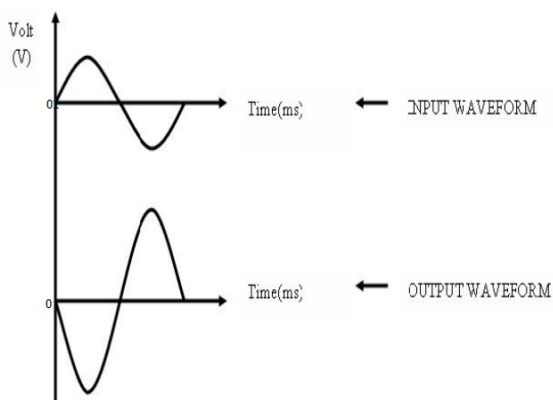


Fig: Inverting Amplifier

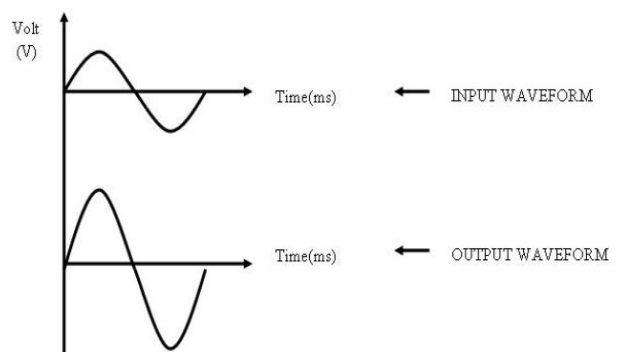


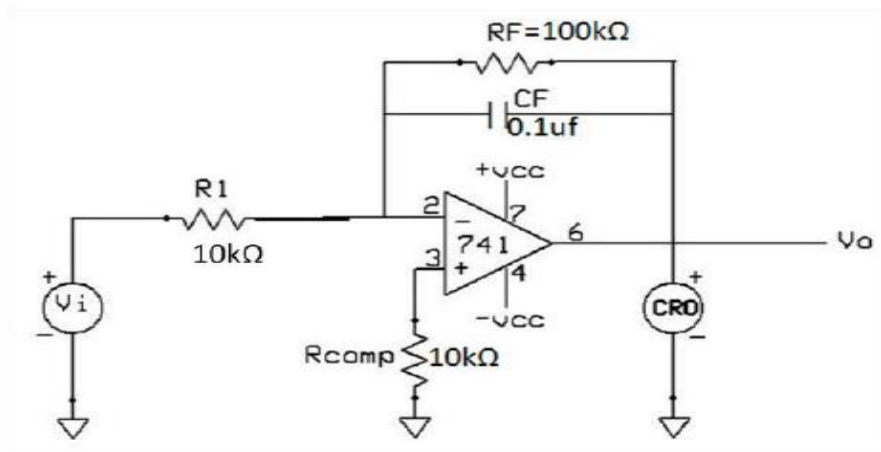
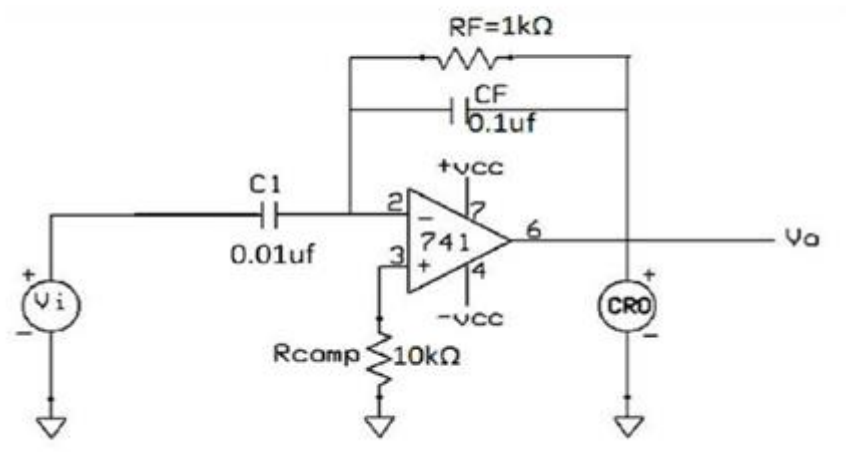
Fig: Non Inverting Amplifier

Non-Inverting Amplifier

1. Connect the circuit as shown in figure: 2.
2. Apply a Sine wave of $5V_{P-P}$ at 1 KHz frequency at the non-inverting terminal.
3. Study the effect of slew rate.
4. Observe the output waveform
5. Plot the waveform on a graph.

RESULT:**CONCLUSION:****VIVA QUESTIONS:**

1. How does negative feedback modify the gain of amplifier?
2. What are the advantages of negative feedback amplifier?
3. What is positive and negative feedback amplifier?
4. What are types of feedback amplifiers?
5. What is feedback gain?

CIRCUIT DIAGRAM:**INTEGRATOR:****DIFFERENTIATOR:**

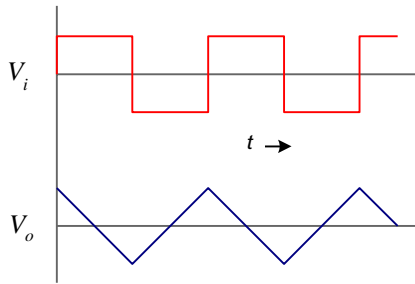
MODEL WAVEFORMS:

Fig 3. Integrator output

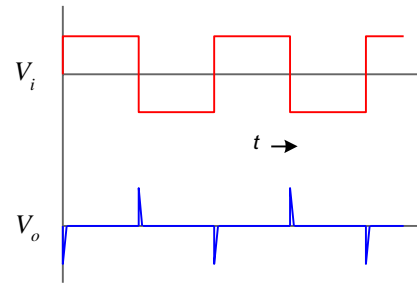


Fig 4. Differentiator output

TABULAR COLUMN:**INTEGRATOR:**

| Sl. No | | Input | Output |
|--------|--|-------|--------|
| 1. | Amplitude (No. of div x Volts per div) | | |
| 2. | Time period (No. of div x Time per div) | | |

Exp No:

Date:

INTEGRATOR AND DIFFERENTIATOR**AIM:** To design and study the characteristics of integrator and differentiator.**APPARATUS:**

| S.NO | Equipment/Component name | Specifications/Value | Quantity |
|------|--------------------------|--|----------|
| 1 | Capacitors | 0.1 μ f,0.01 μ f | 1 |
| 2 | Resistor | 1k Ω ,10k Ω ,100k Ω | 1 |
| 3 | IC | 741 | 1 |
| 4 | Regulated Power supply | (0 – 10)V | 1 |
| 5 | Function Generator | (0 – 3MHz), 20V _{p-p} | |
| 6 | Cathode Ray Oscilloscope | 20MHz | 1 |
| 7. | Connecting wires | | - |

OPERATION:**INTEGRATOR:**

As its name implies, the op-amp integrator is an operational amplifier circuit that performs the mathematical representation of integration. That is, we can cause the output v_o to respond to changes in the input voltage over time as the op-amp integrator produces an output voltage which is proportional to the integral of the input voltage.

The formulae for determining the output voltage for integrator is $v_o = -\int V_{in}/R_c dt$

Where c = output voltage at start time.

Another application would be to integrate a signal representing water flow, producing a signal representing total quantity of water that has passed by the flow meter.

DIFFERENTIATOR:

One of the simplest of the Op amp circuits that contain a capacitor is the differentiating amplifier or differentiator. As the name suggests, the circuit performs the mathematical operation of differentiation, i.e., the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1 .

The output voltage V_O is equal to $1/R_1 C_1$ times the negative instantaneous rate of change of the input voltage V_{in} with time. Since the differentiator performs the reverse of the integrator's function, a cosine wave input will produce a sine wave output or a triangular input will produce a square wave output.

DIFFERENTIATOR:

| Sl. No | | Input | Output |
|--------|--|-------|--------|
| 1. | Amplitude (No. of div x Volts per div) | | |
| 2. | Time period (No. of div x Time per div) | | |

PROCEDURE:

1. Connect the circuit as shown in figure:1
2. Apply the power supplies as $V_{CC} = +12V$ and $V_{EE} = -12V$.
3. Apply square wave input at 1KHz and 2Vp-p amplitude, choose the time period of the signal
 $T \geq R_F C_F$
4. Observe integrator output at terminal V_o .
5. Plot the input and output waveforms.

PRECAUTIONS:

1. Connections should be made properly.
2. Avoid loose connections.

RESULT:**CONCLUSION:**

VIVA QUESTIONS:

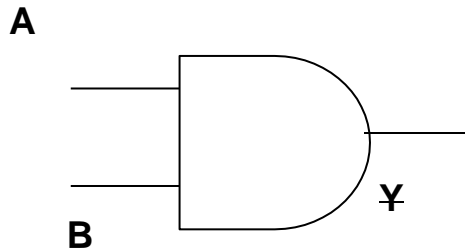
1. Why an integrator cannot be using low pass rc circuit?
2. What is ic741?
3. Why op-amp is called 741?
4. Why resistor is shunted across feedback capacitor in the practical integrator?
5. what is the symbol of op-amp?

PART B
DIGITAL IC'S

LOGIC GATES

TRUTH TABLES

AND GATE:

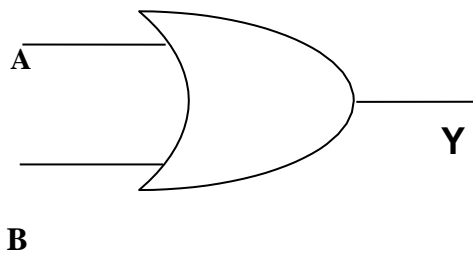


$Y = A . B$

74 LS 08

| Input s | | Output |
|------------|---|--------|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

OR GATE:

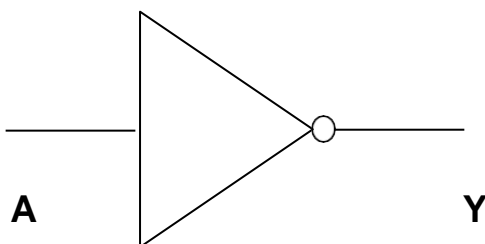


$Y = A + B$

74 LS 32

| Input s | | Output |
|------------|---|--------|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

NOT GATE:



$Y = A'$

74 LS 04

| Input | Output |
|-------|--------|
| A | Y |
| 0 | 1 |
| 1 | 0 |

Exp No:

Date:

VERIFICATION OF LOGIC GATES**AIM:** To verify the truth tables of different logic gates..**APPARATUS:**

| S.NO | APPARATUS | RANGE | QUANTITY |
|------|----------------------------|---|----------|
| 1 | IC's | 74LS08, 74LS32, 74LS04, 74LS00, 74LS02, 74LS86 | 1 |
| 2 | Light Emitting Diode (LED) | | 1 |
| 3 | Bread board | | 1 |
| 4 | Connecting wires | | REQUIRED |
| 5 | Fixed Power Supply | (0-5V) | 1 |

OPERATION:

Binary Logic gates consist of Binary variables and logical operations. The variables are designated by letters of alphabets such as A, B, C or X, Y, Z With variables having two and only two distinct possible values 0 and 1.

AND: This operation is represented as 'dot'. The IC number of AND gate is 74LS08. The output of logical operation AND is 1 if and only if both inputs are 1 in all other cases it is 0.

$$Z = A \cdot B$$

OR: This operation is represented as 'plus'. The IC number of OR gate is 74LS32. The output of logical operation OR is 1 if any one of the input is 1. If both the inputs are 0, the output is 0.

$$Z = A + B$$

NOT: This operation is represented by a 'bubble' before a common gate. The IC number of NOT gate is 74LS04. The output NOT gate is 1 if the input is 0 and viceversa

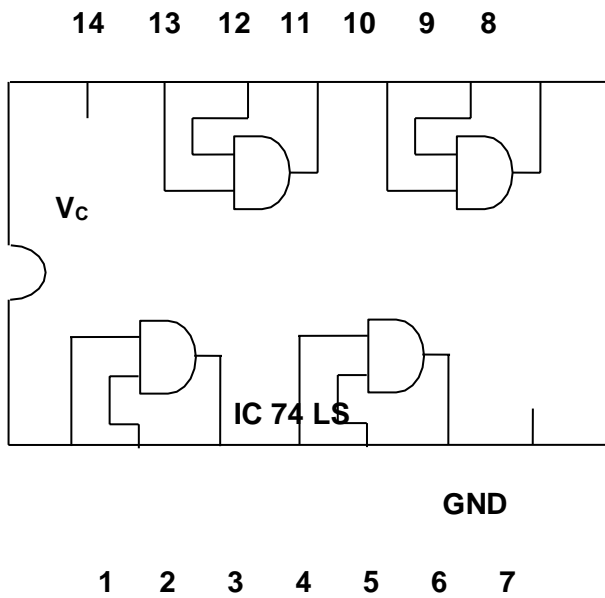
$$Z = A'$$

PROCEDURE:

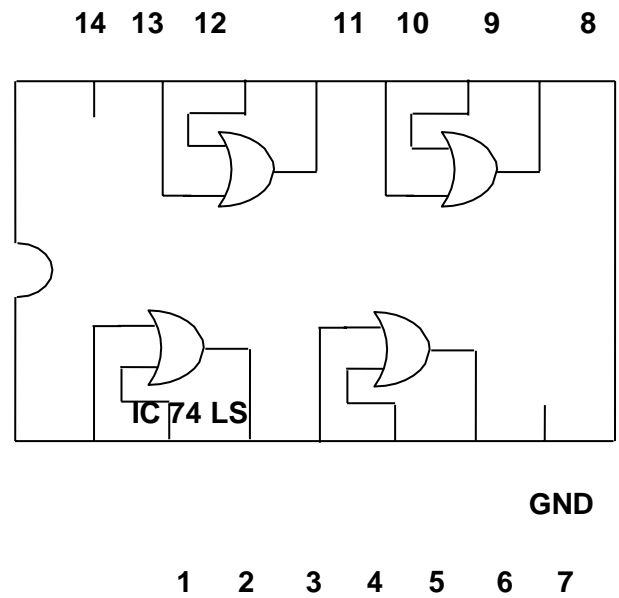
1. The IC's are placed on the bread board.
2. A voltage of +5V is applied to pin no.14 and -Ve is applied to pin no.7.
3. Inputs and Outputs are connected according the gates which are taken.
4. For the input 1 we have to connect the input terminal to +5V and for 0 to -Ve.
5. Output is verified in LED. If the LED is ON the output is 1, if OFF it is 0.
6. According to the Logic gates truth table we have to verify the inputs and outputs.

PIN DETAILS OF GATES:

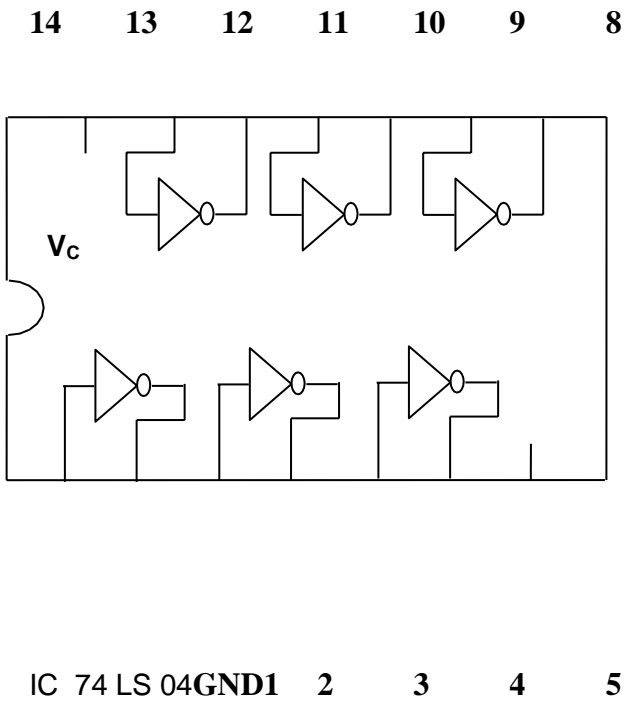
AND GATE



OR GATE



NOT GATE



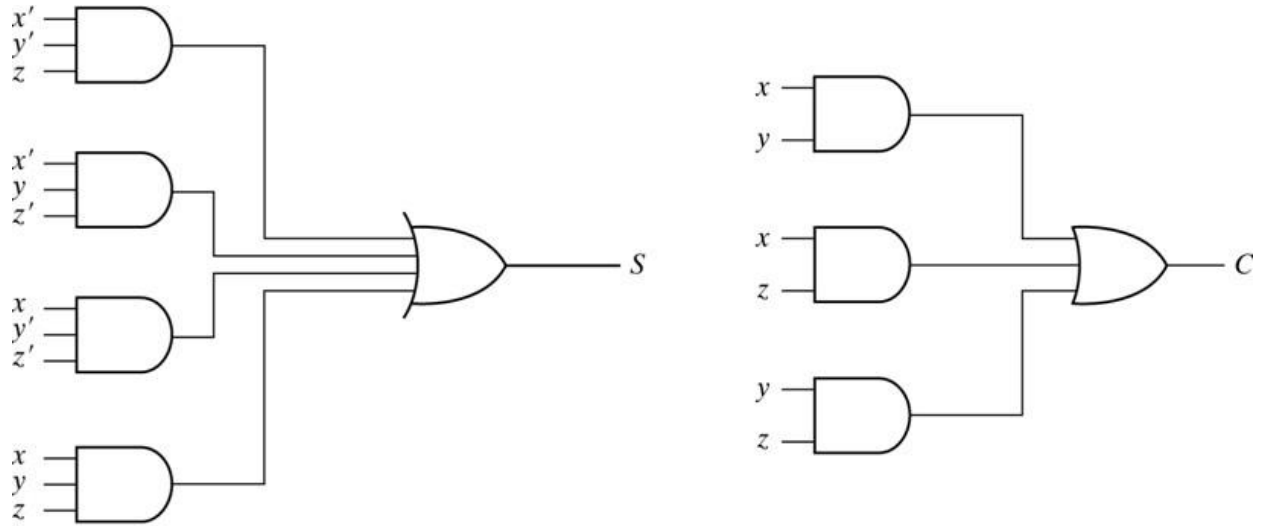
RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What are the 7 logic gates?
2. What do you mean by logic gates?
3. What are used to complement logic gates?
4. What is the principle of logic gates?
5. Who invented logic gates?

CIRCUIT DIAGRAM:



Implementation of Full Adder in Sum of Products

TRUTH TABLE

| X | Y | Z | Sum (S) | Carry (C) |
|---|---|---|---------|-----------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Exp No:

Date:

FULL ADDER**AIM:** To verify the truth tables of Full Adder.**APPARATUS:**

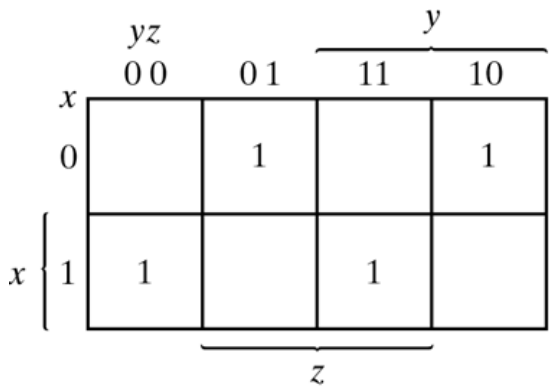
| S.NO | APPARATUS | RANGE | QUANTITY |
|------|----------------------------|---|----------|
| 1 | IC's | 74LS08, 74LS32, 74LS04, 74LS00, 74LS02, 74LS86 | 1 |
| 2 | Light Emitting Diode (LED) | | 1 |
| 3 | Bread board | | 1 |
| 4 | Connecting wires | | REQUIRED |
| 5 | Fixed Power Supply | (0-5V) | 1 |

OPERATION:**Full adder**

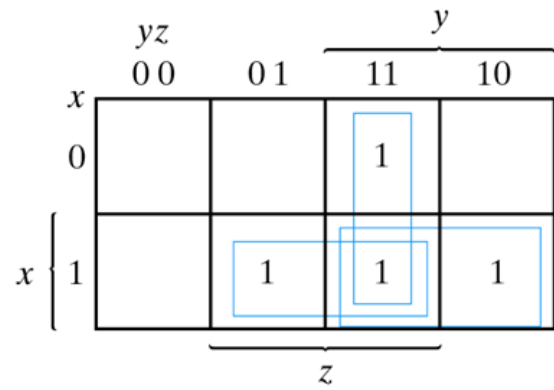
A Full adder is a combinational circuit that performs addition of three input bits. Half adder has inputs X, Y, Z and outputs sum (S) and carry(C). The truth table is

| X | Y | Z | Sum (S) | Carry (C) |
|---|---|---|------------|--------------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

The simplified Boolean expressions are



$$S = x'y'z + x'yz' + xy'z' + xyz$$

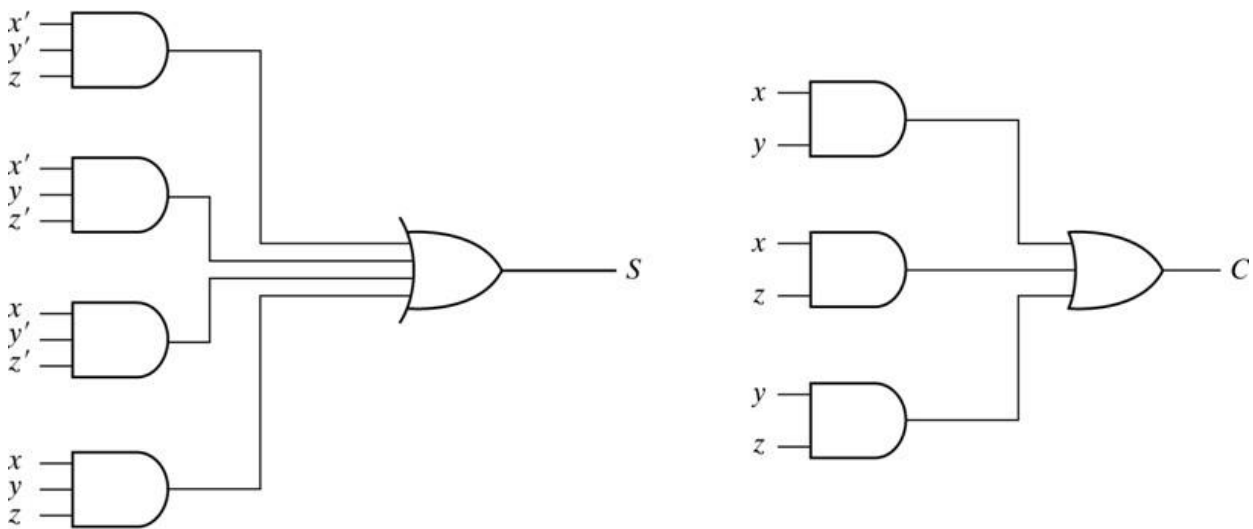


$$C = xy + xz + yz$$

$$= xy + xy'z + x'yz$$

Maps for Full Adder

The logic circuit to implement is as shown below



Implementation of Full Adder in Sum of Products

FULL ADDER USING TWO HALF ADDERS AND OR GATE

A full adder can also be implemented using two half adders and one OR gate as shown in fig.

The sum output from second half adder is

$$S = x \text{ EXOR } y \text{ EXOR } z \quad S = x'y'z' + x'yz' + xy'z' + xyz$$

$$C=xy+yz+xz$$

PROCEDURE:

1. The IC's are placed on the bread board.
2. A voltage of +5V is applied to pin no.14 and -Ve is applied to pin no.7.
3. Inputs and Outputs are connected according the gates which are taken. 10.For the input 1 we have to connect the input terminal to +5V and for 0 to -Ve.
4. Output is verified in LED. If the LED is ON the output is 1, if OFF it is 0. 12.According to the Logic gates truth table we have to verify the inputs and outputs.

RESULT:**CONCLUSION****VIVA QUESTIONS:**

1. What is use of Full adder?
2. What is difference between the half and full adder?
3. How many half adders required to make a full adder?
4. In full adder how many types of gates are required?
5. Draw full adder circuit?

Exp No:

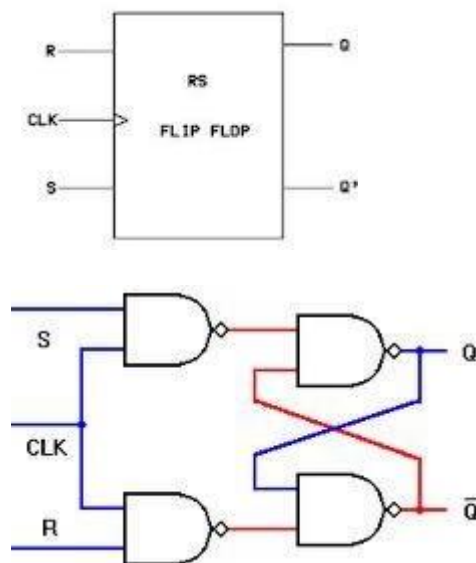
Date:

FLIP-FLOPS**AIM:** To verify the truth tables of Flip-Flops.**APPARATUS:**

| S.NO | APPARATUS | RANGE | QUANTITY |
|------|----------------------------|---|----------|
| 1 | IC's | 74LS08, 74LS32, 74LS04, 74LS00, 74LS02, 74LS86 | 1 |
| 2 | Light Emitting Diode (LED) | | 1 |
| 4 | Bread board | | 1 |
| 5 | Connecting wires | | REQUIRED |
| 6 | Fixed Power Supply | (0-5V) | 1 |

OPERATION:**i) RS flip-flop**

The fig shows clocked RS flip flop symbol, circuit and truth table.



$$Q_{N+1} = S + \bar{R}Q, SR = 0$$

| S | R | Q | Q_{N+1} |
|---|---|---|-----------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | X |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | X |

Indeterminate State

It consists of basic RS latch with two additional NAND gates and clock pulse. The operation is follows

- **When S = 0 , R = 0 and CLK=1:** There is no state change in the output.
- **When S = 1 , R = 0 and CLK=1:** Output Q is HIGH.
- **When S = 0 , R = 1 and CLK=1:** Output Q is LOW.
- **When S = 1 , R=1 and CLK=1:** Output is invalid and it is indeterminate state.

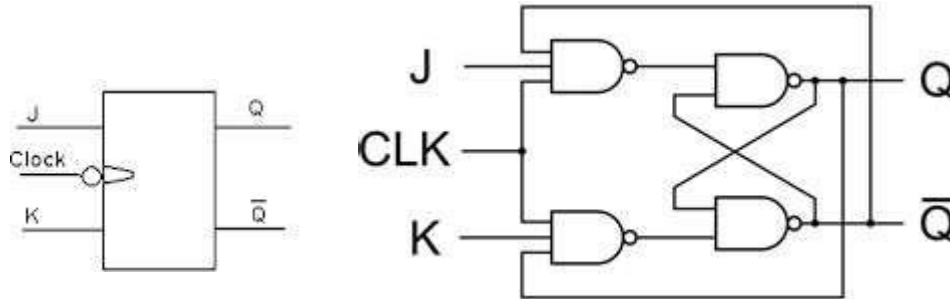
ii) JK- Flip Flop

JK flip-flop

The indeterminate state output in the RS latch was eliminated in the D latch by joining the inputs with an inverter. But the D latch has a single input. JK latch is similar to RS latch in that it has 2 inputs J and K as shown figure below. The indeterminate state has been

eliminated here: when both inputs are high, output toggles. The only difference we see here is output feedback to inputs, which is not there in the RS latch.

The fig shows JK flip flop symbol, circuit and truth table.

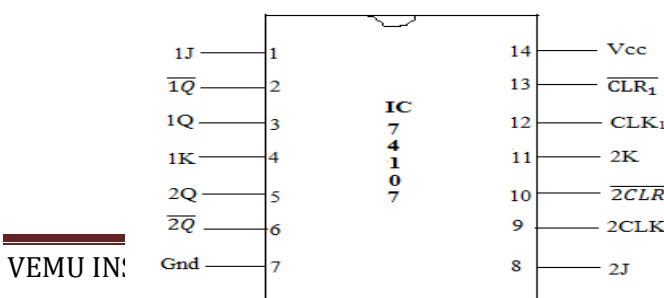


$$Q_{N+1} = J\bar{Q} + \bar{K}Q$$

| J | K | Q | Q _{N+1} |
|---|---|---|------------------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Master Slave J K Flip – Flop:

IC – 74107: Dual – Master – Slave J-K Flip - Flop



CIRCUIT IMPLEMENTATION:

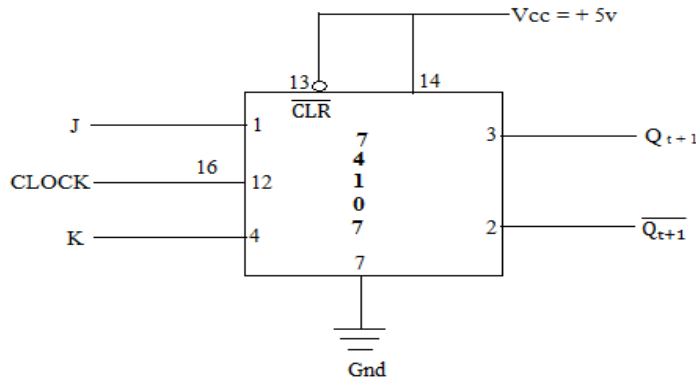
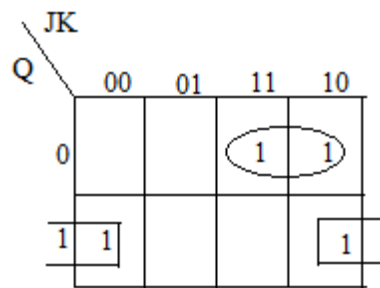


Fig: Master – Slave J –K Flip – Flop Circuit.

Truth Table of Master – Slave – JK Flip – Flop:

| Inputs | | | Outputs |
|--------|---|---|------------------|
| Q | J | K | Q _{t+1} |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |



Where
Q Present state

Characteristic eqn $Q_{t+1} = JQ + KQ$

Q_{t+1} Next state

RESULT:-

CONCLUSION:

VIVA QUESTIONS:

1. In full adder how many types of gates are required?
2. Difference between Mealy and Moore state machine?
3. What are the applications of flipflops?
4. what is disadvantage of SR flip-flop?
5. What is advantage of SR flip-flop?

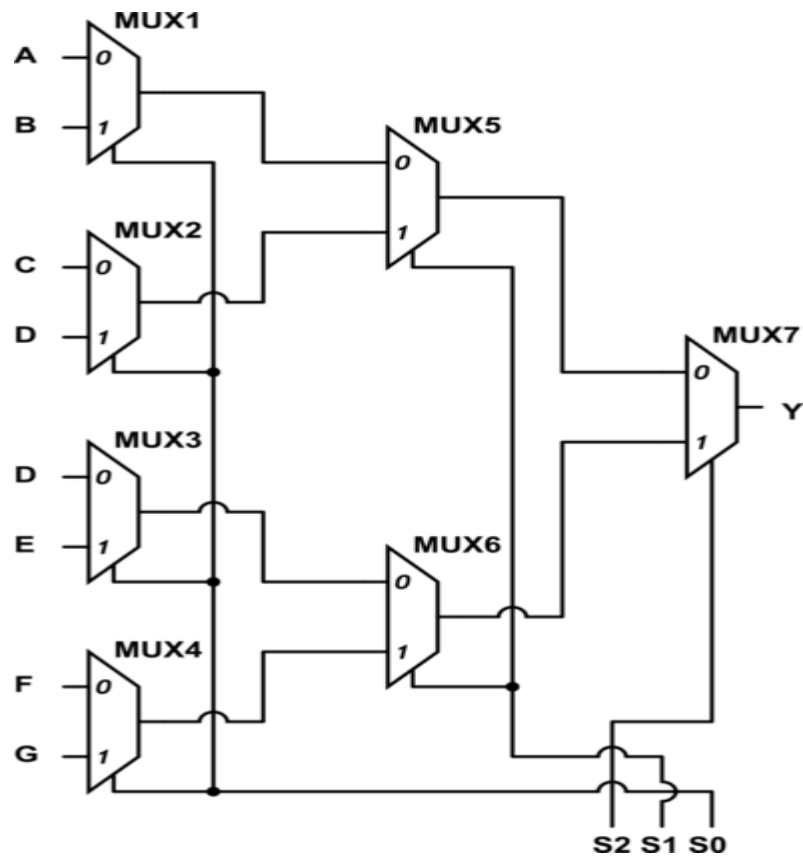
CIRCUIT DIAGRAM:

Fig: 8x1 MUX using 2x1 MUX

TRUTH TABLE:

| Select Data Inputs | | | Output |
|--------------------|-------|-------|--------|
| S_2 | S_1 | S_0 | Y |
| 0 | 0 | 0 | D_0 |
| 0 | 0 | 1 | D_1 |
| 0 | 1 | 0 | D_2 |
| 0 | 1 | 1 | D_3 |
| 1 | 0 | 0 | D_4 |
| 1 | 0 | 1 | D_5 |
| 1 | 1 | 0 | D_6 |
| 1 | 1 | 1 | D_7 |

Exp No:

Date:

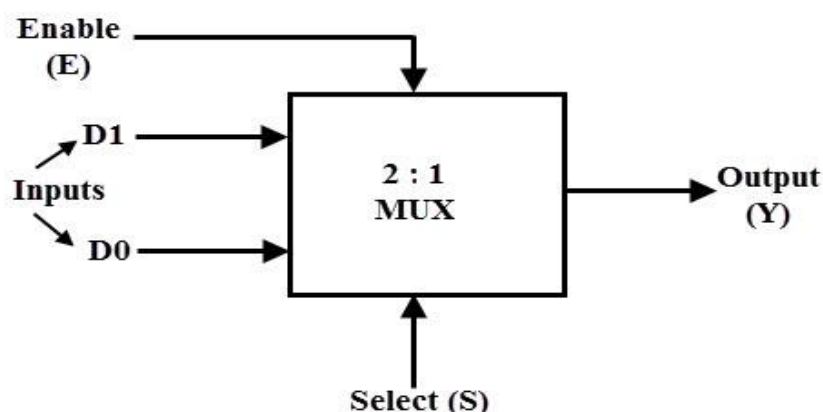
DESIGN AND REALIZATION OF 8X1 MUX USING 2X1 MUX**AIM:** To design and implement 8x1 MUX using 2x1 MUX.**APPARATUS:**

| S.NO | APPARATUS | RANGE | QUANTITY |
|------|--------------------|--------|----------|
| 1 | IC's | 74157 | 3 |
| 2 | Bread board | | 1 |
| 3 | Connecting wires | | REQUIRED |
| 4 | Fixed Power Supply | (0-5V) | 1 |

OPERATION:

2-to-1 Multiplexer A 2-to 1 multiplexer consists of two inputs D0 and D1, one select input S and one output Y. Depends on the select signal, the output is connected to either of the inputs. Since there are two input signals only two ways are possible to connect the inputs to the outputs, so one select is needed to do these operations. If the select line is low, then the output will be switched to D0 input, where as if select line is high, then the output will be switched to D1 input.

The figure below shows the block diagram of a 2-to-1 multiplexer which connects two 1-bit inputs to a commend estimation.

2to1 MUX:-

The truth table of the 2-to-1 multiplexer is shown below. Depending on the selector switching the inputs are produce dat outputs, i.e., D0, D1and are switched to the output for S=0 and S=1 respectively. Thus, the Boolean expression for the output becomes D0 when S=0 and output is D1 when S=1.

From the truth table the Boolean expression of the output is given as exp

$$Y = D_0 \bar{S} + D_1 S$$

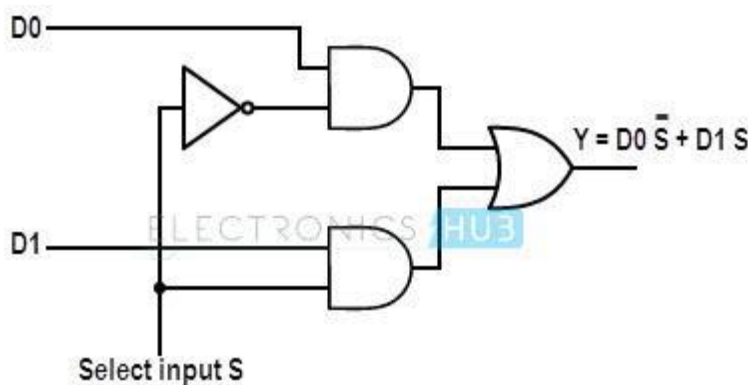
1 to 1 MUX truth table:-

| Select | Inputs | | Output |
|--------|--------|---|--------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

From the above output expression, the logic circuit of 2-to-1 multiplexer can be implemented using logic gates as shown in figure. It consists of two AND gates, one NOT gate and one OR gate. When the select line, S=0, the output of the upper AND gate is zero, but the lower AND gate is D0.

Thus, the output generated by the OR gate is equal to D0. Similarly, when S=1, the output of the lower AND gate is zero, but the output of upper AND gate is D1. Therefore, the output of the OR gate is D1. Thus, the above given Boolean expression is satisfied by this circuit.

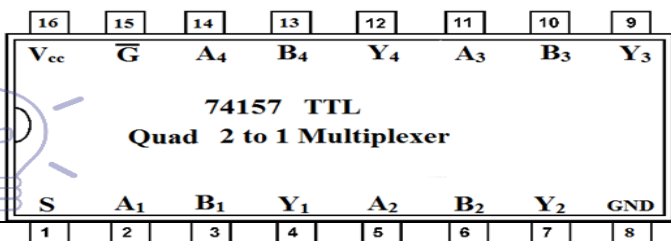
2to1 mux logic diagram:-



In some cases, two or more multiplexers are fabricated on a single IC because simple logic gates can implement the multiplexer. Generally four 2 line to 1 line multiplexers are fabricated in a single IC as shown in figure below. Some of these ICs of 2 to 1 multiplexers include IC74157 and IC74158. The selection line controls the input lines to the output in all four multiplexers.

Pin diagram of 74157 IC:-

| Pin Number | Configuration |
|------------|-----------------------------|
| 1 | Control signal S |
| 2 | Input A ₁ |
| 3 | Input B ₁ |
| 4 | Output Y ₁ |
| 5 | Input A ₂ |
| 6 | Input B ₂ |
| 7 | Output Y ₂ |
| 8 | GND |
| 9 | Output Y ₃ |
| 10 | Input B ₃ |
| 11 | Input A ₃ |
| 12 | Output Y ₄ |
| 13 | Input B ₄ |
| 14 | Input A ₄ |
| 15 | Active Low Enable \bar{G} |
| 16 | Vcc, power supply |



PROCEDURE:-

1. Connect the circuit as for circuit diagram.
2. Vary the inputs lines (Datalines) and selection lines and observe the output.
3. Verify the truth table for 8x1 mux.

RESULT:**CONCLUSION:****VIVA QUESTIONS:**

1. What is a multiplexer?
2. What is a 2x1 MUX?
3. What is a 8x1 MUX?
4. What is the function of an enable input on a multiplexer chip?
5. What are advantages of using MUX?

ADDITIONAL EXPERIMENTS

CIRCUIT DIAGRAM:

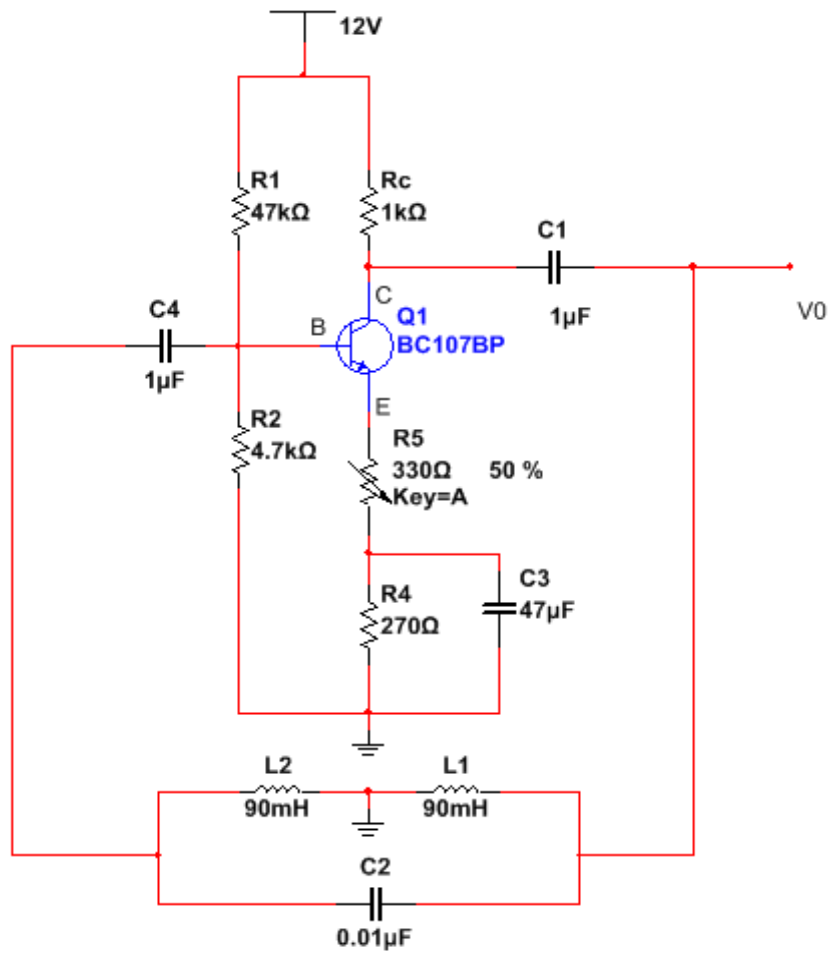
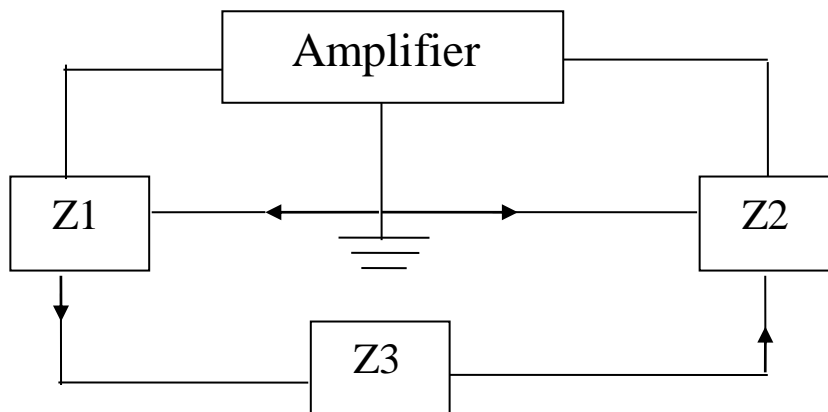


Fig: Hartley Oscillator

BLOCK DIAGRAM:



Exp:**Date:****HARTLEY OSCILLATOR****AIM:** To design and simulate Hartley oscillator and verify it to the theoretical value.**SOFTWARE REQUIRED:** NI Multisim software 14.1 version.**HARDWARE REQUIRED:** Personal Computer**APPARATUS:**

| S.NO | APPARATUS | RANGE | QUANTITY |
|------|------------------|---------------|----------|
| 1 | Transistor | SL100 | 1 |
| 2 | Resistors | 47K Ω | 1 |
| | | 1K Ω | 1 |
| | | 4.7K Ω | 1 |
| | | 270 Ω | 1 |
| 3 | Capacitors | 1 μ F | 2 |
| | | 47 μ F | 1 |
| | | 0.01 μ F | 1 |
| 4 | DRB | 330 Ω | 1 |
| 5 | DIB | 90mH | 2 |
| 6 | DCB | - | 1 |
| 7 | RPS | 0-30V | 1 |
| 8 | CRO | 30MHz | 1 |
| 9 | Bread Board | - | 1 |
| 10 | Connecting Wires | - | REQUIRED |

OPERATION:

When the power supply is switched ON the transistor starts conducting and the collector current increases. As a result the capacitor C1 starts charging and when the capacitor C1 is fully charged it starts discharging through coil L1. This charging and discharging creates a series of damped oscillations in the tank circuit and it is the key.

The oscillations produced in the tank circuit is coupled (fed back) to the base of Q1 and it appears in the amplified form across the collector and emitter of the transistor.

The output voltage of the transistor (voltage across collector and emitter) will be in phase with the voltage across inductor L1. Since the junction of two inductors is grounded, the voltage across L2 will be 180° out of phase to that of the voltage across L1. The voltage across L2 is actually fed back to the base of Q1.

From this we can see that, the feedback voltage is 180° out of phase with the transistor and also the transistor itself will create another 180° phase difference. So the total phase difference between input and output is 360° and it is very important condition for creating sustained oscillations.

The frequency "F" of a Hartley oscillator can be expressed using the equation;

$$F = \frac{1}{2\pi\sqrt{LC}}$$

C is the capacitance of the capacitor C1 in the tank circuit.

$L = L_1 + L_2$, the effective series inductance of the inductors L1 and L2 in the tank circuit.

Here the coils L1 and L2 are assumed to be wound on different cores. If they are wound on a single core then $L = L_1 + L_2 + 2M$ where M is the mutual inductance between the two coils.

SOFTWARE PROCEDURE:

1. Design the circuit as per specifications.
2. Simulate the circuit.
3. Observe the response from oscilloscope.
4. Calculate the efficiency and compare it with theoretical value.
5. Plot the graph for simulated output.

HARDWARE PROCEDURE:

1. Connect the circuit diagram as shown in the figure
2. Set $V_{CC} = 12V$
3. Keep the capacitance of the decade capacitance box to $0.1\mu F$, and measure the generated output signal amplitude and frequency from CRO.
4. Vary the Inductance in steps and note down frequency and amplitude at each.

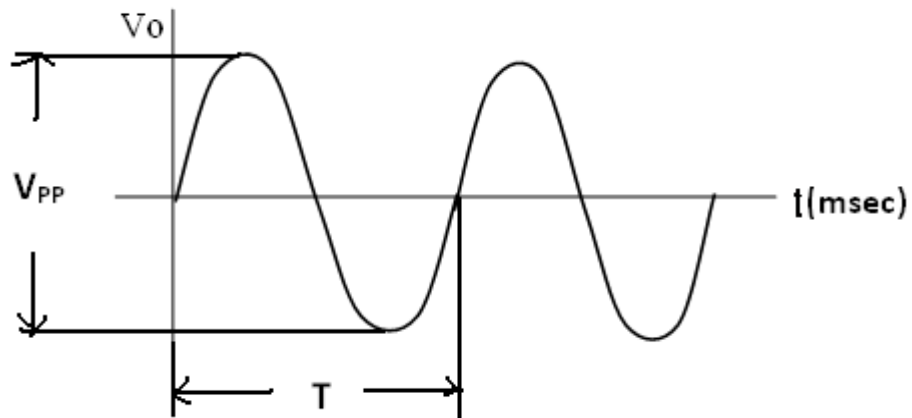
Plot the graph from CRO and verify the practical frequency with theoretical frequency

CALCULATIONS:

Theoretical frequency $f_0 = \frac{1}{2\pi\sqrt{CL_{eq}}}$

Where $L = L_1 + L_2$

C = Capacitance of decade capacitance box at particular frequency

MODEL WAVE FORM:**TABULAR COLUMN:****SOFTWARE:**

| SL. NO. | C (μ F) | L ₁ (mH) | L ₂ (mH) | THEORETICAL f(HZ) | PRACTICAL Timeperiod(sec) | PRACTICAL f(HZ) | AMPLITUDE (V) |
|---------|--------------|---------------------|---------------------|-------------------|---------------------------|-----------------|---------------|
| | | | | | | | |

HARDWARE:

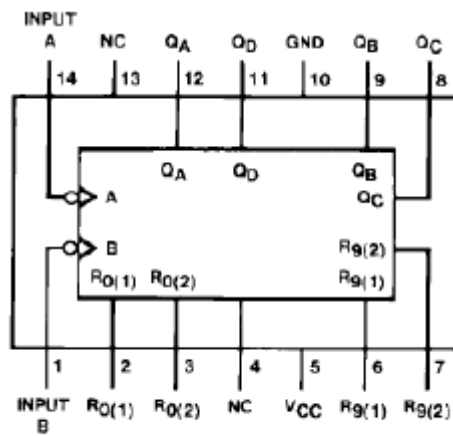
| SL. NO. | C (μ F) | L ₁ (mH) | L ₂ (mH) | THEORETICAL f(HZ) | PRACTICAL Timeperiod(sec) | PRACTICAL f(HZ) | AMPLITUDE (V) |
|---------|--------------|---------------------|---------------------|-------------------|---------------------------|-----------------|---------------|
| | | | | | | | |

RESULT:**CONCLUSION:****VIVA QUESTIONS:**

1. What are the advantages and disadvantages of negative feedback?
2. What are the conditions for sustained oscillator or what is Barkhausen criterion?
3. What are the types of feedback oscillators?
4. What is LC oscillator?
5. How does an oscillator differ from an amplifier?

DECADE COUNTER 74LS90

PIN DIAGRAM:-



1) BCD Count sequence when O/P QA is connected to input B for BCD count.

| Count | Outputs | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _D | Q _C | Q _B | Q _A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

2) BCD Count sequence when O/P Q_D is connected to input A for Bi-quinary count

| Count | Outputs | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _A | Q _D | Q _C | Q _B |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

Exp No:

Date:

DECADE COUNTER 74LS90**AIM:** To construct and verify the working of a single digit decade counter using IC 7490.**APPARATUS:**

| S.NO | APPARATUS | RANGE | QUANTITY |
|------|------------------------|----------|----------|
| 1 | IC | IC74LS90 | 1 |
| 2 | Digital IC Trainer Kit | | |
| 3 | Patch card | | REQUIRED |
| 4 | Fixed Power Supply | (0-5V) | 1 |

THEORY:

The 7490 monolithic counter contains four master slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The counter has a gated zero reset and also has gated set to nine inputs for used in BCD nine's complement applications.

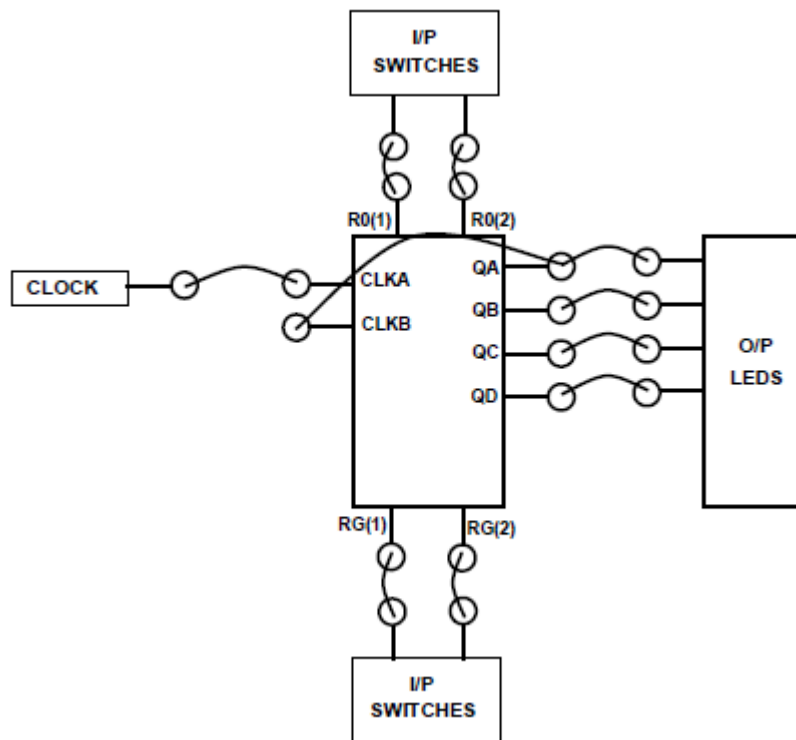
To use the maximum count length (decade or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate Function Table.

A symmetrical divide-by-ten count can be obtained from the counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide by- ten square wave at output Q_A.

RESET/ COUNT function table

| Reset Inputs | | | | Outputs | | | |
|--------------|-------|-------|-------|----------------|----------------|----------------|----------------|
| R0(1) | R0(2) | R9(1) | R9(2) | Q _D | Q _C | Q _B | Q _A |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | COUNT | | | |
| L | X | L | X | COUNT | | | |
| L | X | X | L | COUNT | | | |
| X | L | L | X | COUNT | | | |

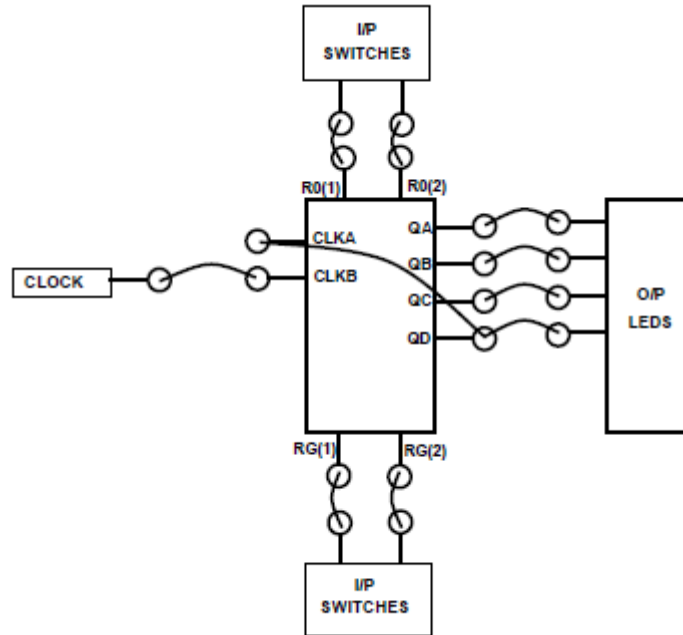
H = HIGH Level
L = LOW Level
X = Don't Care

PROCEDURE:

1. Do the connection as shown in block diagram above and switch ON the power supply.
2. Provide the proper logic inputs to R0 (1), R0 (2), RG (1) and RG (2) by referring its RESET/ COUNT function table
3. Now provide Clock pulse one at a time by pressing Clock switch & observe the led indication at O/P section. It should be as shown in table.

| SR NO | CLOCK PULSES | OUTPUTS | | | |
|-------|--------------|---------|----|----|----|
| | | QD | QC | QB | QA |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | 2 | 0 | 0 | 0 | 1 |
| 3 | 3 | 0 | 0 | 1 | 0 |
| 4 | 4 | 0 | 0 | 1 | 1 |
| 5 | 5 | 0 | 1 | 0 | 0 |
| 6 | 6 | 0 | 1 | 0 | 1 |
| 7 | 7 | 0 | 1 | 1 | 0 |
| 8 | 8 | 0 | 1 | 1 | 1 |
| 9 | 9 | 1 | 0 | 0 | 0 |
| 10 | 10 | 1 | 0 | 0 | 1 |

4. Once the count reached to 1001 counter resets to 0000. That means it count 10 clock pulses and counter advances its counts by ten. The 7490 can be configured in following mode also.

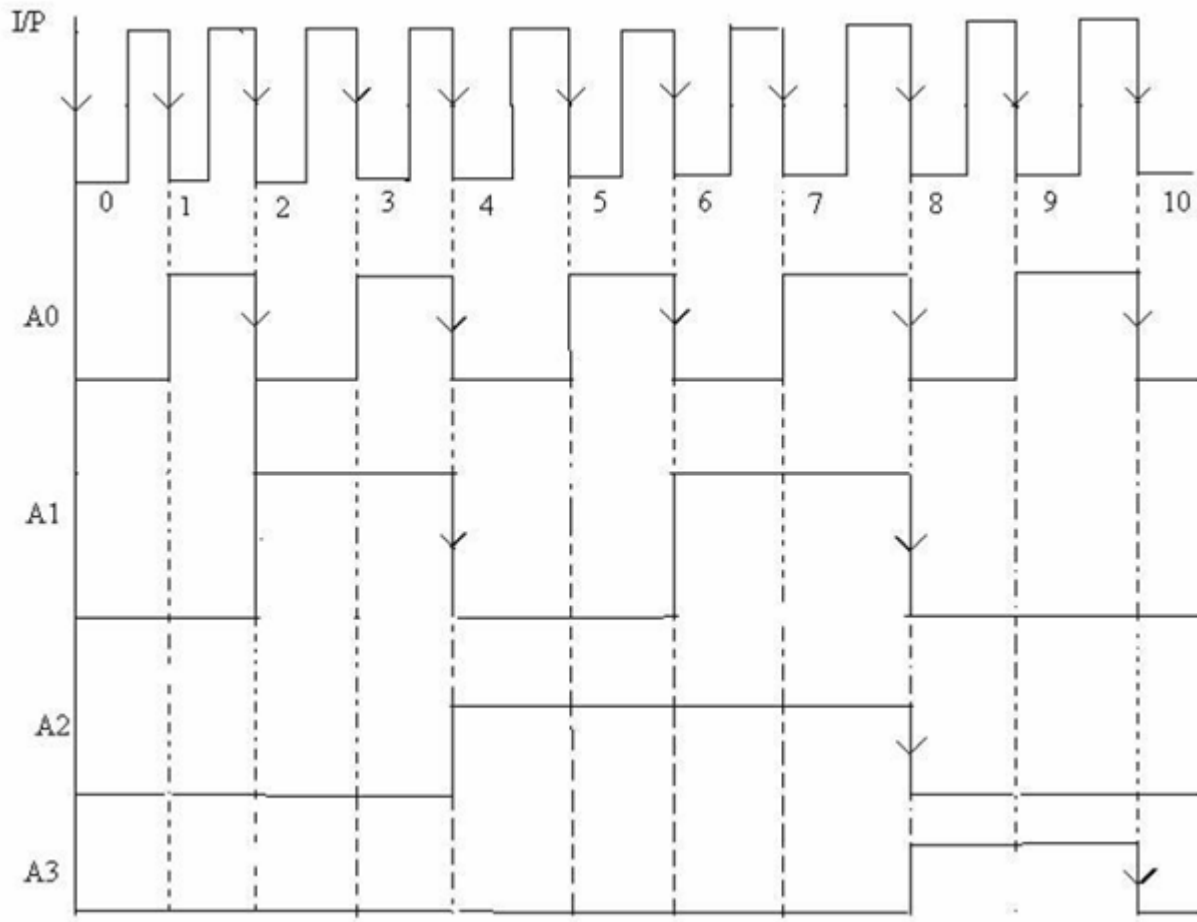


5. Do the connection as shown in block diagram above
6. Provide the proper logic inputs to R0 (1), R0 (2), RG (1) and RG (2) by referring its RESET/ COUNT function table.
7. Now provide Clock pulse one at a time by pressing Clock switch & observe the LED Indication at O/P section. It should be as shown in table.

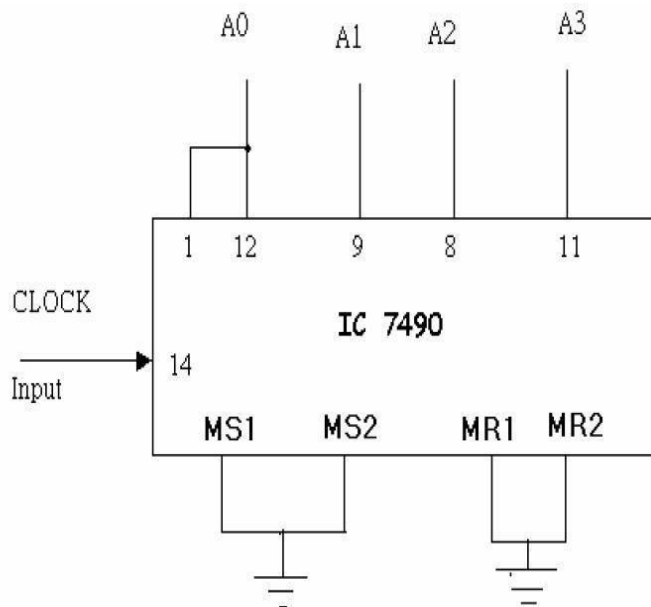
| SR NO | CLOCK PULSES | OUTPUTS | | | |
|-------|--------------|---------|----|----|----|
| | | QA | QD | QC | QB |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 2 | 2 | 0 | 0 | 1 | 0 |
| 3 | 3 | 0 | 0 | 1 | 1 |
| 4 | 4 | 0 | 1 | 0 | 0 |
| 5 | 5 | 1 | 0 | 0 | 0 |
| 6 | 6 | 1 | 0 | 0 | 1 |
| 7 | 7 | 1 | 0 | 1 | 0 |
| 8 | 8 | 1 | 0 | 1 | 1 |
| 9 | 9 | 1 | 1 | 0 | 0 |
| 10 | 10 | 0 | 0 | 0 | 0 |

8. In this case counter output is not in sequence as in earlier case. Once the count reached to 1100 counter resets to 0000. That means it count 10 clock pulses.

WAVE FORMS:



PIN DIAGRAM:-



RESULT:**CONCLUSION:****VIVA QUESTIONS:**

1. Define counter, mention some application?
2. What is the difference between ring counter and Johnson counter?
3. What is the other name for decade counter?
4. How many states are there in decade counter?
5. How many flip-flops are needed for a decade counter?