SUBJECT:VLSI DESIGN(20A04606)

YEAR/SEM: III-II

BRANCH:EEE

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MOS Field-Effect Transistors (MOSFETs)

- **Compared to BJTs, MOSFETs can be made quite small (i.e., requiring a small area on the silicon IC chip).**
- **Their manufacturing process is relatively simple.**
- **Their operation requires comparatively little power.**
- **Ways to implement digital and analog functions utilizing MOSFETs almost exclusively (i.e., with very few or no resistors).**

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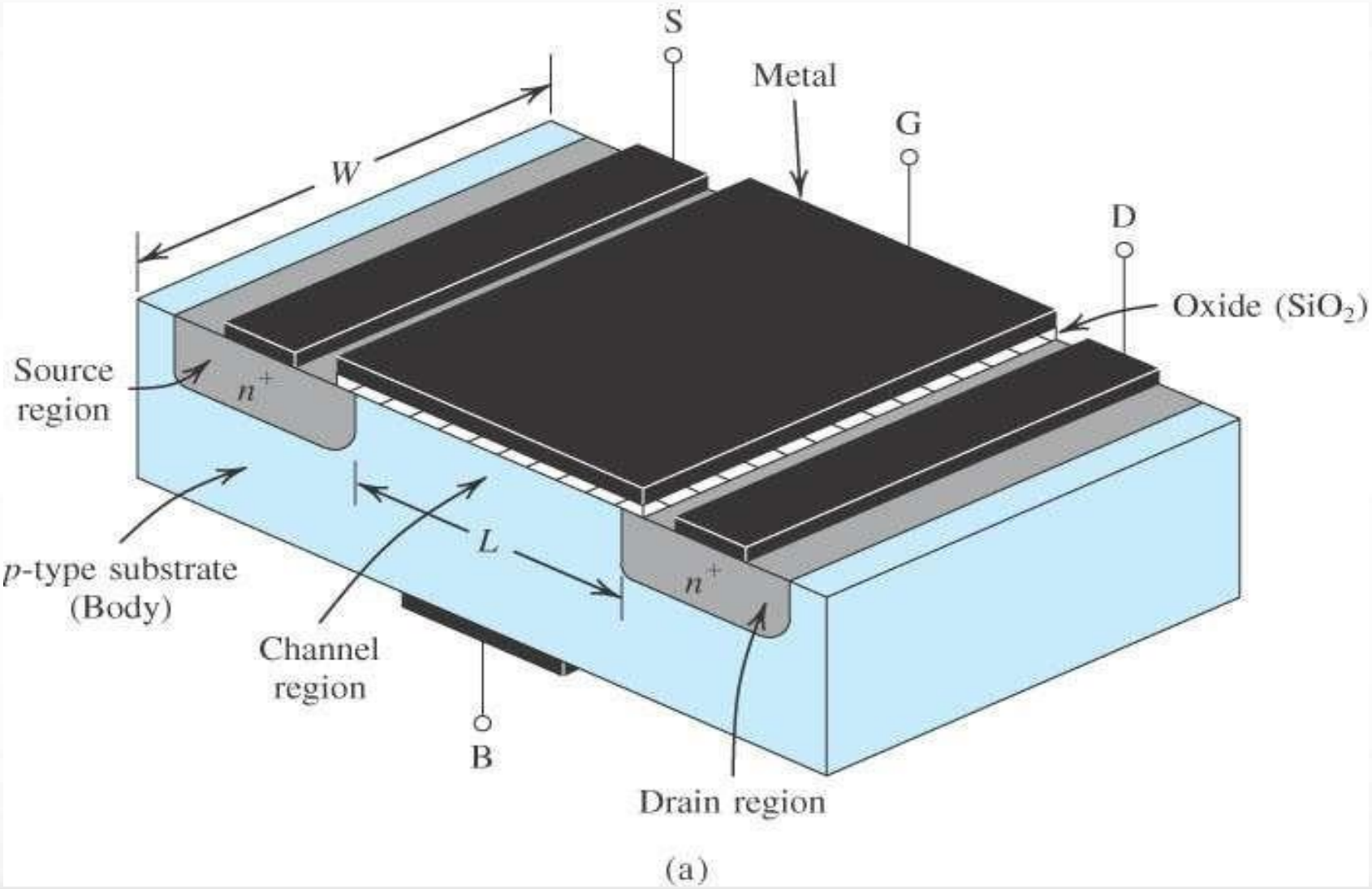
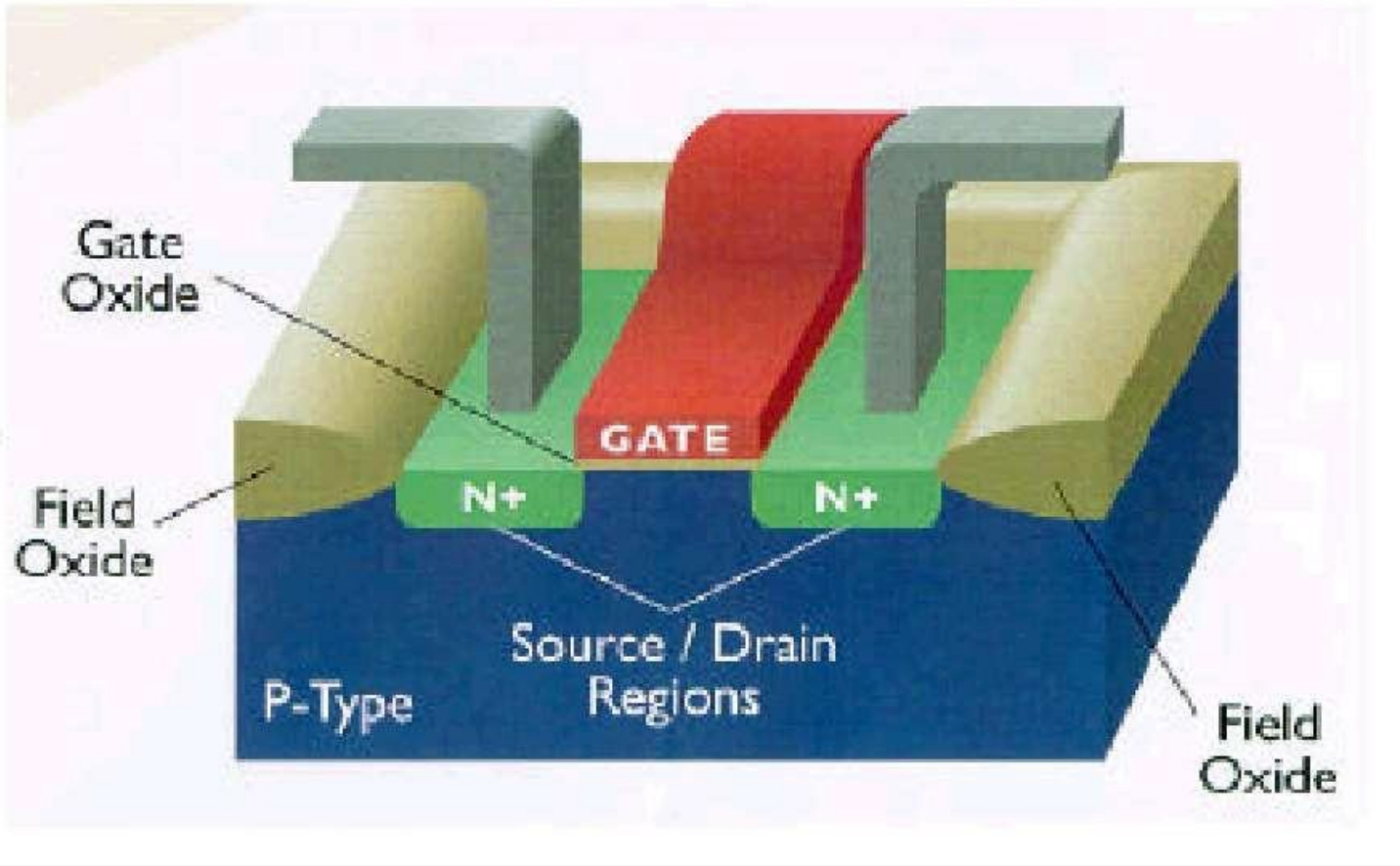
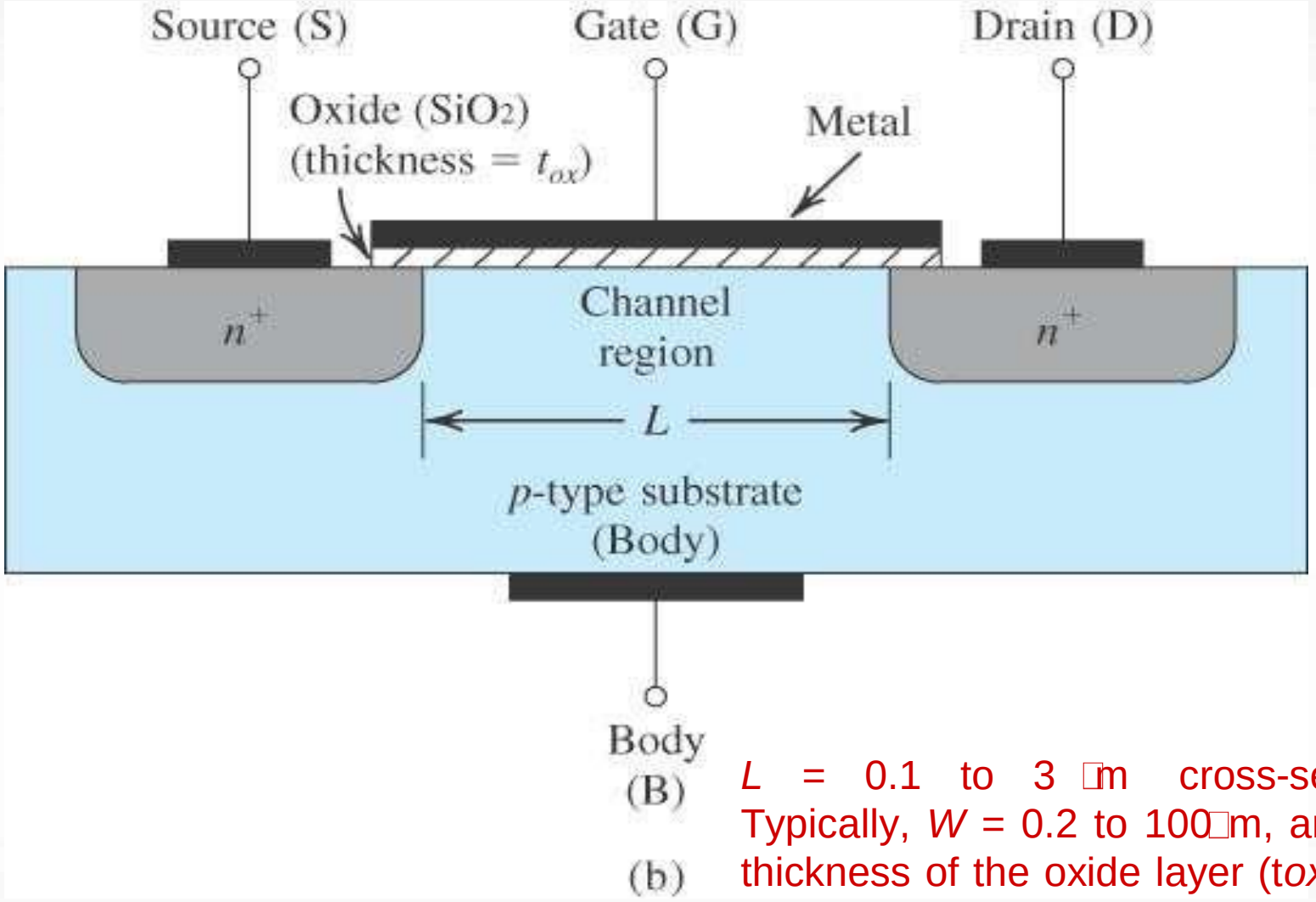
- **Possible to pack large numbers of MOSFETs (>200 million!) on a single IC chip to implement very sophisticated, very-large-scale-integrated (VLSI) circuits such as those for memory and micro-processors.**
- **Analog circuits such as amplifiers and filters are also implemented in MOS Technology.**

Physical structure of the enhancement-type NMOS transistor



3D Perspective

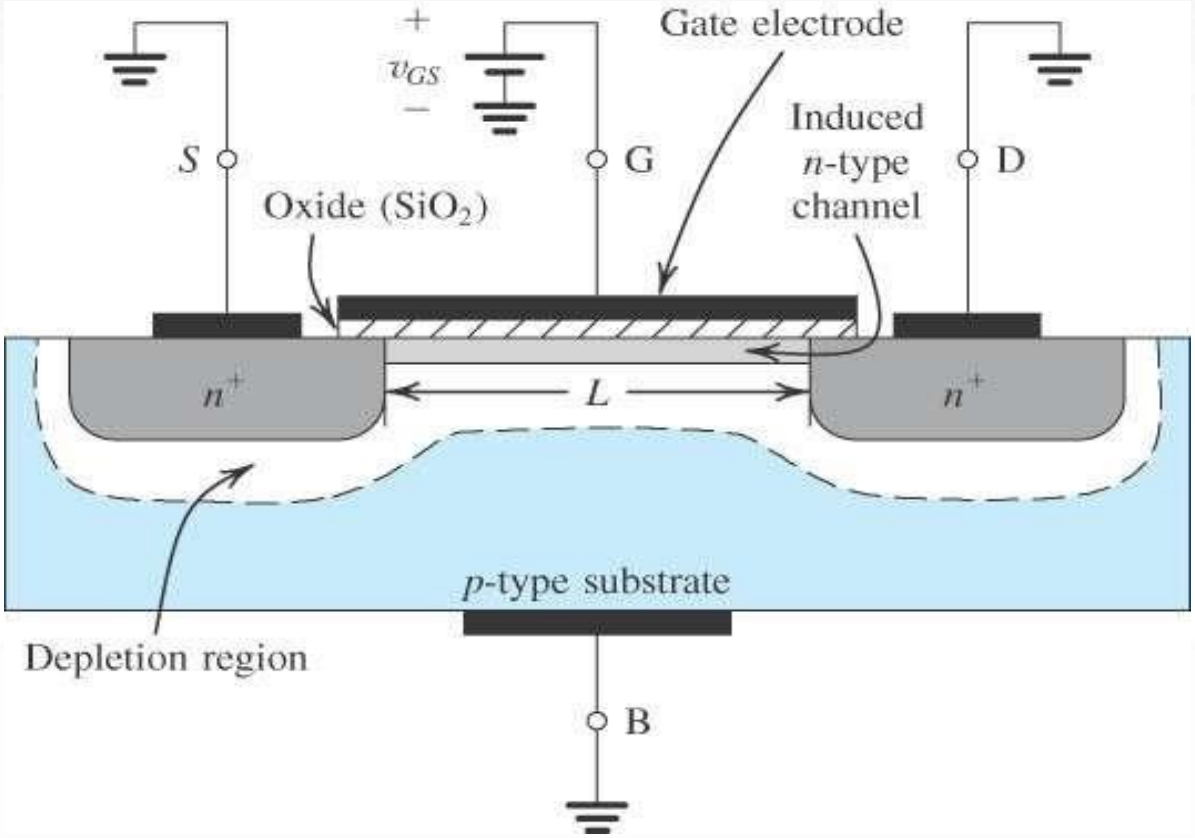




(b)

L = 0.1 to 3 □m cross-section. Typically, W = 0.2 to 100□m, and the thickness of the oxide layer (t*ox*) is in the range of 2 to 50 nm.

Creating a Channel for Current Flow



N-channel MOSFET is formed in a p-type substrate: Channel created by inverting the substrate surface from p type to n type. Hence the induced channel is also called an inversion layer.

Gate voltage at which a sufficient number of mobile electrons accumulate---- Threshold voltage Vt

Applying a Small VDS

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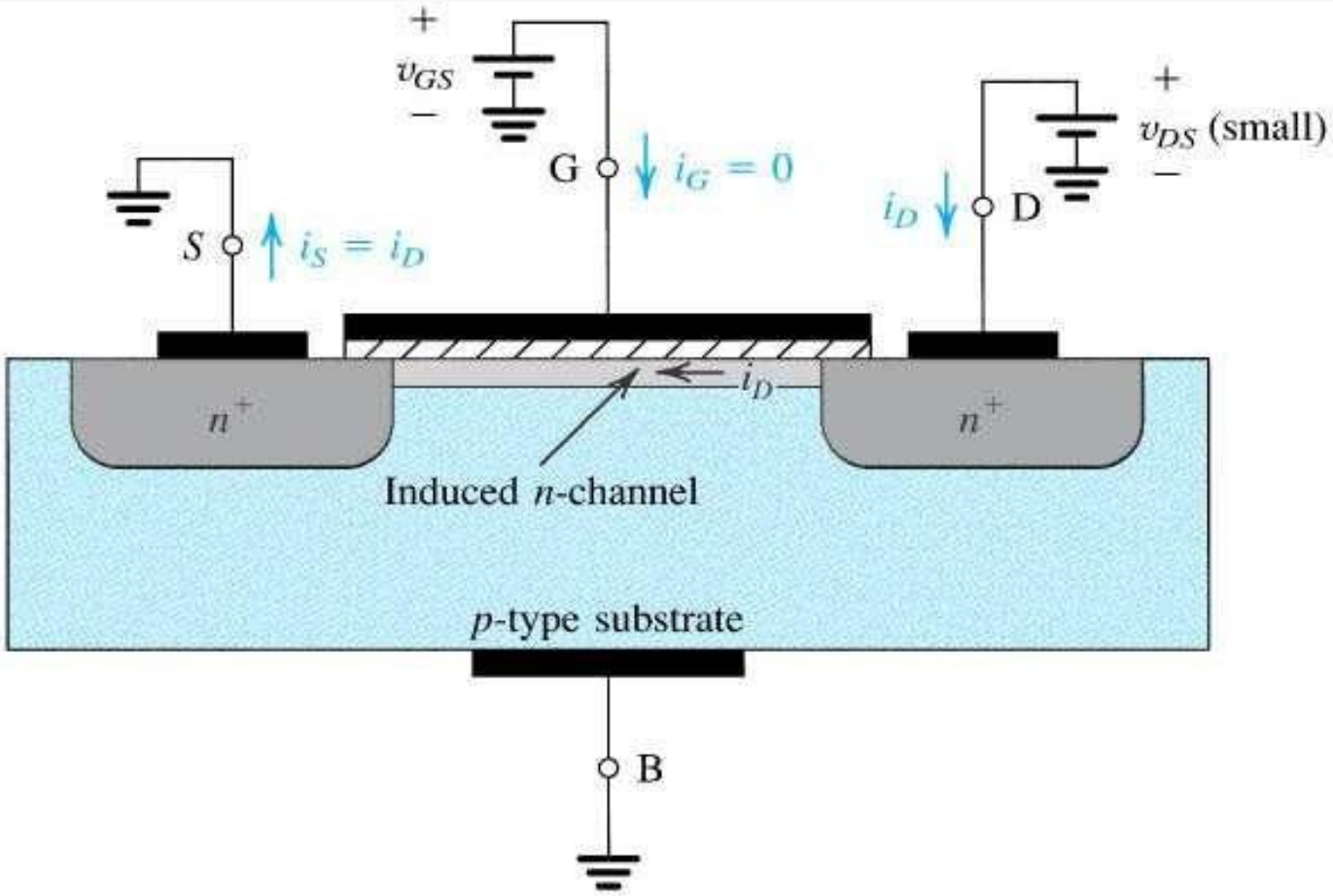
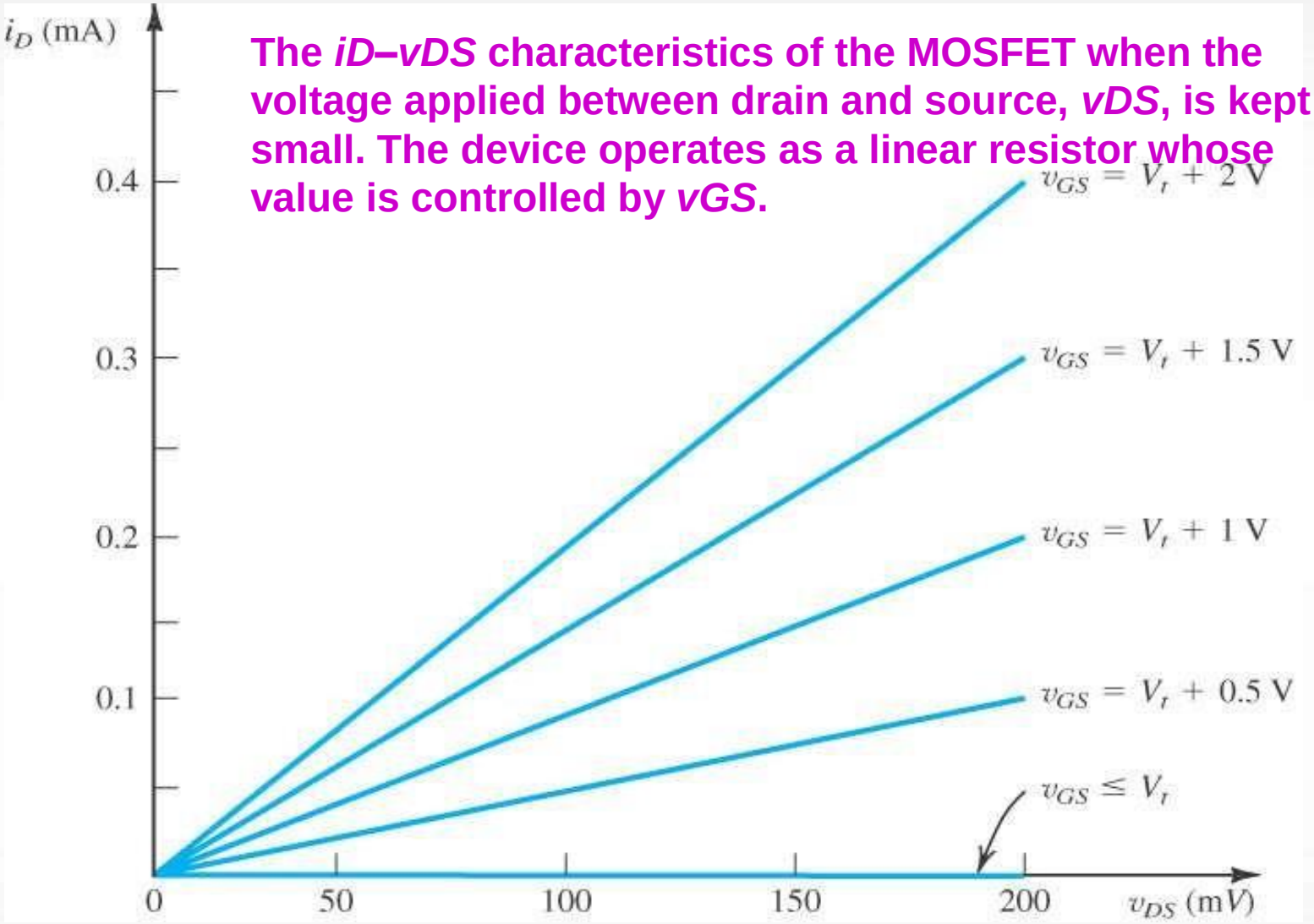
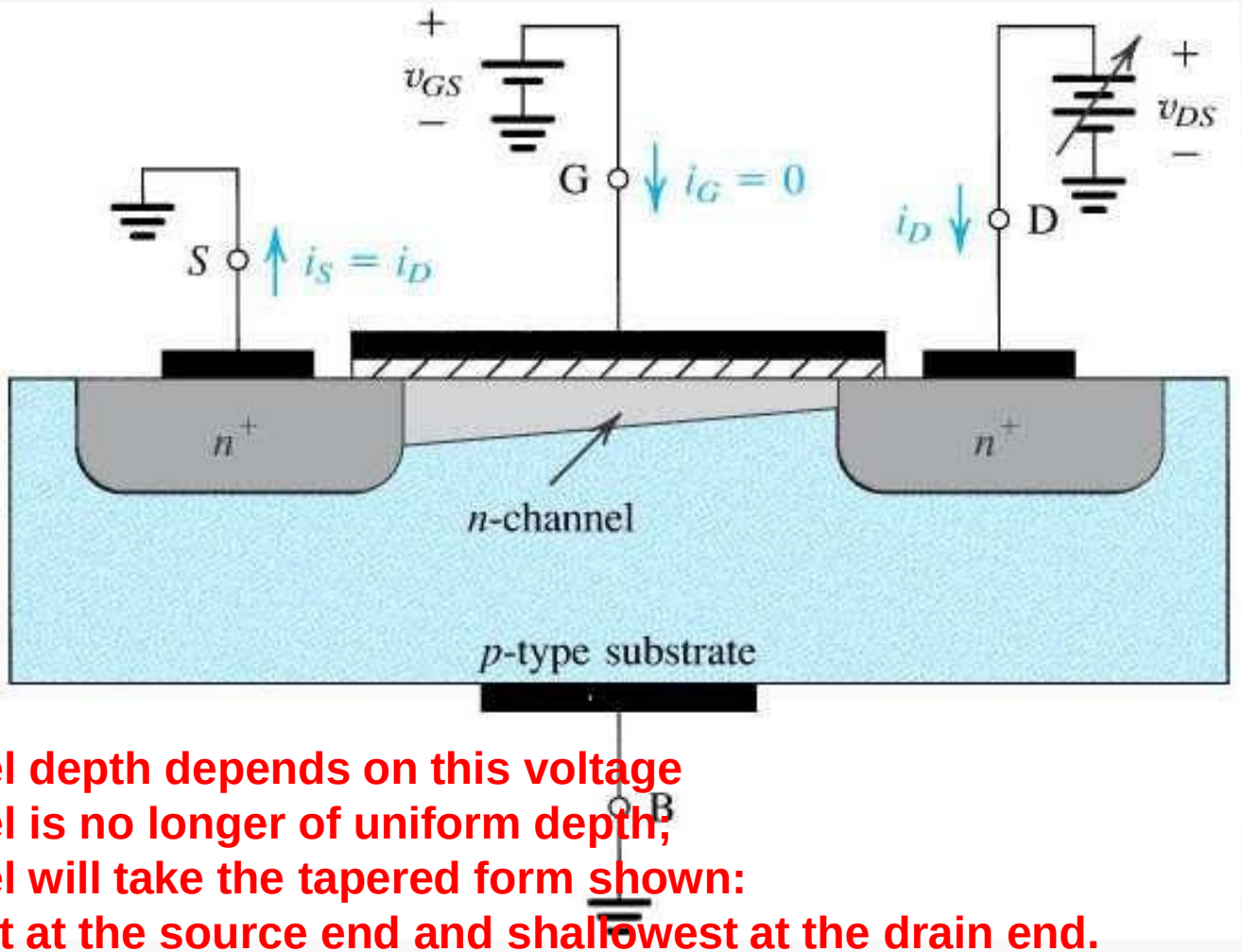


VDS causes a current ID to flow through source and drain.Conductance of the channel is proportional to the excess gate voltage VGS above Vt

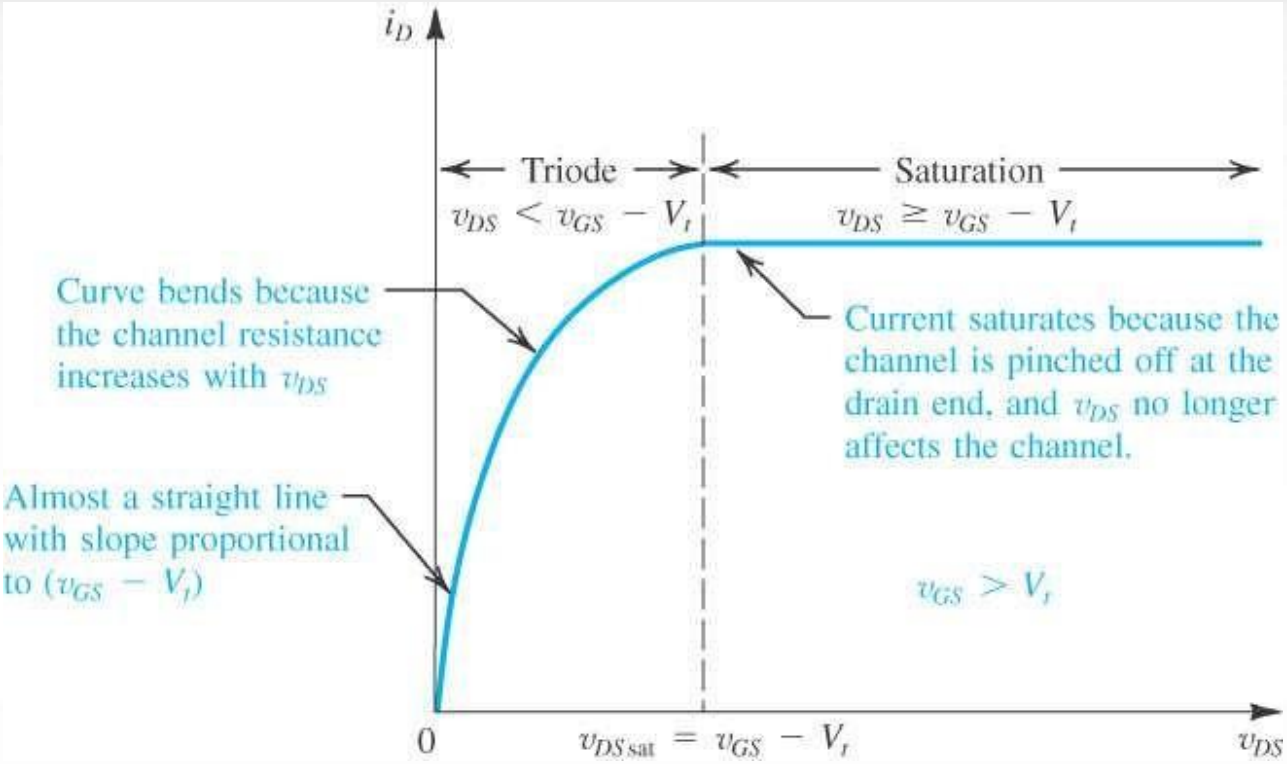
The *iD–vDS* characteristics of the MOSFET when the voltage applied between drain and source, *vDS*, is kept small. The device operates as a linear resistor whose value is controlled by *vGS*.

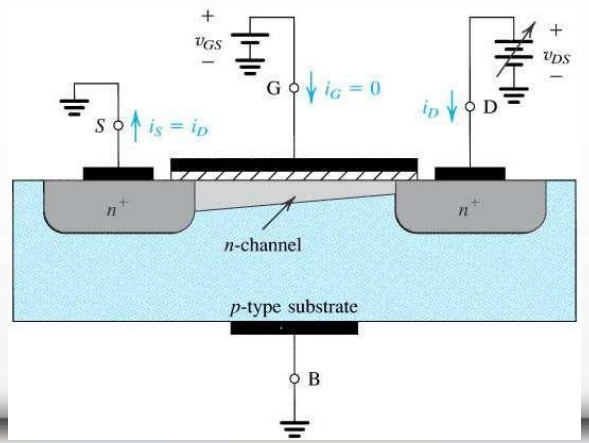


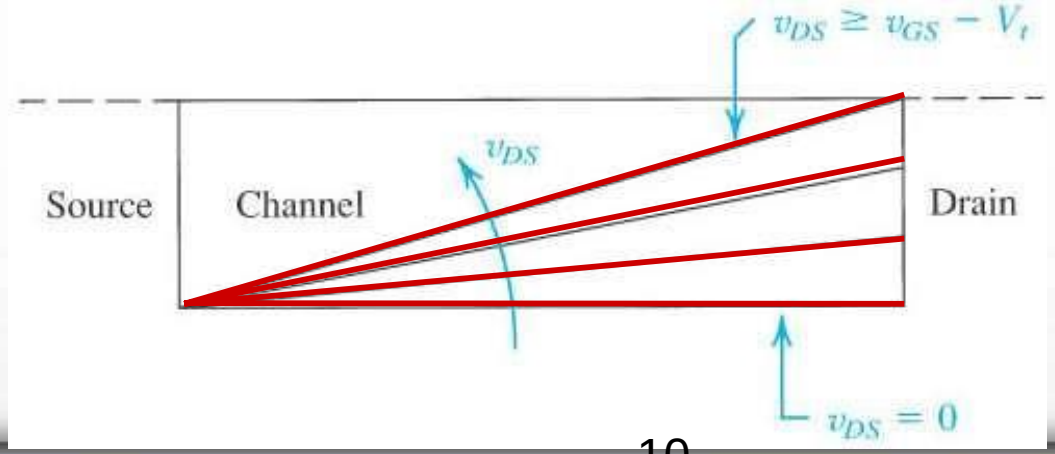
Operation as VDS Is Increase



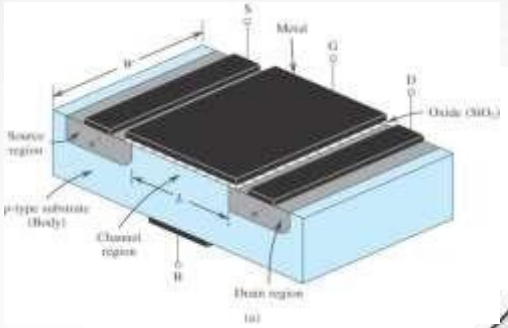
- Channel depth depends on this voltage
- Channel is no longer of uniform depth;
- Channel will take the tapered form shown:
- Deepest at the source end and shallowest at the drain end.
- As VDS is increased, the channel becomes more tapered and its resistance increases correspondingly


i_D
Triode
$v_{DS} < v_{GS} - V_t$
Saturation
$v_{DS} \geq v_{GS} - V_t$
Curve bends because the channel resistance increases with v_{DS}
Current saturates because the channel is pinched off at the drain end, and v_{DS} no longer affects the channel.
Almost a straight line with slope proportional to $(v_{GS} - V_t)$
$v_{GS} > V_t$
0
$v_{DS\,sat} = v_{GS} - V_t$
v_{DS}


v_{GS}
G
$i_G = 0$
S
$i_S = i_D$
i_D
D
v_{DS}
n^+
n^+
n-channel
p-type substrate
B


$v_{DS} \geq v_{GS} - V_t$
v_{DS}
Source
Channel
Drain
$v_{DS} = 0$

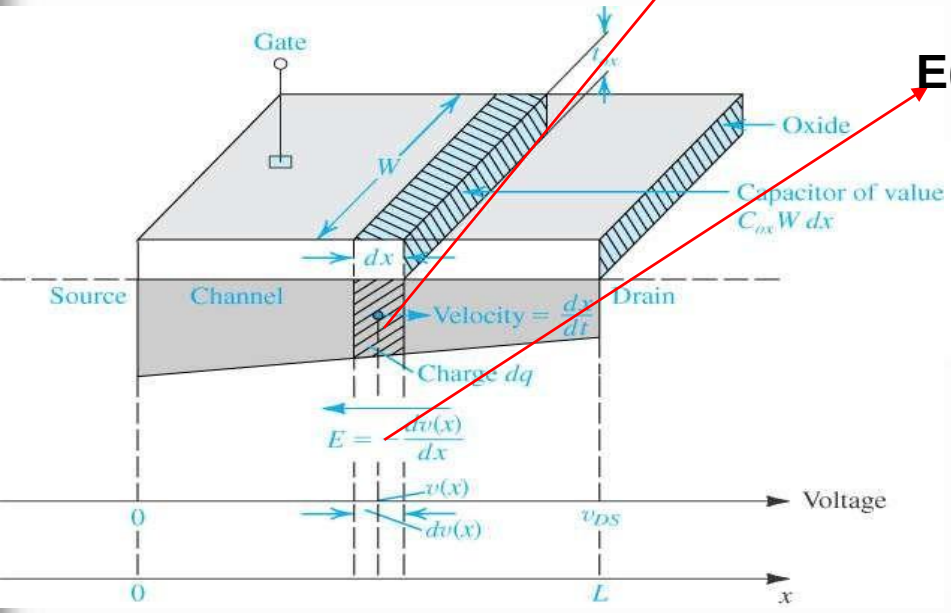
Derivation of the iD-VDS Relationship .



Cox =

□ox/tox =3.9 x 8.854 x 10-12 = 3.45 x 10-11F/ m

$$dq = -C_{ox}(W\,dx)[v_{GS} - v(x) - V_t]$$



$$E(x) = -\frac{dv(x)}{dx}$$

Electrtric field E(x) causes the electron charge dq to drift toward the drain with a velocity dx/dt

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dv(x)}{dx}$$

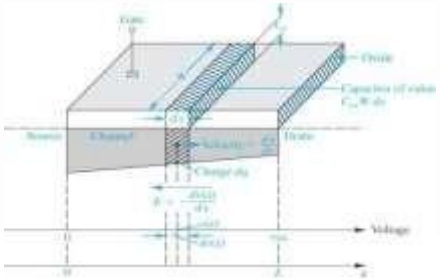
$$i = dq/dt = \frac{dq}{dx}\frac{dx}{dt}$$

$$i = -\mu_n C_{ox} W [V_{GS} - v(x) - V_t] \frac{dv(x)}{dx}$$

$$iDdx = \mu nCoxW\,[VGS - Vt - v(x)]\,dv(x)$$

Integrating both sides of this equation from x= 0 to x=L and, correspondingly, for v(0) = 0 and v(L)=vDS

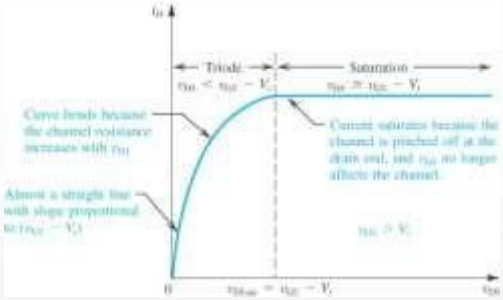
$$\int_0^L iDdx = \int_0^{v_{DS}} \mu nCoxW\,[VGS - Vt - v(x)]\,dv(x)$$



$$iD = (\mu nCox)\frac{W}{L}\left[(VGS - Vt)VDS - \frac{1}{2}V2DS\right]$$

At the beginning of the saturation region *substituting* VDS = VGS - V t ,

$$i_D = \frac{1}{2}k_n\left(\frac{W}{L}\right)(v_{GS} - V_t)^2$$



□nCox is a constant determined by the process technology used to fabricate the n-channel MOSFET. It is known as the *process transconductance* parameter.

Denoted k'n and has the dimensions of A/V2

k'n = □nCox

Aspect Ratio of the MOSFET

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$ (Triode region)

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2$$ (Saturation region)

Different notations: Kn, K'n □n; C"ox Tox ; VT0,VTN,VTP;

Consider a process technology for which Lmin =0.4 □m, tox = 8 nm, □n = 450 cm2/V- s, and Vt = 0.7 V.

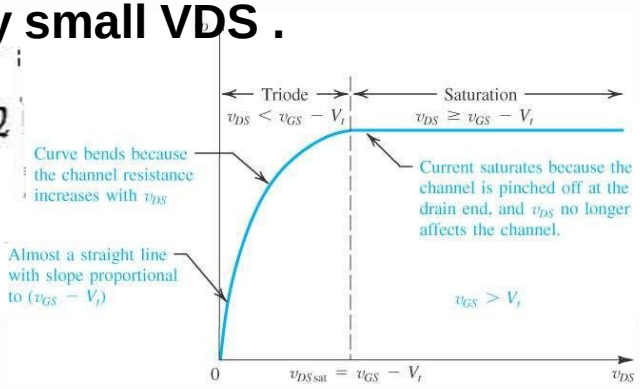
(a) Find Cox and k'n .

(b) For a MOSFET with W /L = 8 □m/0.8 □m, calculate the values of VGS and VDSmin needed to operate the transistor in the saturation region with a dc current ID = 100 □A.

(c) For the device in (b), find the value of VGS reguired to cause the device to operate as a l000-□ resistor for very small VDS .

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}}{8 \times 10^{-9}} = 4.32 \times 10^{-3}\ \text{F/m}^2$$

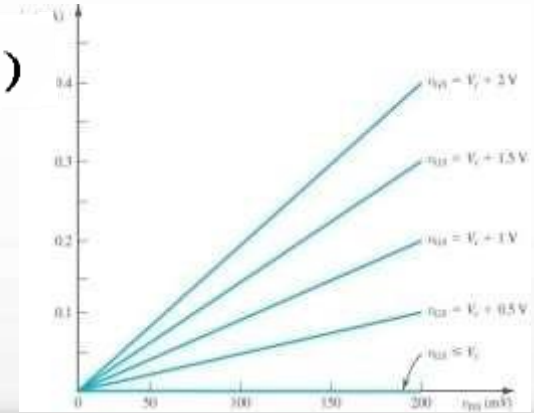
$$= 4.32\ \text{fF}/\mu\text{m}^2$$



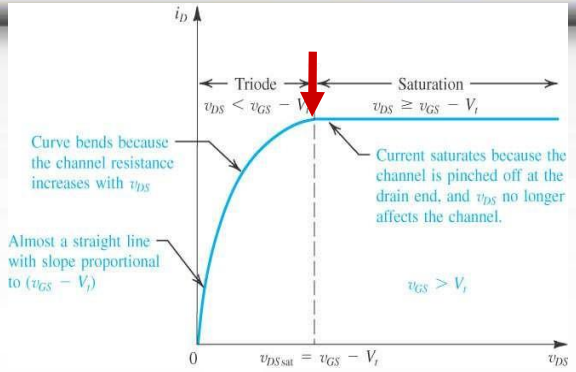
$$k_n' = \mu_n C_{ox} = 450\ (\text{cm}^2/\text{V}\cdot\text{s}) \times 4.32\ (\text{fF}/\mu\text{m}^2)$$

$$= 450 \times 10^8\ (\mu\text{m}^2/\text{V}\cdot\text{s}) \times 4.32 \times 10^{-15}\ (\text{F}/\mu\text{m}^2)$$

$$= 194 \times 10^{-6}\ (\text{F/V}\cdot\text{s}) = 194\ \mu\text{A/V}^2$$



(b) For operation in the saturation region,



$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2$$

$$100 = \frac{1}{2} \times 194 \times \frac{8}{0.8} (V_{GS} - 0.7)^2$$

$$V_{GS} - 0.7 = 0.32 \text{ V} \qquad V_{GS} = 1.02 \text{ V}$$

$$V_{DS\min} = V_{GS} - V_t = 0.32 \text{ V}$$

(c) For the MOSFET in the triode region with VDS very sm

$$r_{DS} \equiv \left. \frac{v_{DS}}{i_D} \right|_{\text{small } v_{DS}} = 1 \Big/ \left[k_n' \frac{W}{L} (V_{GS} - V_t) \right]$$

$$1000 = \frac{1}{194 \times 10^{-6} \times 10(V_{GS} - 0.7)}$$

$$V_{GS} - 0.7 = 0.52 \text{ V}$$

$$V_{GS} = 1.22 \text{ V}$$

The p-Channel MOSFET

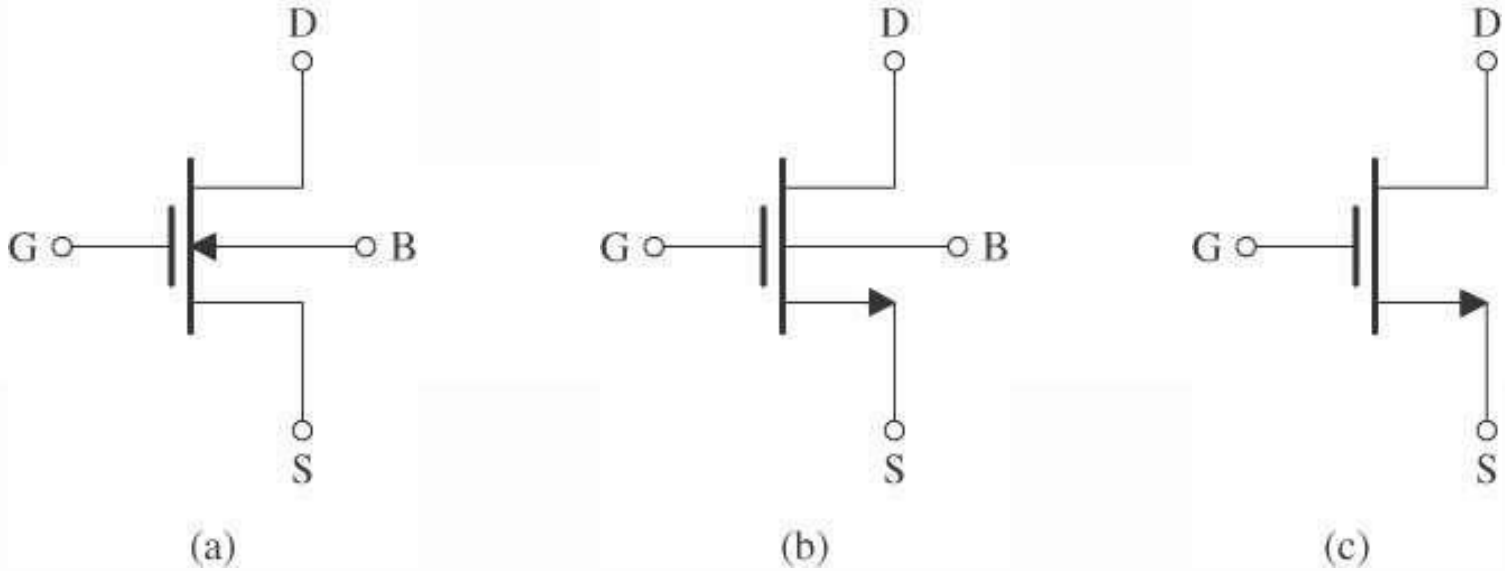
- Fabricated on an n-type substrate
- p + regions for the drain and source
- Has holes as charge carriers
- VGS and VDS are negative and the threshold voltage Vt is negative

It is important to be familiar with the PMOS transistor for two reasons:

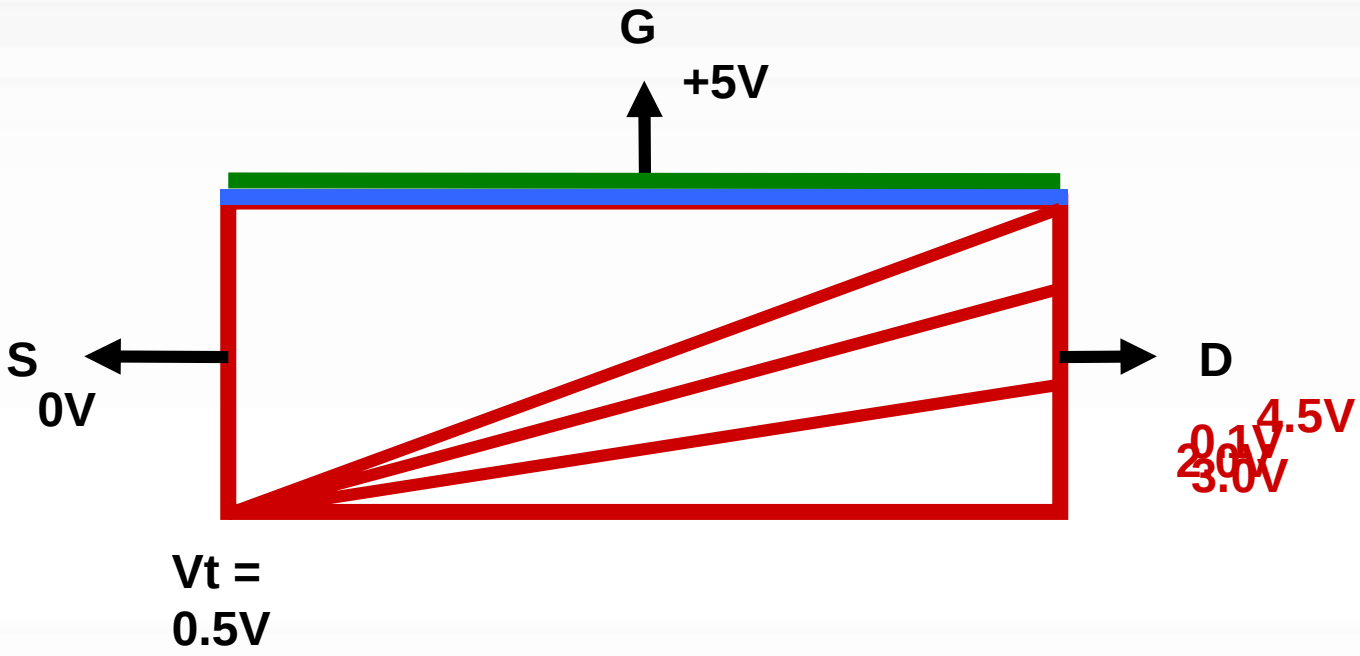
1. PMOS devices are still available for discrete-circuit design

2. Both PMOS and NMOS transistors are utilized in complementary MOS or CMOS circuits, which is currently the dominant MOS technology.

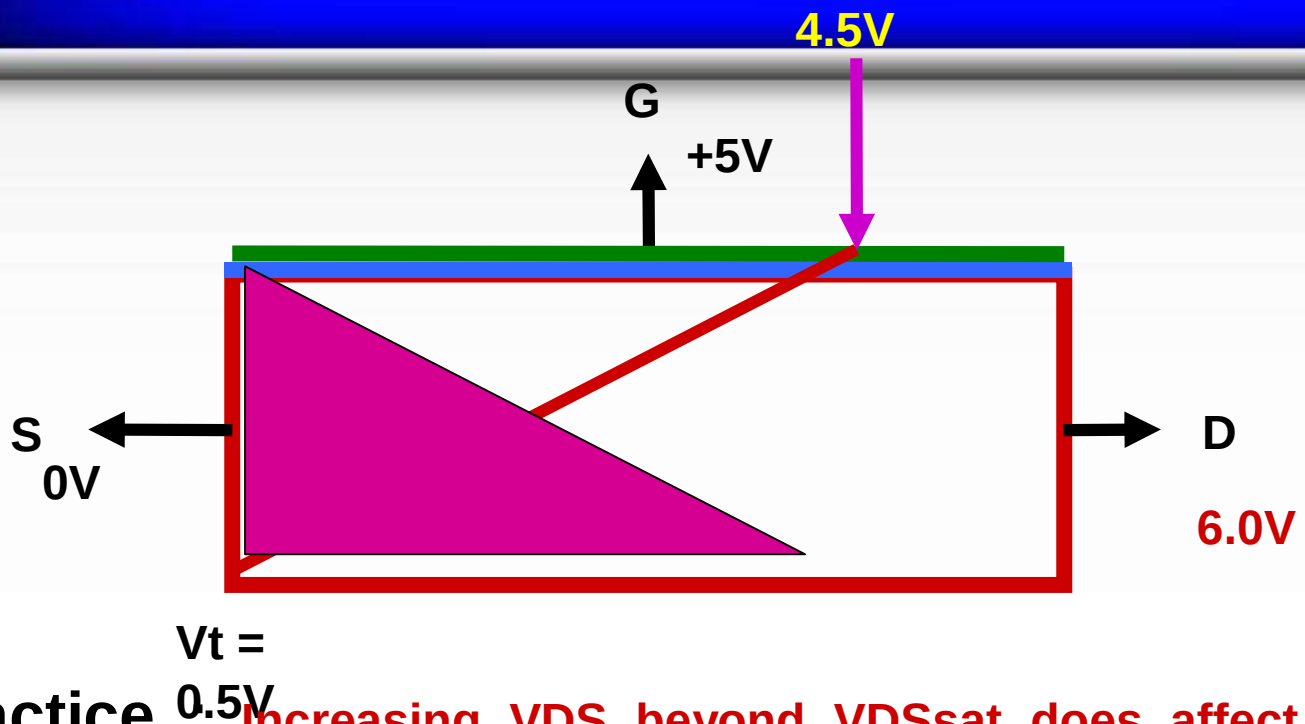
Circuit symbol for the *n*-channel enhancement-type MOSFET



Finite Output Resistance in Saturation

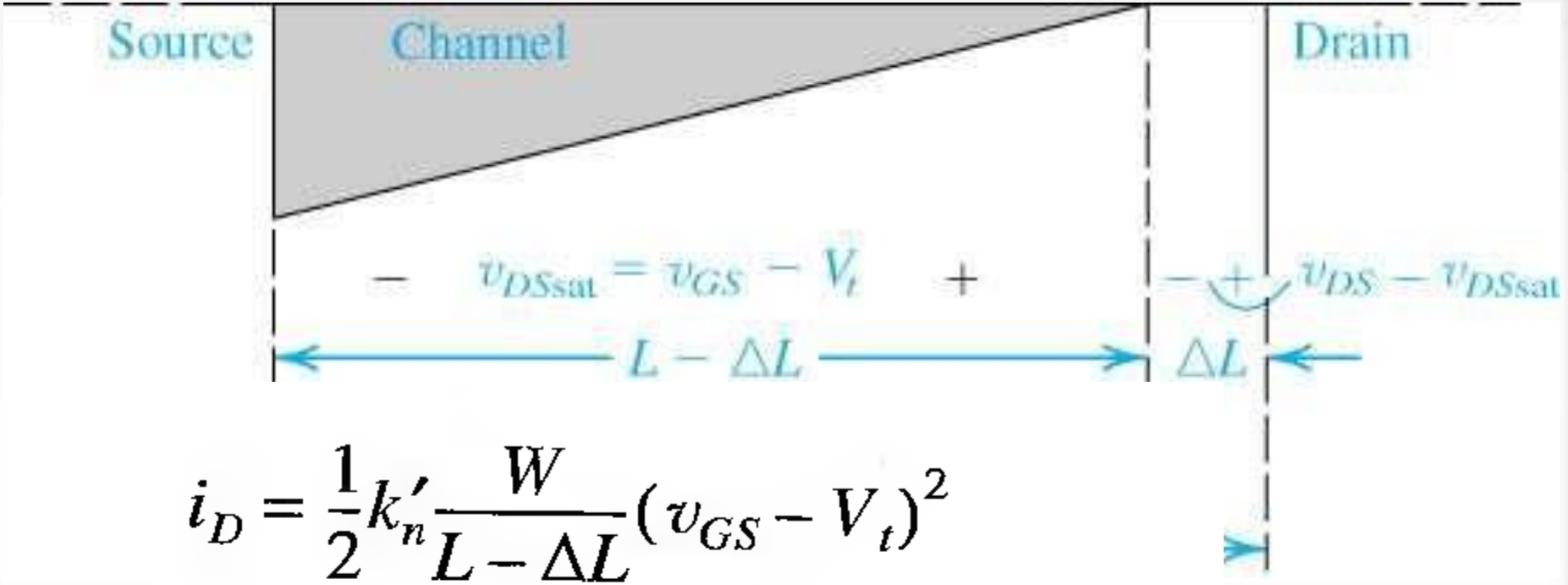


Ideal : ***Once the channel is pinched off at the drain end, further increases in VDS have no effect on the channel's shape.***



- **Practice :** Increasing VDS beyond VDSsat does affect the channel. Channel pinch-off point is moved slightly away from the drain, toward the source. The voltage across the channel remains constant at VGS - Vt = VDSsat. Additional voltage applied to the drain appears as a voltage drop across the narrow depletion region between the end of the channel and the drain region. This voltage accelerates the electrons that reach the drain end of the channel. The channel length is in effect reduced, from L to L – ΔL.

Phenomenon known as ***channel-length modulation*** . iD is inversely proportional to the channel length. iD increases with VDS



$$i_D = \frac{1}{2}k_n'\frac{W}{L-\Delta L}(v_{GS}-V_t)^2$$

$$= \frac{1}{2}k_n'\frac{W}{L}\frac{1}{1-(\Delta L/L)}(v_{GS}-V_t)^2$$

$$\cong \frac{1}{2}k_n'\frac{W}{L}\left(1+\frac{\Delta L}{L}\right)(v_{GS}-V_t)^2$$

$(\Delta L/L) \ll 1$

ΔL = □'
vDS

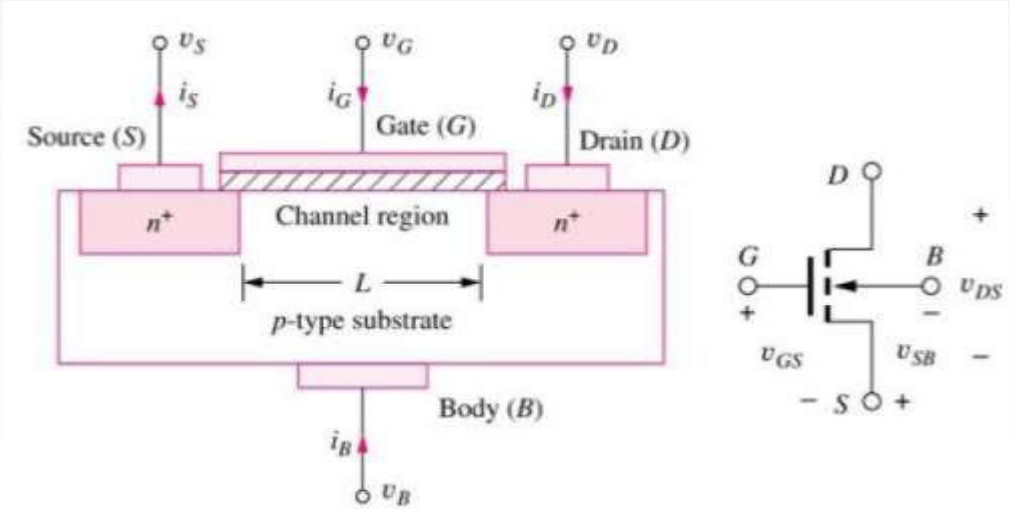
□' is a process-technology parameter with the dimensions of □m/V

$$i_D = \frac{1}{2} k_n' \frac{W}{L}\left(1 + \frac{\lambda'}{L} v_{DS}\right)(v_{GS} - V_t)^2$$

$$\lambda = \frac{\lambda'}{L}$$

$$i_D = \frac{1}{2} k_n' \frac{W}{L}(v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$

The Role of the Substrate - *The Body Effect*



- Source terminal connected to the substrate (or body) terminal B,
  - In ICs, the substrate is usually common to many MOS transistors.
  - Substrate connected to the most negative power supply in an NMOS circuit (most positive in a PMOS circuit).
- Resulting reverse-bias voltage between source and body (VSB) will have an effect on device operation.

Problem

To maintain the cutoff condition for all the substrate-to-channel junctions

The reverse bias voltage will widen the depletion region .This in turn reduces the channel depth. To return the channel to its former state, VGS has to be increased. The effect of VSB on the channel can be represented as a change in the threshold voltage Vt . Increasing the reverse substrate bias voltage VSB results in an increase in Vt .

$$V_t = V_{t0} + \gamma[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}]$$

Vto Threshold voltage for VSB = 0

□f Physical parameter with (2 □f) typically 0.6 V

□ Fabrication-process parameter

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_s}}{C_{ox}}$$

q Electron charge (1.6 x 10-19 C)

NA Doping concentration of the p-type substrate

□s Permittivity of silicon (11.7□0 = 11.7 x 8.854 x 10-14 = 1.04 X 10-12 F/cm)

The parameter □ has the dimension of □ V and is typically 0.4 V½

hannel Devices

VSB by I VSBI

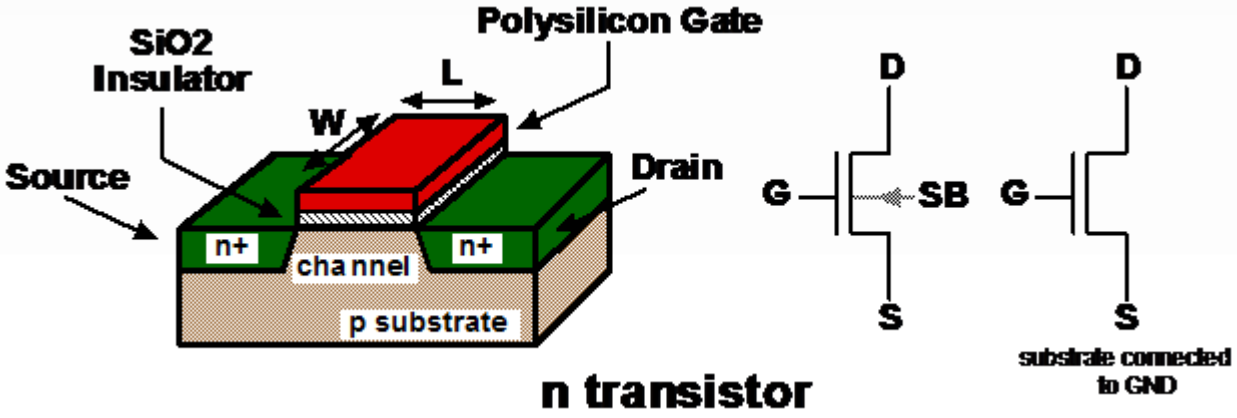
NA by ND ,

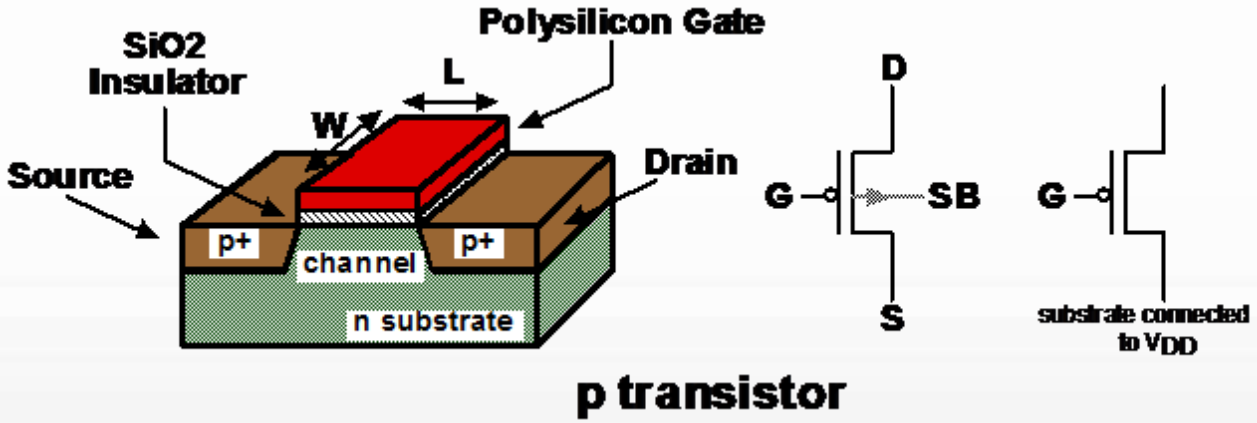
2□f is typically 0.75 V

□ is typically -0.5 V½ (Negative)

Review

Transistor Structure

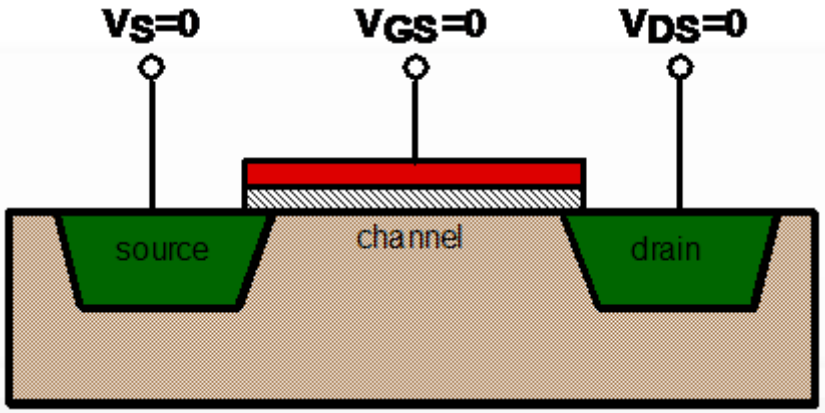




Review……

N Transistor Operation - Cutoff

- **Vgs << Vt : Transistor OFF**
  - Majority carrier in channel (holes)
  - No current from source to drain

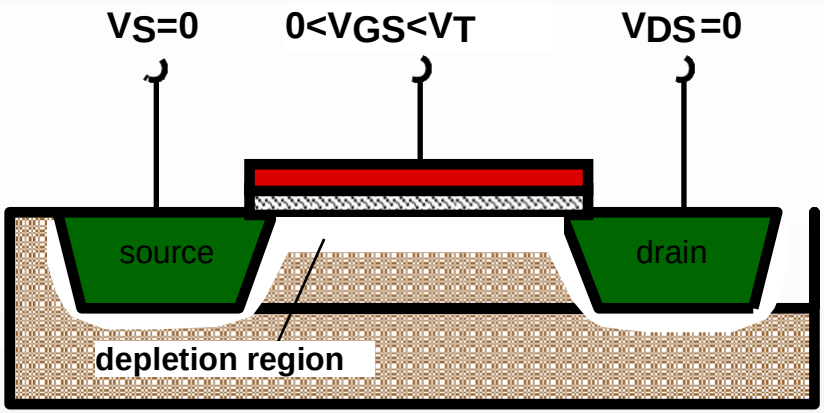


Some Values for Vtn:
Book (0.5µm) : 0.7V
AMI (1.5µm): 0.61V

Review……

N Transistor Operation - Subthreshold

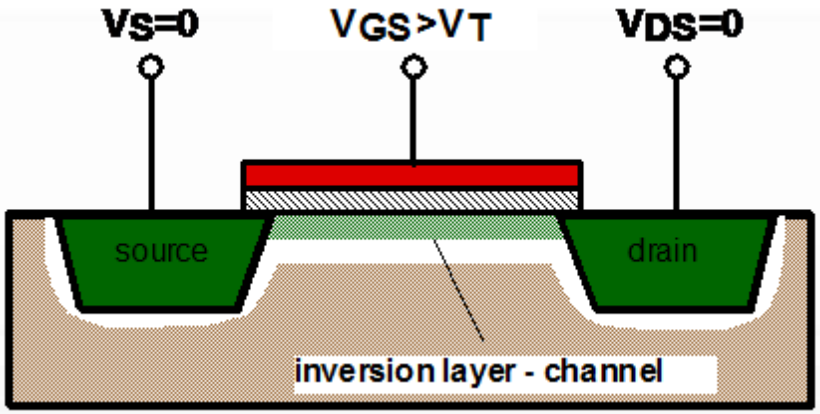
- **0 < Vgs < Vt : Depletion region**
  - Electric field repels majority carriers (holes)
  - Depletion region forms - no carriers in channel
  - No current flows (except for leakage current)



Review……

N Transistor Operation - ON

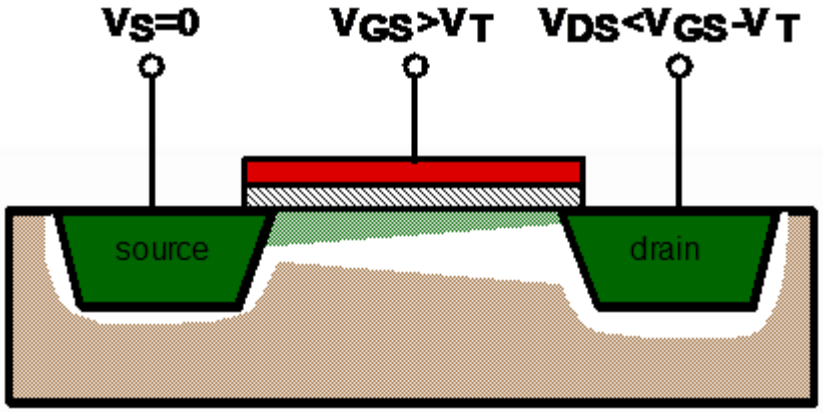
- **Vgs > Vt , VDS=0: Transistor ON**
  - **Electric field attracts minority carriers (electrons)**
  - **Inversion region forms in channel**
  - **Depletion region insulates channel from substrate**
  - **Current can now flow from drain to source!**



Review……

N Transistor Operation - Linear

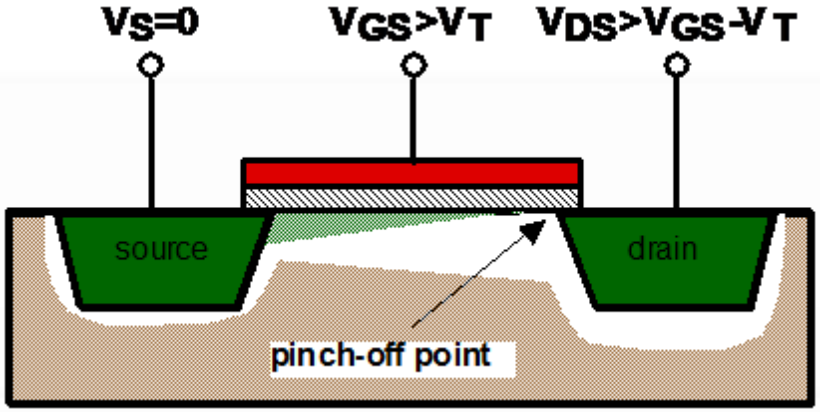
- **Vgs > Vt , VDS < VGS - Vt : Linear (Active) mode**
  - **Combined electric fields shift channel and depletion region**
  - **Current flow dependent on VGS, VDS**



Review……

N Transistor Operation - Saturation

- **Vgs > Vt , VDS >VGS -Vt : Saturated mode**
  - **Channel "pinched off"**
  - **Current still flows due to electron drift**
  - **Current flow dependent on VGS**



Review……

P Transistor Operation

- **Opposite of N-Transistor**
  - **Vgs >> Vt : Transistor OFF**
    - Majority carrier in channel (electrons)
    - No current from source to drain
  - **0 > Vgs > Vt : Depletion region**
    - Electric field repels majority carriers (electrons)
    - Depletion region forms - no carriers in channel
    - No current flows (except for leakage current)
  - **Vgs < Vt , VDS=0: Transistor ON**
    - Electric field attracts minority carriers (holes)
    - Inversion region forms in channel
    - Depletion layer insulates channel from substrate
    - Current can now flow from source to drain!

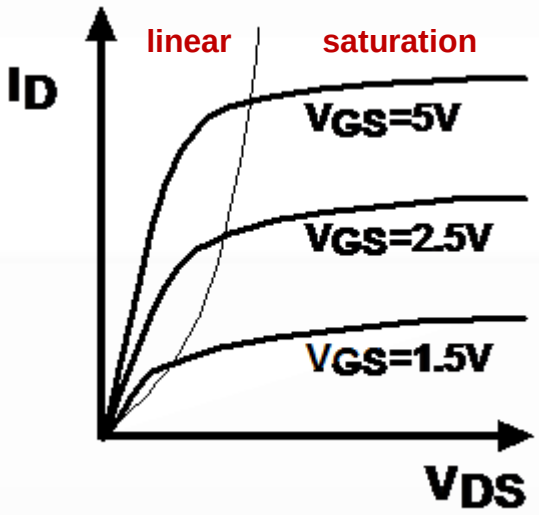
Review……

P Transistor Modes of Operation

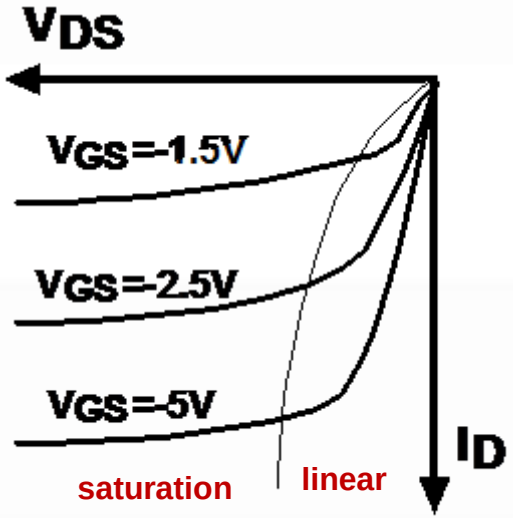
- **Vgs < Vt , VDS > VGS - VT : Linear (Active) mode**
- **Combined electric fields shift channel and depletion region**
- **Current flow dependent on VGS, VDS**
- **Vgs < Vt , VDS < VGS - VT : Saturation mode**
- **Channel "pinched off"**
- **Current still flows due to hole drift**
- **Current flow dependent on VGS**

Some Values for Vtp:
Book (0.5µm) : -0.8V
AMI (1.5µm): -1.02V

I-V Characteristics of MOS Transistors



n transistor

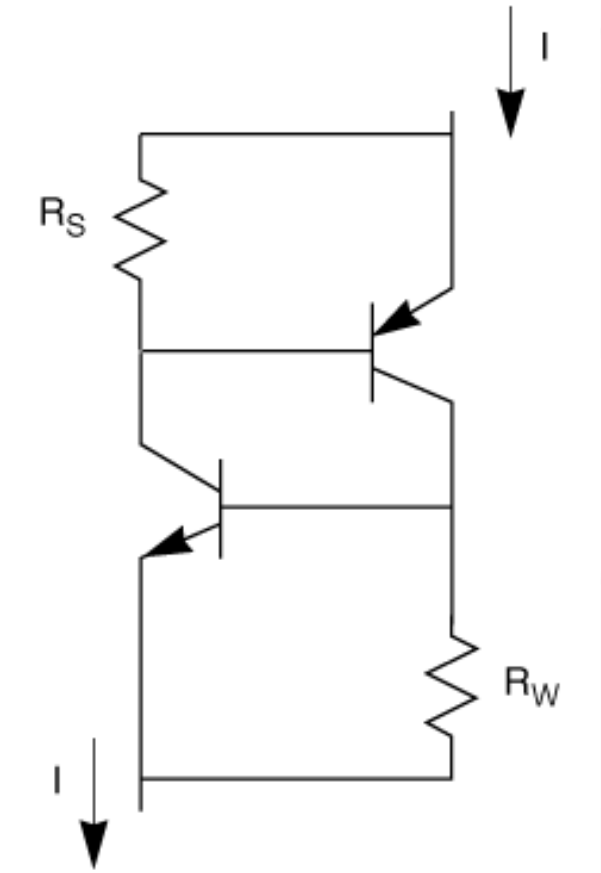


p transistor

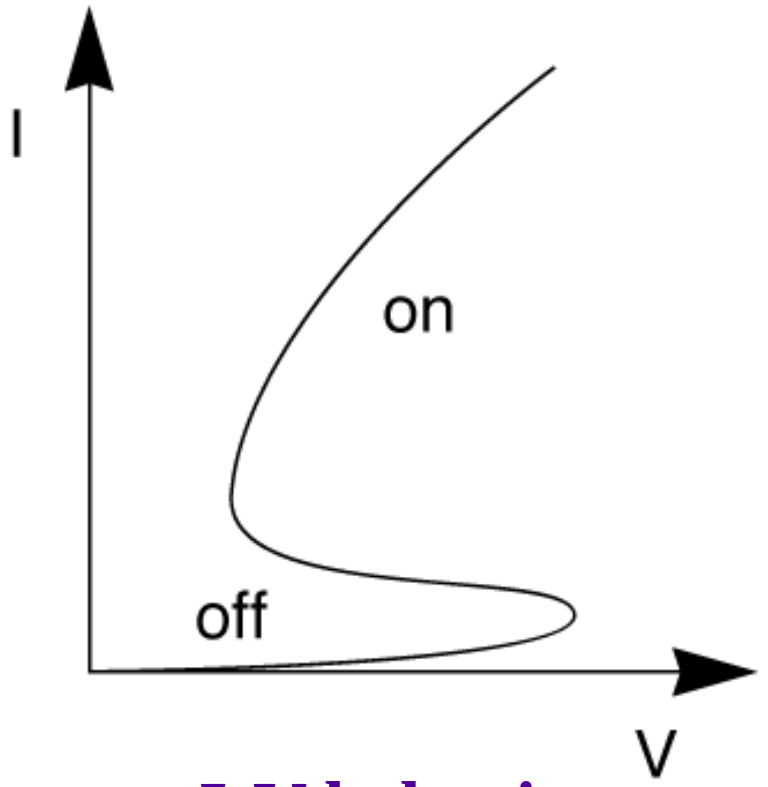
Latch-up

- CMOS ICs have parasitic silicon-controlled rectifiers (SCRs).
- When powered up, SCRs can turn on, creating low-resistance path from power to ground. Current can destroy chip.
- Early CMOS problem. Can be solved with proper circuit/layout structures.

Parasitic SCR



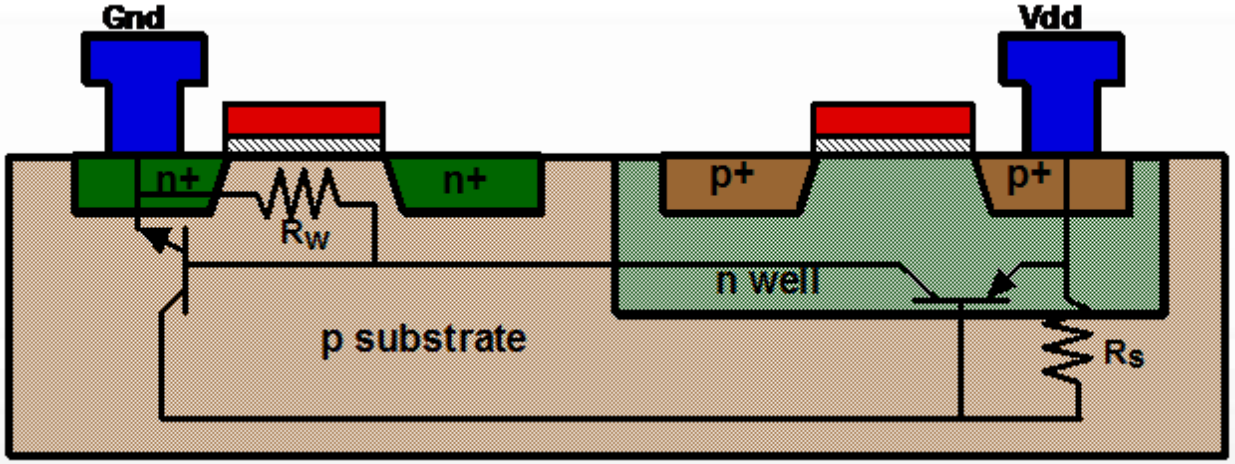
Circuit



I-V behavior

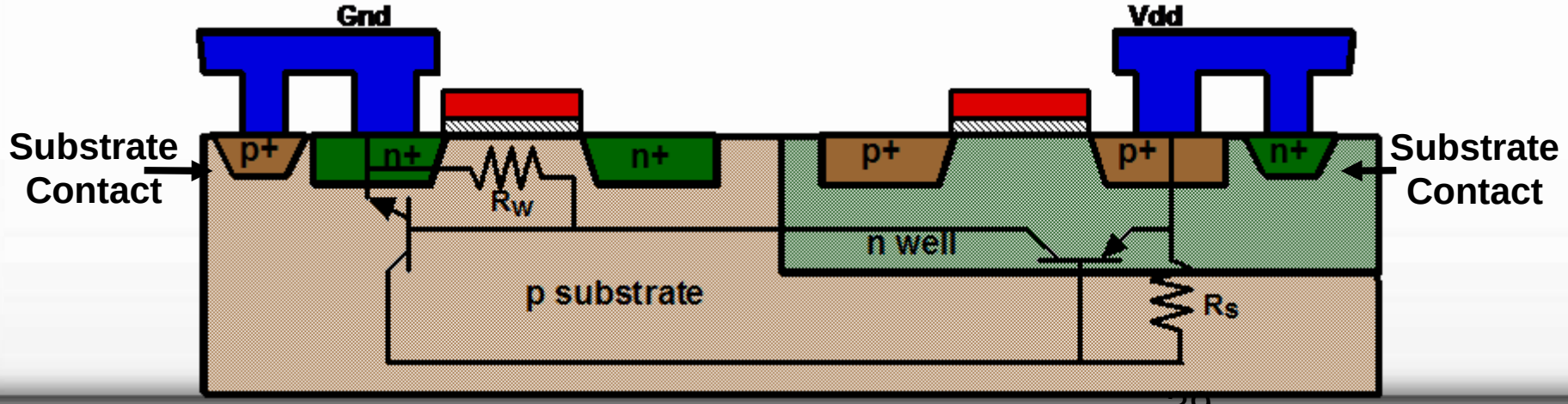
Parasitic Transistors

- Parasitic bipolar transistors form at N/P junctions
- Latchup - when parasitic transistors turn on
- Preventing latchup:
  - Add substrate contacts ("tub ties") to reduce Rs, Rw
    OR
  - Use Silicon-on-Insulator



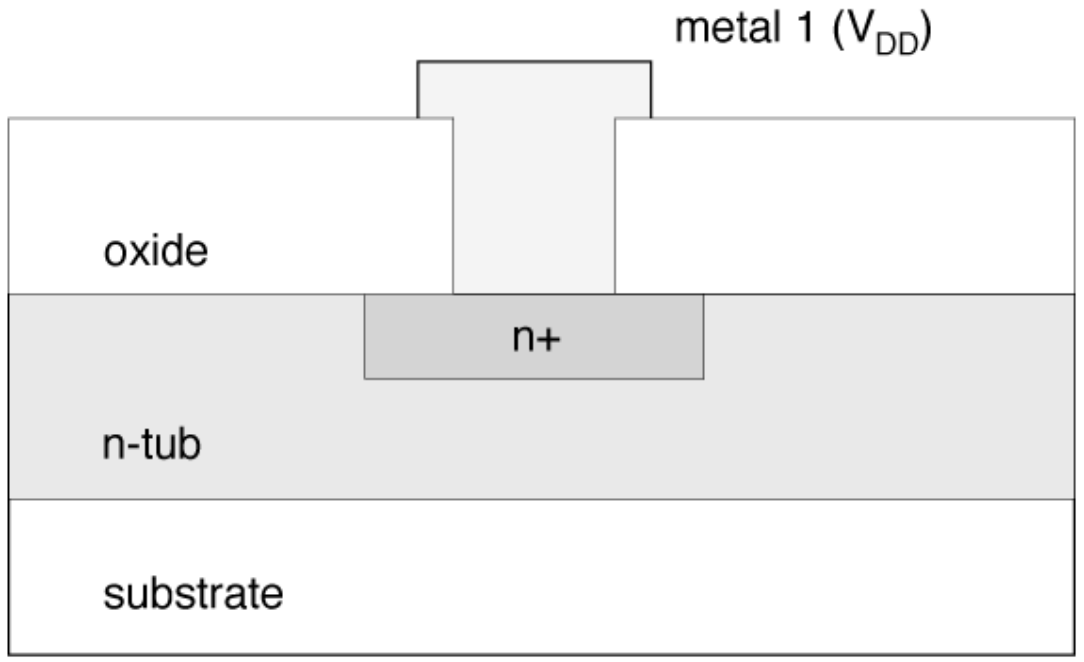
Controlling Latchup - Substrate Contacts

- Purpose: connect well/substrate to power supply
- Alternative term: tub tie
- Recommendations (source: Weste & Eshraghian)
  - Conservative: 1 substrate contact for every supply connection
  - Less conservative: 1 substrate contact for every 5-10 transistors
  - High-current circuits: use guard rings



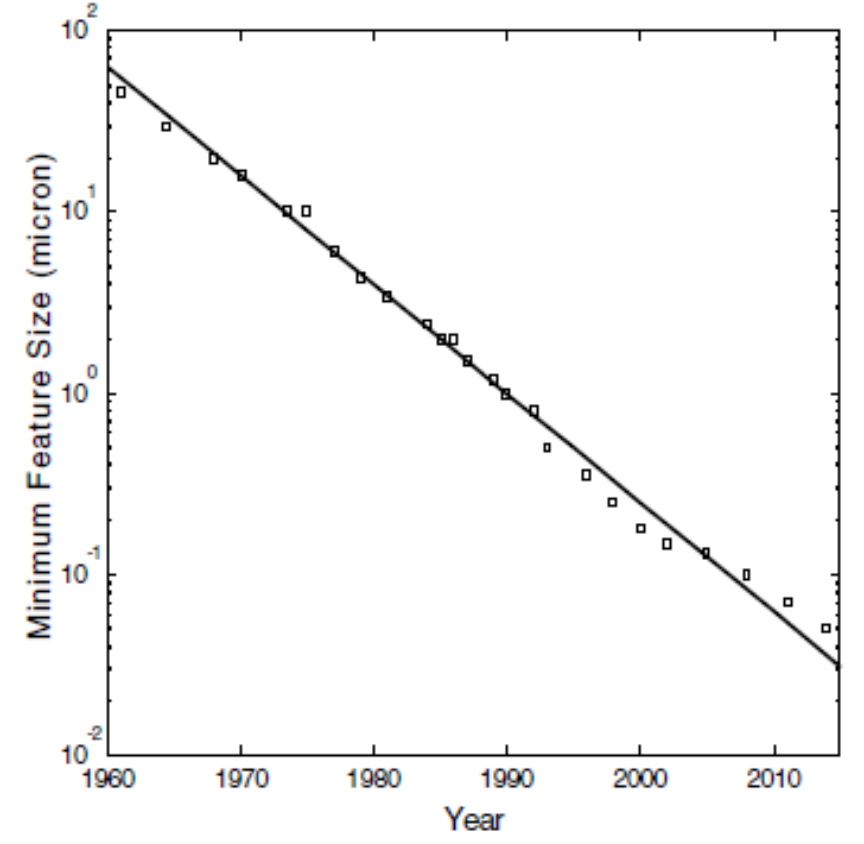
Solution to latch-up

Use tub ties to connect tub to power rail. Use enough to create low-voltage connection.



Scaling of CMOS

Advances in device manufacturing technology allow for a steady reduction of the minimum feature size such as the minimum transistor channel length realizable on a chip.



Evolution of (average) minimum channel length of MOS transistors over time.

Scaling of CMOS….

- Scaling refers to the systematic reduction of transistor dimensions from one generation to the next.
- It reduces the parasitic capacitances and also the carrier transit times in the devices.
- Improves the circuit speed.
- It narrows the performance gap between CMOS and logic gates based on bipolar transistors.
- Reduction of the transistor dimensions improves the packing density of CMOS.

Full Scaling of CMOS

- "**Full Scaling**," involves scaling all dimensions and voltages by the same factor, 1/s, where s is greater than one.

- Scaling factor of 1/□2 is used (*s* = □2 *),* then the *packing density* in transistors per square centimeter will be doubled.

- The goal is to keep the electrical field patterns in the scaled device identical to those in the original device.

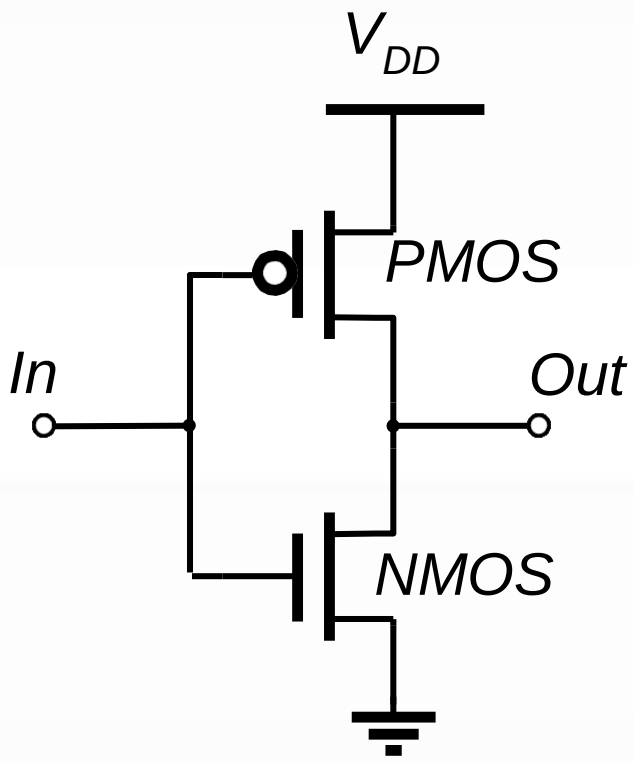
- Keeping the electrical fields constant ensures the physical integrity of the device and avoids breakdown or other secondary effects.

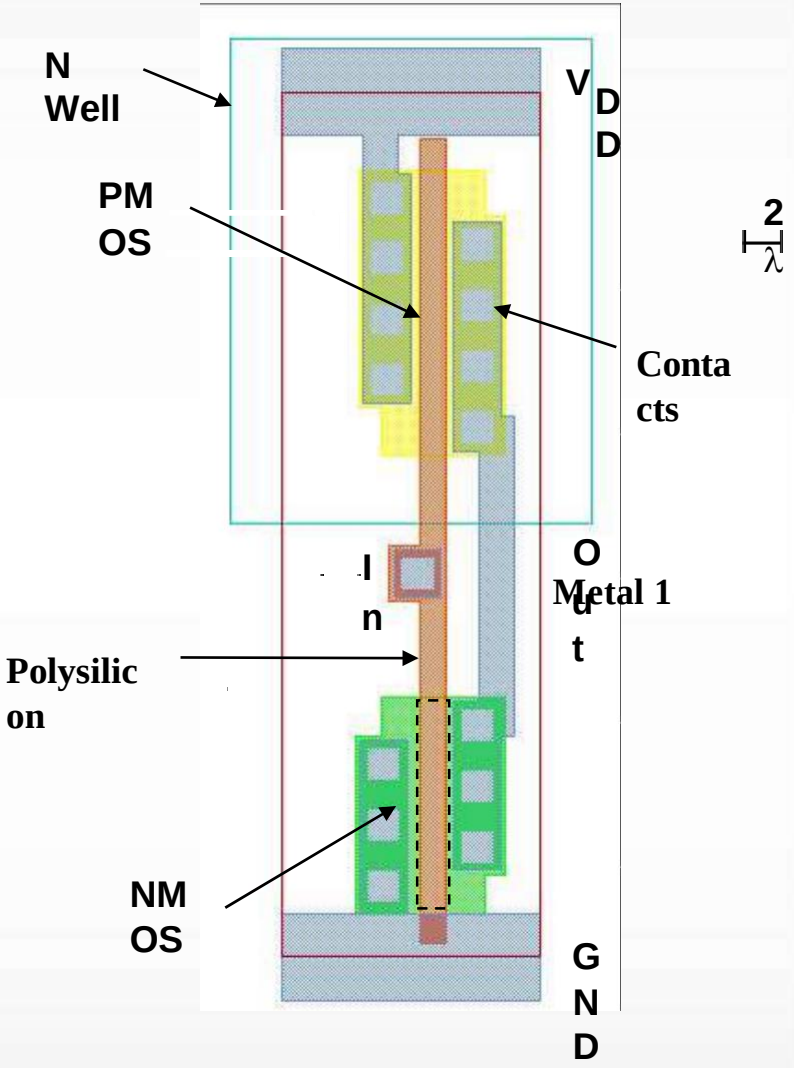
- This scaling leads to greater device density (*Area), higher performance (Intrinsic Delay), and reduced power consumption (P).*

Full Scaling of CMOS

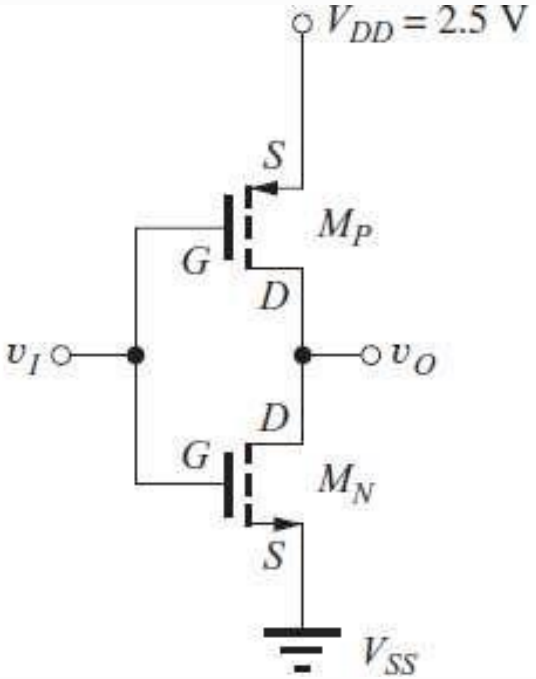
Parameter	Relationship	Scales by
L	-	1/s
W	-	1/s
t_{ox}	-	1/s
V_{DD}	-	1/s
C_{OX}	$\frac{\varepsilon_{ox} WL}{t_{ox}}$	1/s
K	$\frac{W}{L}\frac{\mu\varepsilon_{ox}}{t_{ox}}$	s
t_p	$\propto \frac{C_L}{V_{DD}K} \propto \frac{C_{ox}}{V_{DD}K}$	1/s
P	$fC_L V_{DD}^2$	$1/s^3$
Packing Density	-	s^2
Power Density	-	1/s

CMOS Inverter

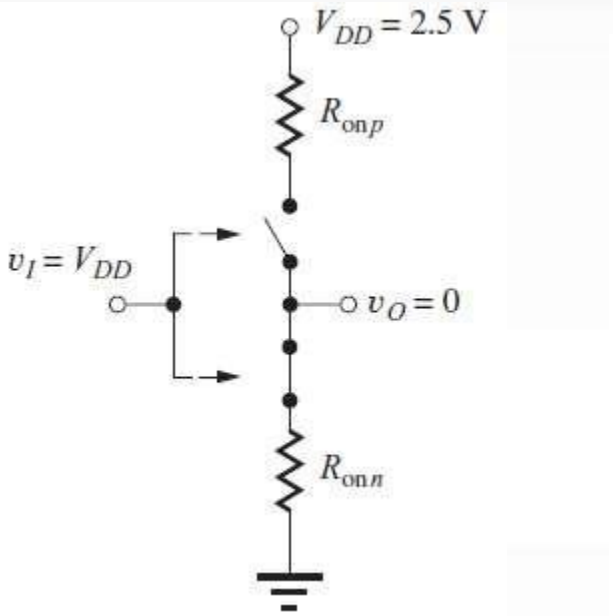




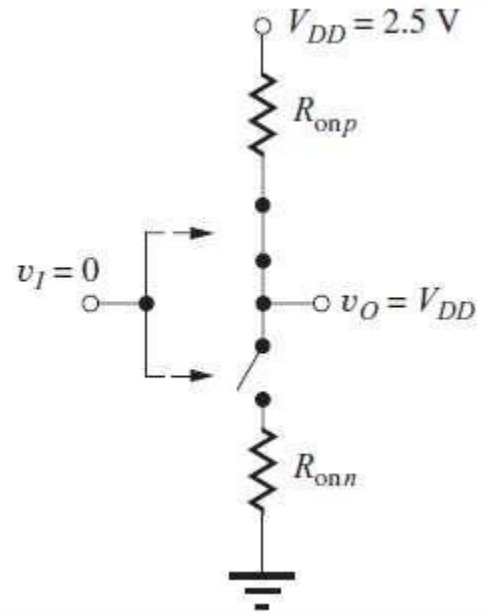
CMOS INVERTER



A CMOS inverter uses one NMOS and one PMOS transistor.



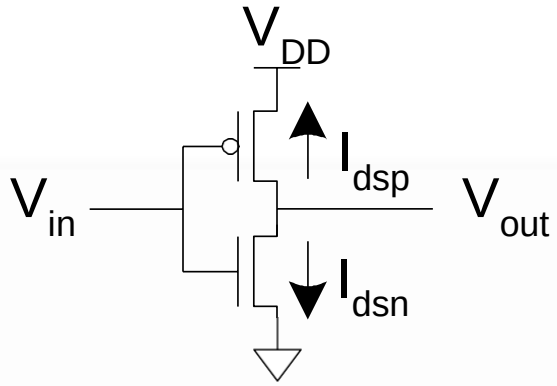
A simplified model of the inverter for a high input level. The output is forced to zero through the on-resistance of the NMOS transistor.



Simplified model of the inverter for a low input level. The output is pulled to *VDD through the on-resistance of the PMOS transistor.*

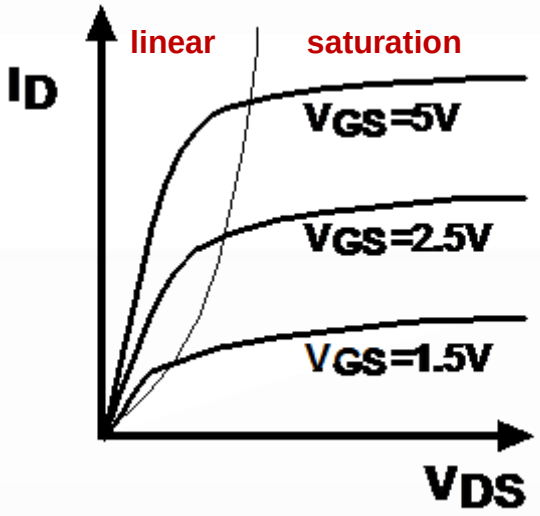
CMOS Inverter - DC Response

- DC Response: Vout vs. Vin for a gate
- Ex: Inverter
  - When Vin = 0 -> Vout = VDD
  - When Vin = VDD -> Vout = 0
  - In between, Vout depends on transistor size and current
  - By KCL, must settle such that Idsn = |Idsp|
  - We could solve equations
  - But graphical solution gives more insight



Transistor Operation

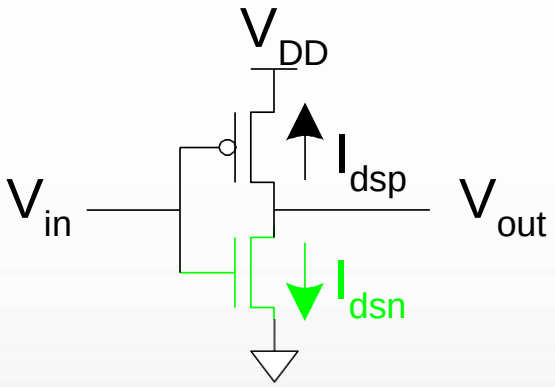
- Current depends on region of transistor behavior
- For what Vin and Vout are NMOS and PMOS in
  - Cutoff?
  - Linear?
  - Saturation?



n transistor

NMOS Operation

Cutoff	Linear	Saturated
Vgsn	Vgsn Vdsn < Vgsn – Vtn Vout < Vin - Vtn	Vgsn Vdsn > Vgsn – Vtn Vout > Vin - Vtn



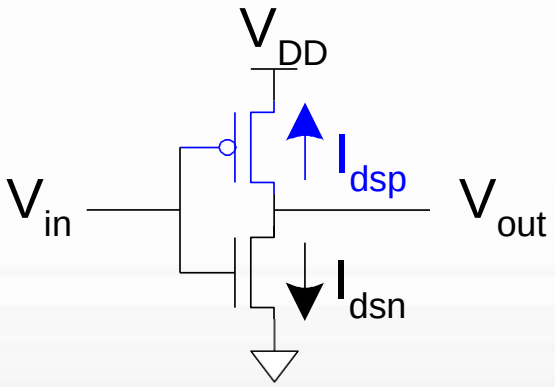
PMOS Operation

Cutoff	Linear	Saturated
Vgsp < Vtp Vin < VDD + Vtp	Vgsp < Vtp Vin < VDD + Vtp Vdsp > Vgsp – Vtp Vout > Vin – Vtp	Vgsp < Vtp Vin < VDD + Vtp Vdsp < Vgsp – Vtp Vout < Vin - Vtp

Vgsp = Vin - VDD

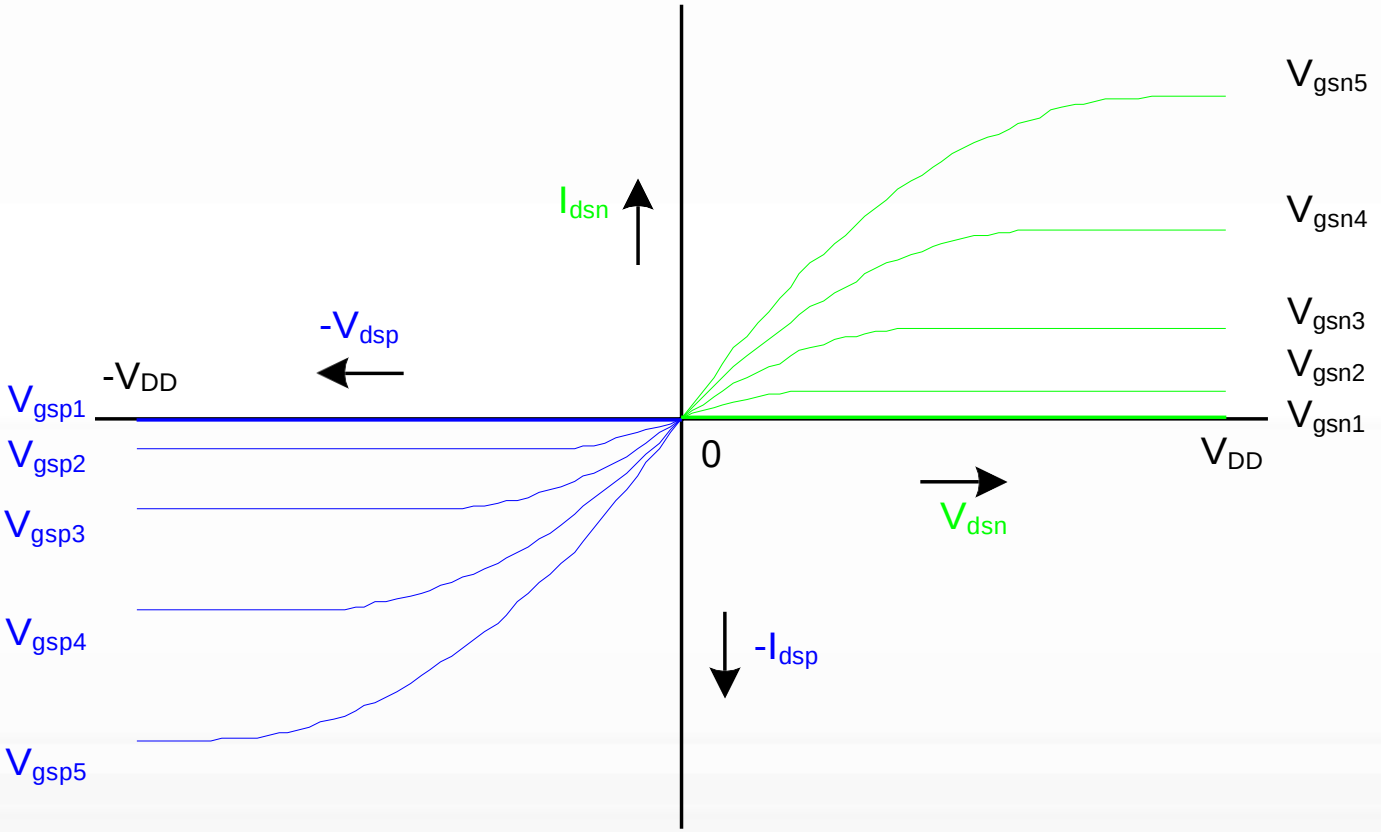
Vdsp = Vout - VDD

Vtp < 0

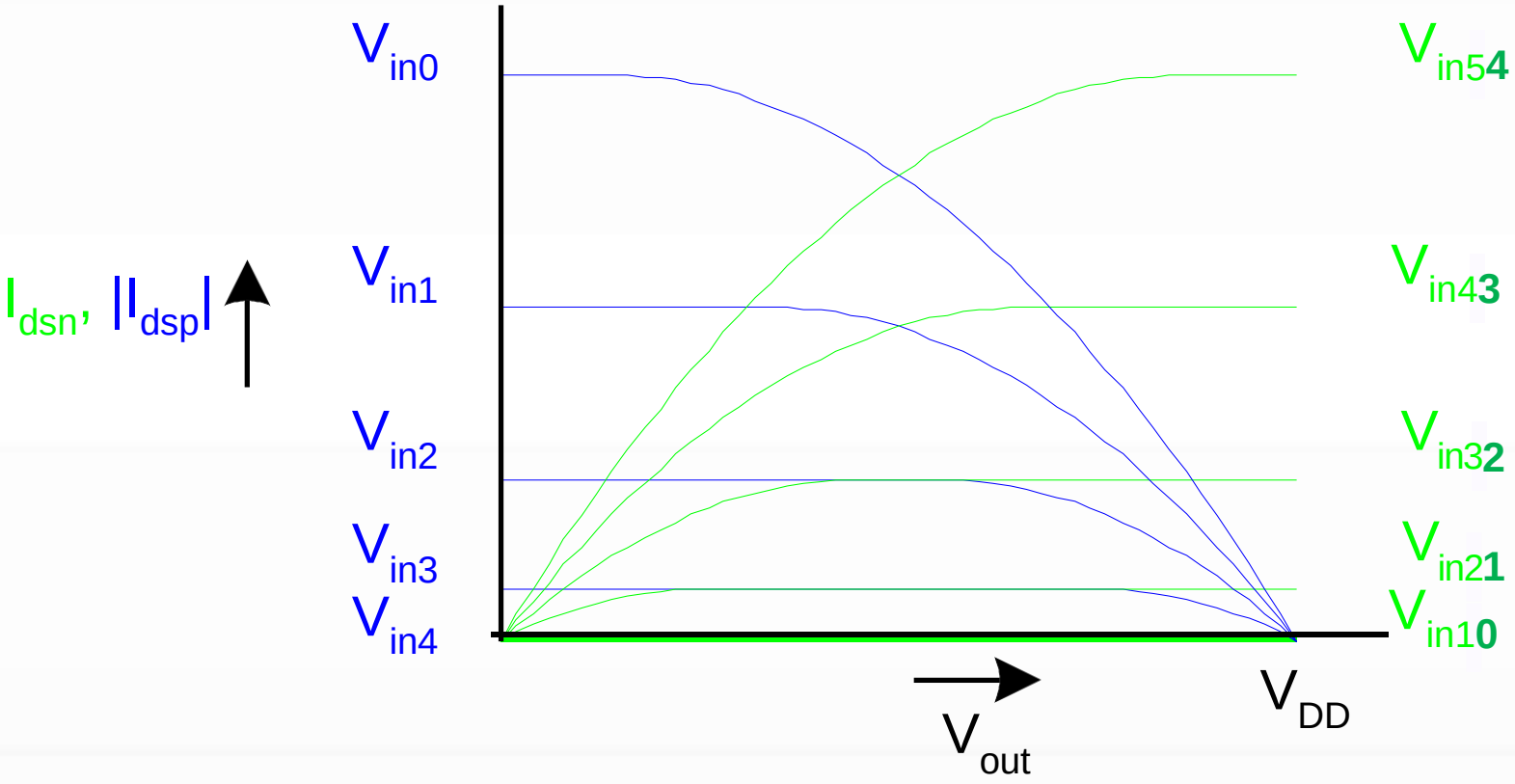


I-V Characteristics

- Make PMOS is wider than NMOS such that Kn = Kp

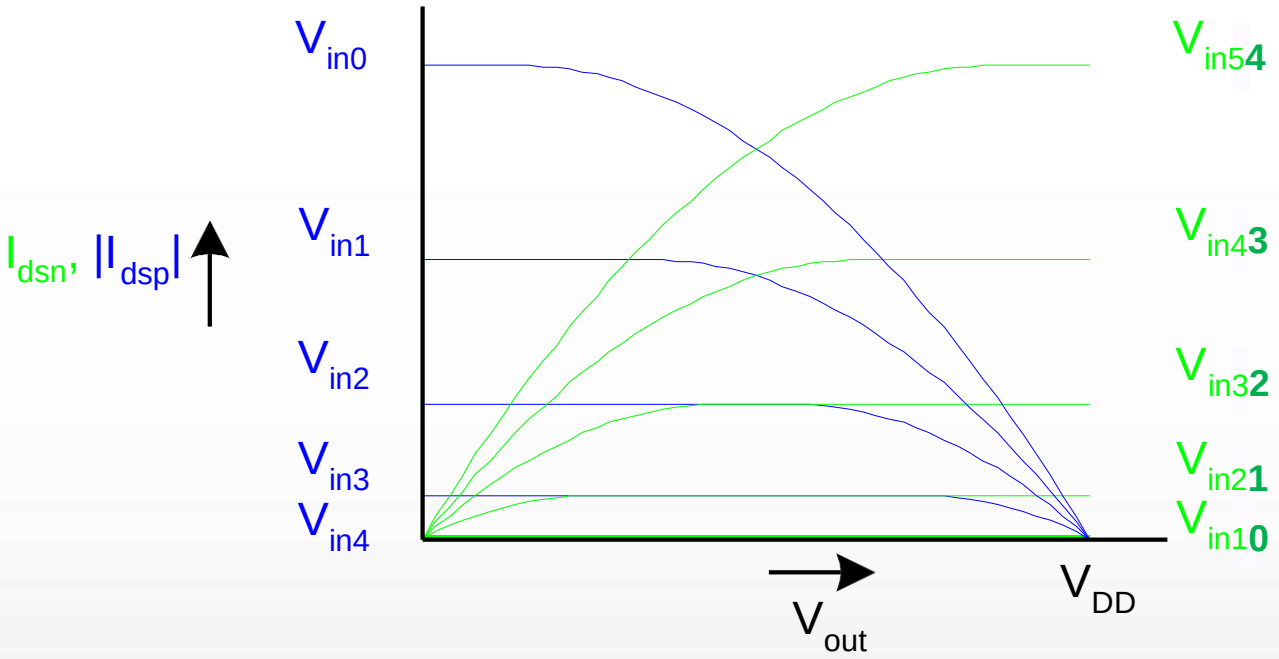


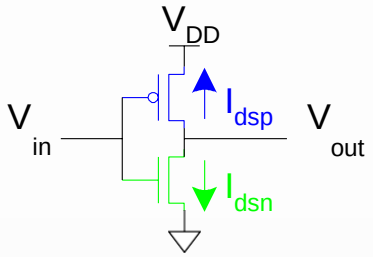
Current vs. Vout, Vin



Load Line Analysis

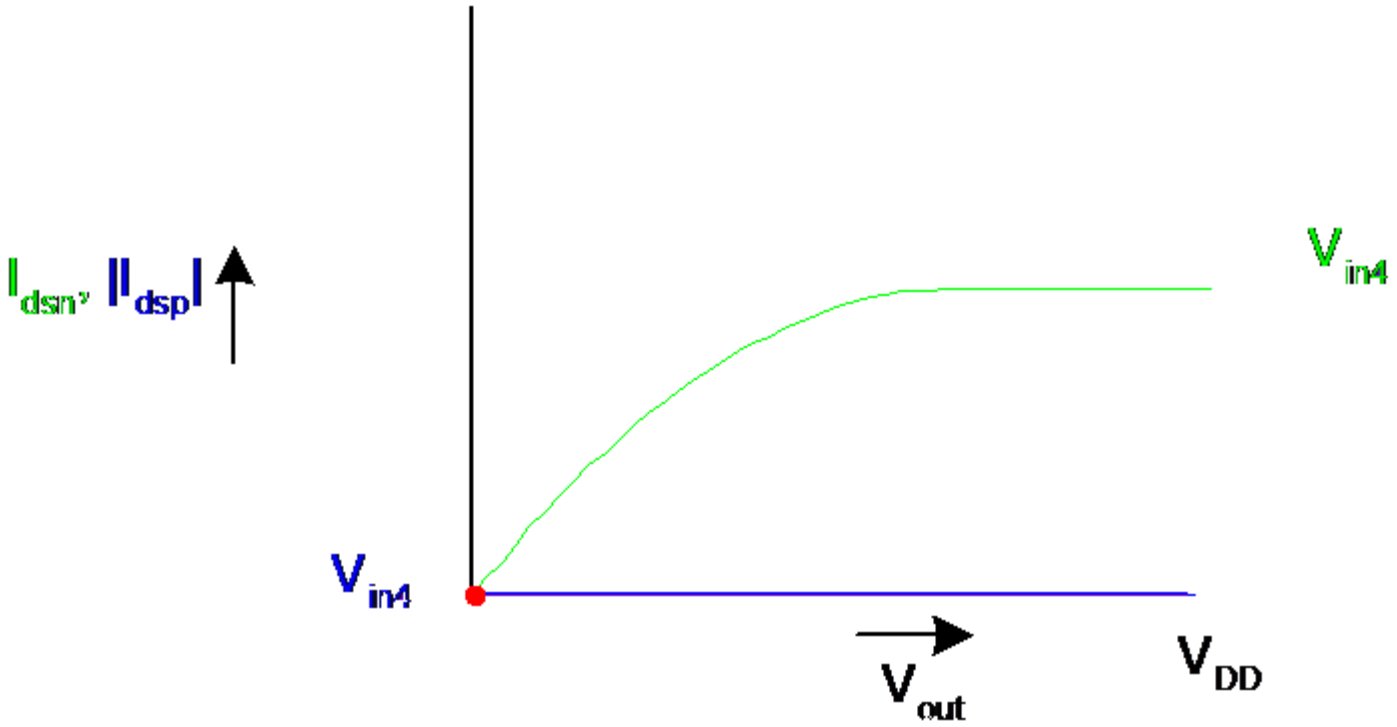
- For a given Vin:
  - Plot Idsn, Idsp vs. Vout
  - Vout must be where |currents| are equal in magnitude



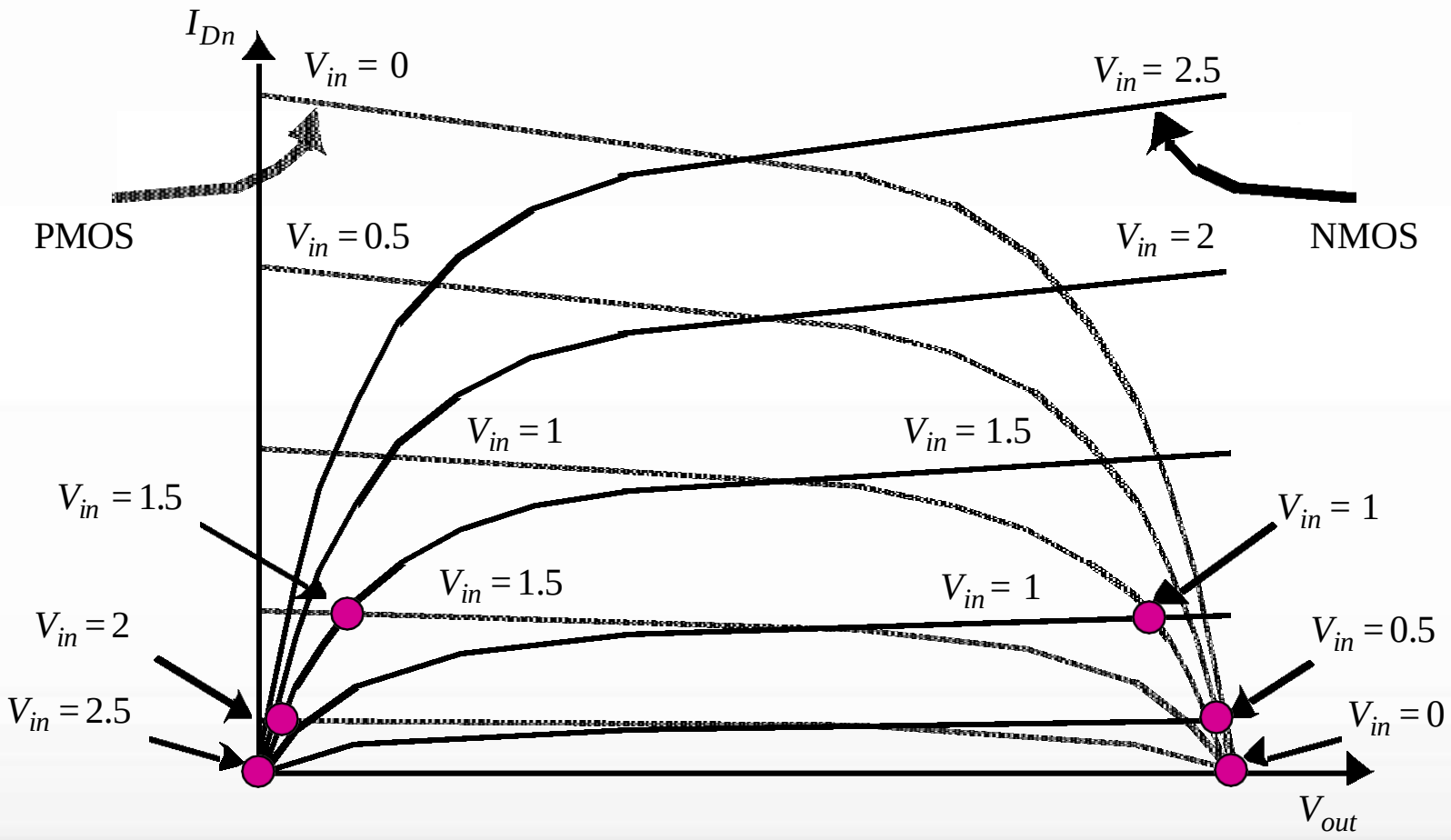


Load Line Analysis

- **Vin =** 0.8VDD

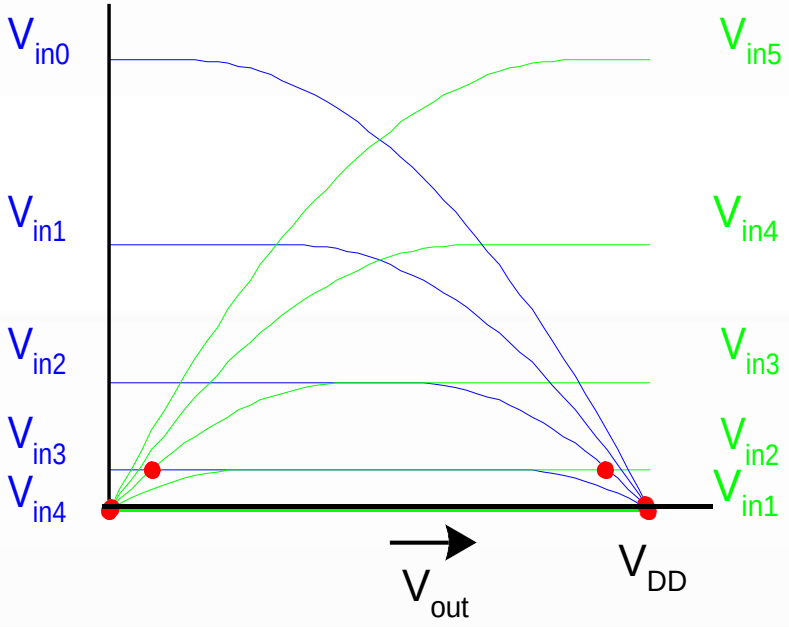


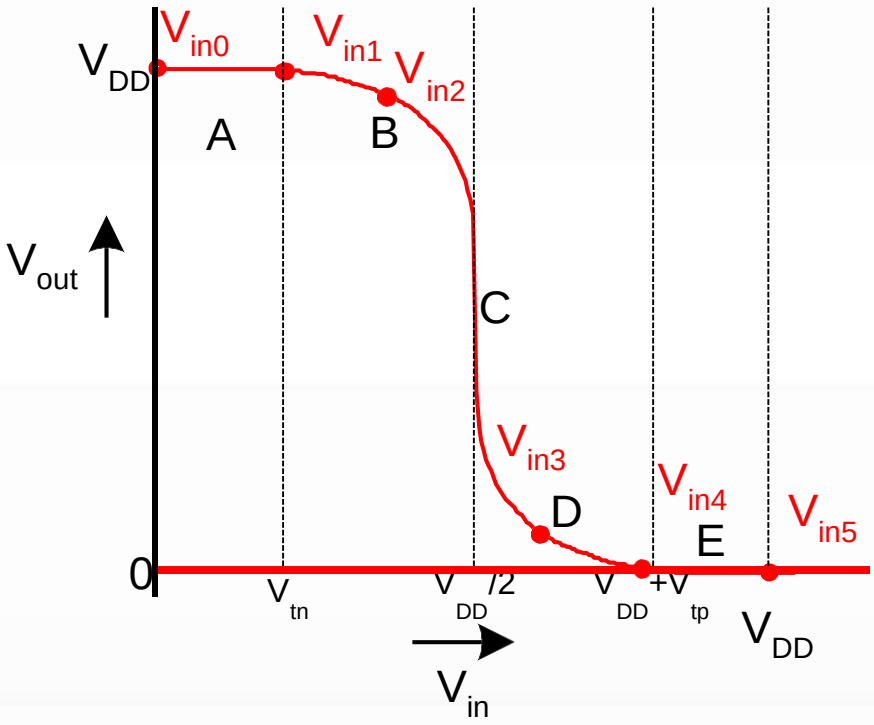
CMOS Inverter Load Characteristics



DC Transfer Curve

- Transcribe points onto Vin vs. Vout plot

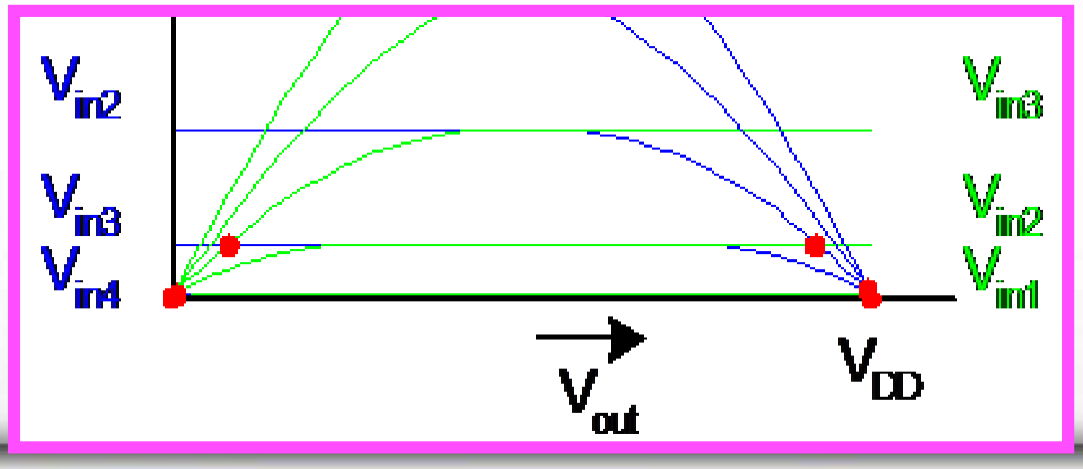


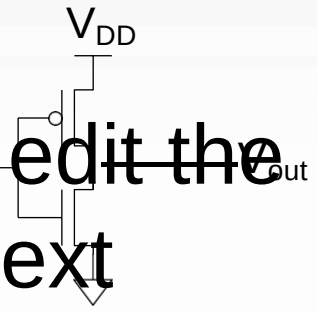


Operating Regions

- Revisit transistor operating regions

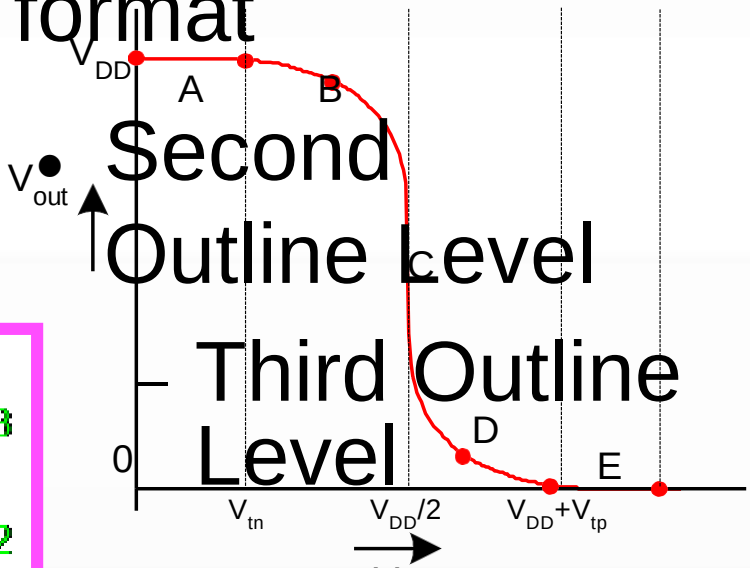
Region	NMOS	PMOS
A		
B		
C		
D		
E		





Click to edit the outline text format

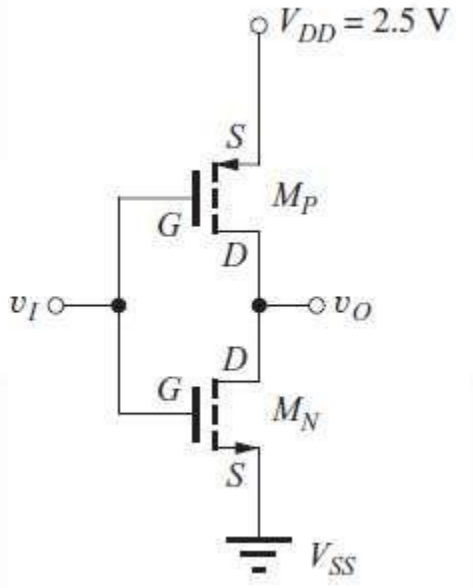
- Second Outline Level
  - Third Outline Level
    - Fourth Outline



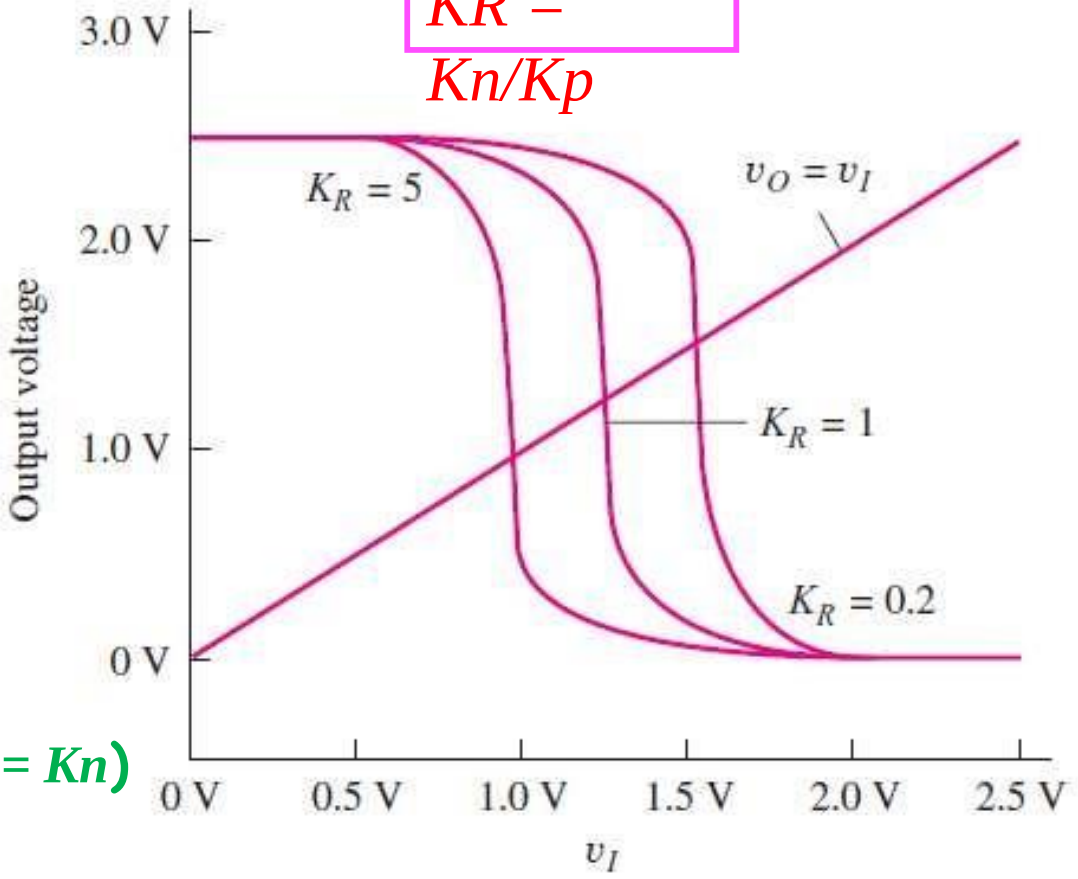
el

V_{DD}

CMOS voltage transfer characteristics



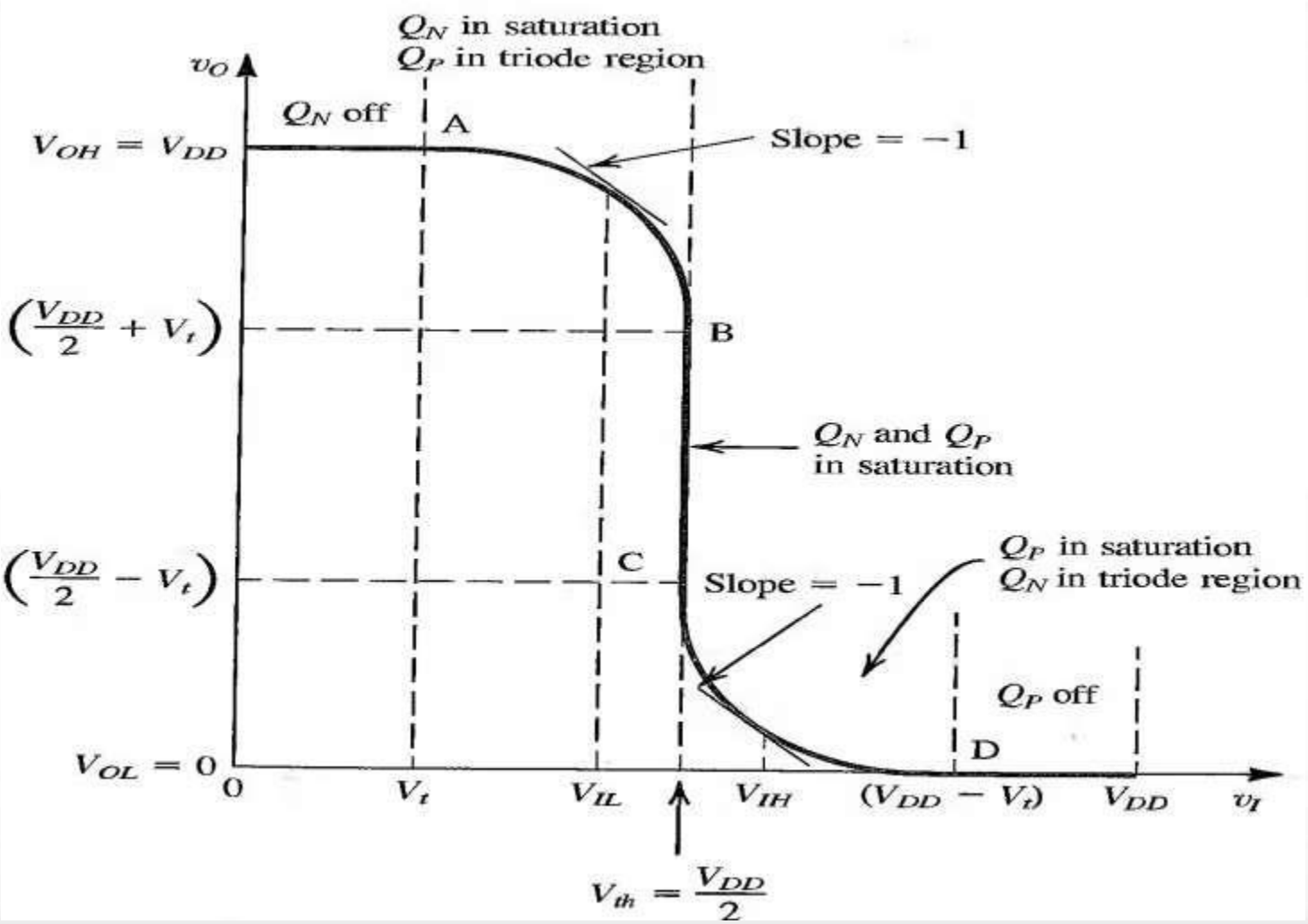
$KR = \frac{Kn}{Kp}$



Symmetrical design ($Kp = Kn$)

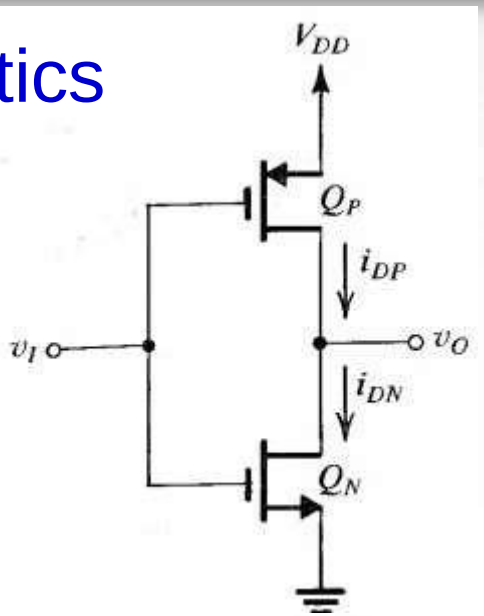
If $Kp \neq Kn$, then the transition shifts away from VDD/2.

CMOS voltage transfer characteristics



CMOS voltage transfer characteristics

Calculate the critical points of the resulting voltage transfer curve. For this we need the *i- v* relationships of QN and QP .



For QN

$$i_{DN} = k_n' \left(\frac{W}{L}\right)_n \left[(v_I - V_{tn})v_O - \frac{1}{2}v_O^2\right] \qquad \text{for } v_O \le v_I - V_{tn}$$

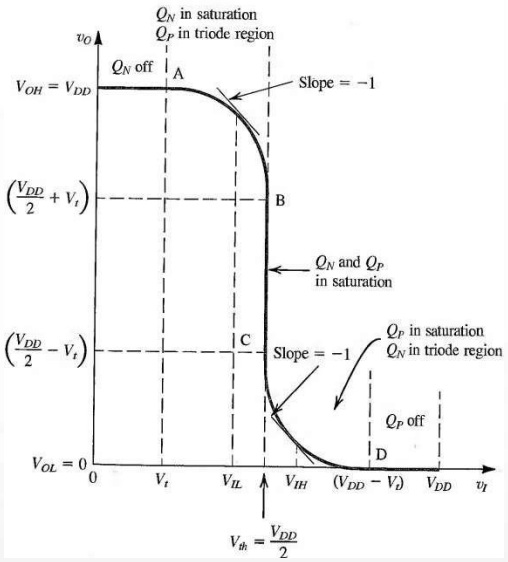
$$i_{DN} = \frac{1}{2}k_n' \left(\frac{W}{L}\right)_n (v_I - V_{tn})^2 \qquad \text{for } v_O \ge v_I - V_{tn}$$

For QP

$$i_{DP} = k_p' \left(\frac{W}{L}\right)_p \left[(V_{DD} - v_I - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - v_O)^2\right]$$

$$\text{for } v_O \ge v_I + |V_{tp}|$$

$$i_{DP} = \frac{1}{2}k_p' \left(\frac{W}{L}\right)_p (V_{DD} - v_I - |V_{tp}|)^2 \qquad \text{for } v_O \le v_I + |V_{tp}|$$



CMOS voltage transfer characteristics…..

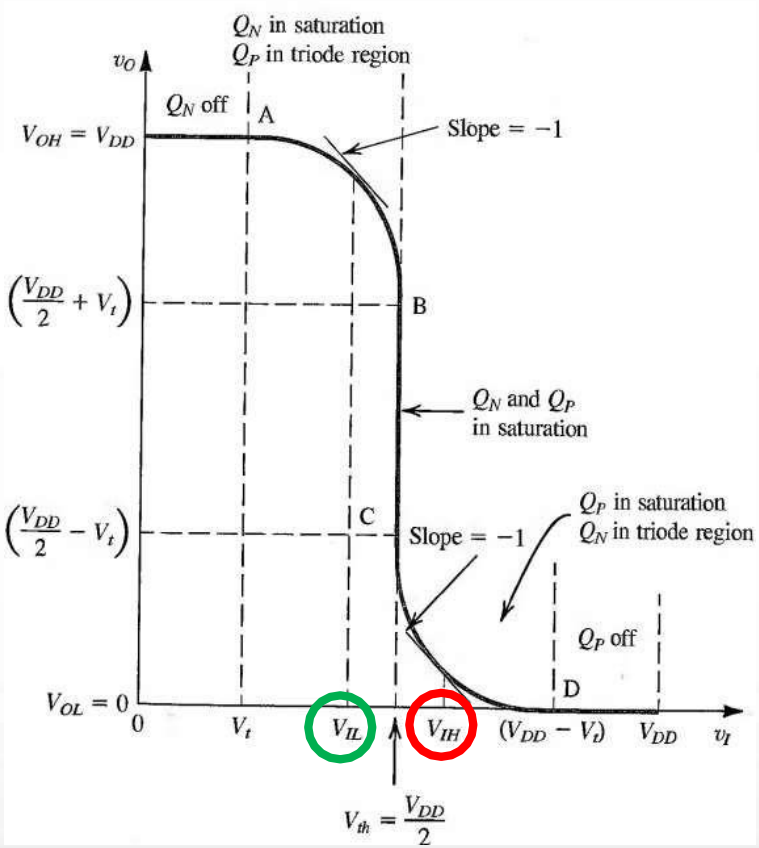
- CMOS inverter is usually designed to have *Vtn* = |*Vtp*| = *Vt and kn'(W/L)n = k'p(WIL)p*
- □p is 0.3 to 0.5 times □n. Kn and Kp should be equal.
- *The width of the p-channel device is made two to* three times that of the n-channel device.
- The two devices are designed to have equal lengths, with widths related by (Wp / Wn) = (□p / □n)
- This will result in k'n(W / L)n = k'p(W / L)p (KN = KP) and the inverter will have a symmetric transfer characteristic and equal current-driving capability in both directions (pull-up and pull-down).

CMOS voltage transfer characteristics…..

VIL — Maximum permitted logic-0 or "low" level at the input.

VIH — Minimum permitted logic-1or "high" level at the input.

Above are formally defined as the two points on the transfer curve at which the incremental gain is unity. (i.e. the slope is =1 V/ V).



CMOS voltage transfer characteristics…..

To determine *VIH :* *QN is in the triode region QP is in salutation* (KN = KP)

Equating *iDN* and *iDP and assume matched devices* (KN = KP)

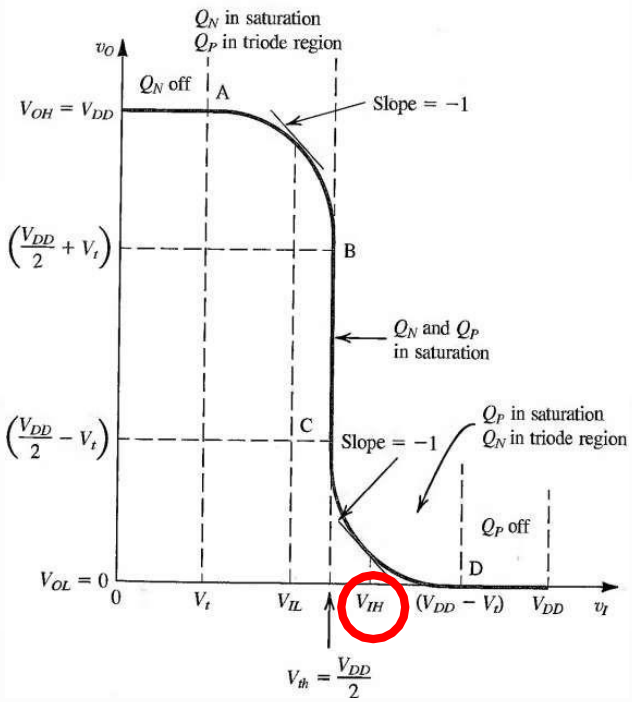
$$(v_I - V_t)v_O - \frac{1}{2}v_O^2 = \frac{1}{2}(V_{DD} - v_I - V_t)^2$$

Differentiating both sides relative to ***vI***

$$(v_I - V_t)\frac{dv_O}{dv_I} + v_O - v_O\frac{dv_O}{dv_I} = -(V_{DD} - v_I - V_t)$$

Substitute *vI = VIH and dvO/dvI = -1 to obtain*

$$v_O = V_{IH} - \frac{V_{DD}}{2}$$



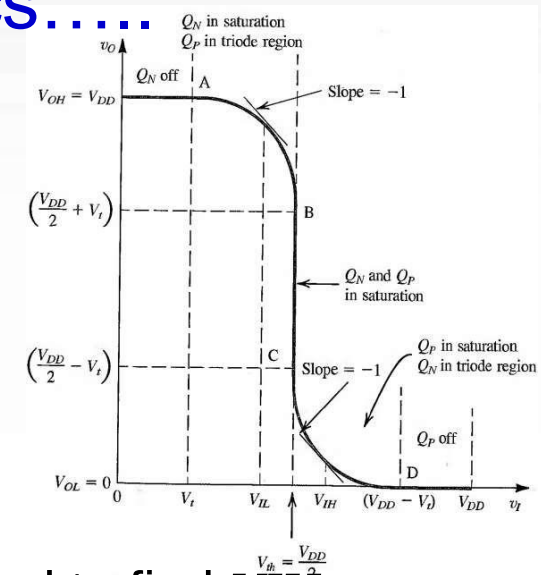
CMOS voltage transfer characteristics…..

$$(v_I - V_t)v_O - \frac{1}{2}v_O^2 = \frac{1}{2}(V_{DD} - v_I - V_t)^2$$

$$v_I = V_{IH}$$

$$v_O = V_{IH} - \frac{V_{DD}}{2}$$

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$$



VIL can be determined in a manner similar to that used to find *VIH*. Alternatively, we can use the symmetry relationship.

$$V_{IH} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2} - V_{IL}$$

Hence we get,

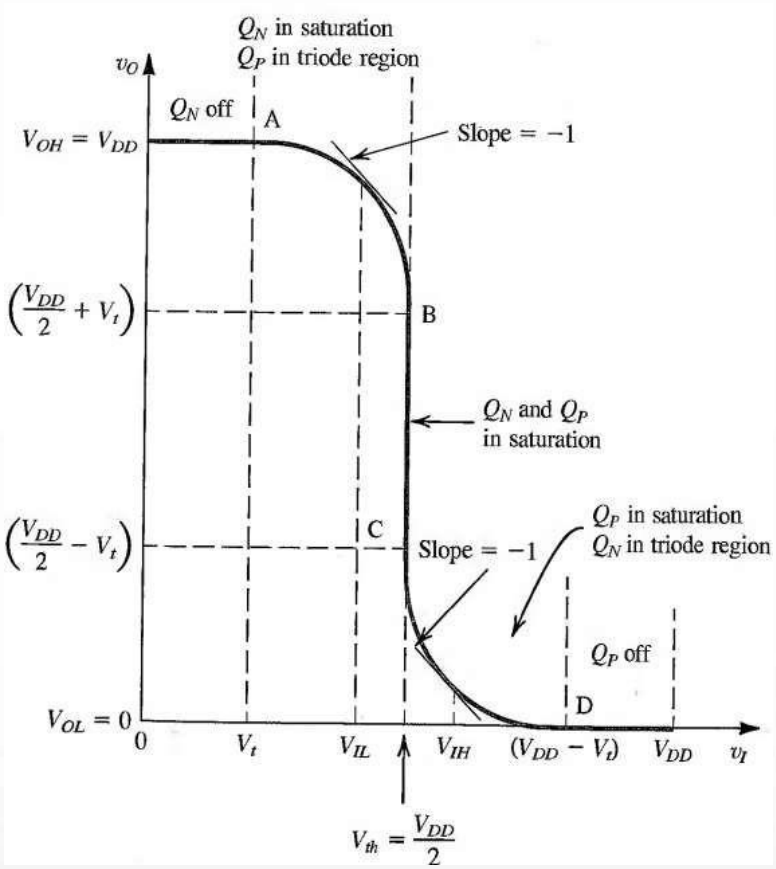
$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

CMOS voltage transfer characteristics…..

The noise margins can now be determined as follows:

$$NM_H = V_{OH} - V_{IH}$$
$$= V_{DD} - \tfrac{1}{8}(5V_{DD} - 2V_t)$$
$$= \tfrac{1}{8}(3V_{DD} + 2V_t)$$

$$NM_L = V_{IL} - V_{OL}$$
$$= \tfrac{1}{8}(3V_{DD} + 2V_t) - 0$$
$$= \tfrac{1}{8}(3V_{DD} + 2V_t)$$



The symmetry of the voltage transfer characteristic results in equal noise margins. If *QN and QP are not matched, the voltage* transfer characteristic *will no* longer be symmetric.